



**MOTOROLA**

DL129/D  
REV 5

# High-Speed CMOS Data

**Logic Integrated Circuits Division**

GLOBAL



EXCELLENCE



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# **MOTOROLA**

## **HIGH-SPEED CMOS LOGIC DATA**

This book presents technical data for the broad line of High-Speed Logic integrated circuits. Complete specifications are provided in the form of data sheets. In addition, a comprehensive Function Selector Guide and a Design Considerations chapter have been included to familiarize the user with these logic circuits.

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Series D

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# WHAT'S NEW! DATA SHEETS

Data Sheets Added		Data Sheets Deleted	
MC54/74HCT00A	MC54/74HCT245A	MC54/74HC03	MC54/74HC374
MC54/74HC03A	MC54/74HC273A	MC54/74HC04	MC54/74HC386
MC54/74HCT08A	MC54/74HCT273A	MC54/74HC76	MC54/74HC533
MC54/74HCT14A	MC54/74HC373A	MC54/74HC113	MC54/74HCT533
MC54/74HCT32A	MC54/74HC374A	MC54/74HC158	MC54/74HC534
MC54/74HCT74A	MC54/74HC534A	MC54/74HC161	MC54/74HCT534
MC54/74HCT138A	MC54/74HC573A	MC54/74HC163	MC54/74HCT540
MC54/74HCT157A	MC54/74HCT573A	MC54/74HC174	MC54/74HC573
MC54/74HC161A	MC54/74HC574A	MC54/74HC242	MC54/74HC574
MC54/74HC163A	MC54/74HCT574A	MC54/74HCT245	MC54/74HCT640
MC54/74HC174A	MC54/74HC4046A	MC54/74HC273	MC54/74HC648
MC54/74HCT174A	MC54/74HC4538A	MC54/74HC354	MC54/74HC4352
		MC54/74HC373	MC54/74HC4538

**“A” Versus “Non-A”** — Motorola has an on-going device performance enhancement program for the High-Speed CMOS family. This is indicated by the “A” suffix of the device identification. Some of the characteristics of this “A” enhancement program are improved design, a better quality process, faster performing AC propagation delays and enhancements to various dc characteristics.

The old “Non-A” process was a 5 micron process that was modified to run a 3.5 micron family. The new “A” process is a true 3 micron process and gives better process control, with improved performance and quality.

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# Function Selector Guide

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# BUFFERS/INVERTERS

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC04A HCT04A HCU04 HC14A HCT14A	Hex Inverter Hex Inverter with LSTTL-Compatible Inputs Hex Unbuffered Inverter Hex Schmitt-Trigger Inverter Hex Schmitt-Trigger Inverter with LSTTL-Compatible Inputs	LS04 LS04 LS04 LS14 LS14	*4069 *4069 4069 4584 4584	LS/CMOS LS/CMOS LS/CMOS LS/CMOS LS/CMOS	14 14 14 14 14
HC125A HC126A HC240A HCT240A HC241A	Quad 3-State Noninverting Buffer Quad 3-State Noninverting Buffer Octal 3-State Inverting Buffer/Line Driver/Line Receiver Octal 3-State Inverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	LS125,LS125A LS126,LS126A LS240 LS240 LS241		LS LS LS LS LS	14 14 20 20 20
HCT241A HC244A HCT244A HC245A HCT245A	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs Octal 3-State Noninverting Buffer/Line Driver/Line Receiver Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs Octal 3-State Noninverting Bus Transceiver Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS241 LS244 LS244 LS245 LS245		LS LS LS LS LS	20 20 20 20 20
HC365 HC366 HC367 HC368 HC540	Hex 3-State Noninverting Buffer with Common Enables Hex 3-State Inverting Buffer with Common Enables Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections Octal 3-State Inverting Buffer/Line Driver/Line Receiver	LS365,LS365A LS366,LS366A LS367,LS367A LS368,LS368A LS540	4503	LS LS LS/CMOS LS LS	16 16 16 16 20
HC541 HCT541 HC640A HC4049 HC4050	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs Octal 3-State Inverting Bus Transceiver Hex Inverting Buffer/Logic-Level Down Converter Hex Noninverting Buffer/Logic-Level Down Converter	LS541 LS541 LS640 LS640 LS640	4049 4050	LS LS LS CMOS CMOS	20 20 20 16 16

2

## BUFFERS/INVERTERS (Continued)

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HC HCT 04A	HCU 04	HC 14A	HC 125A	HC 126A	HC HCT 240A	HC HCT 241A	HC HCT 244A
# Pins	14	14	14	14	14	20	20	
Quad Device				•	•			
Hex Device	•	•	•					
Octal Device						•	•	•
Nine-Wide Device								
Noninverting Outputs				•	•		•	•
Inverting Outputs	•	•	•			•		
Single Stage (unbuffered)		•						
Schmitt Trigger			•					
3-State Outputs				•	•	•	•	•
Open-Drain Outputs								
Common Output Enables						•	•	•
Active-Low Output Enables				•		•	•	•
Active-High Output Enables					•	•	•	•
Separate 4-Bit Sections						•	•	•
Separate 2-Bit and 4-Bit Sections								
Transceiver								
Direction Control								
Logic-Level Down Converter								

2

## BUFFERS/INVERTERS (Continued)

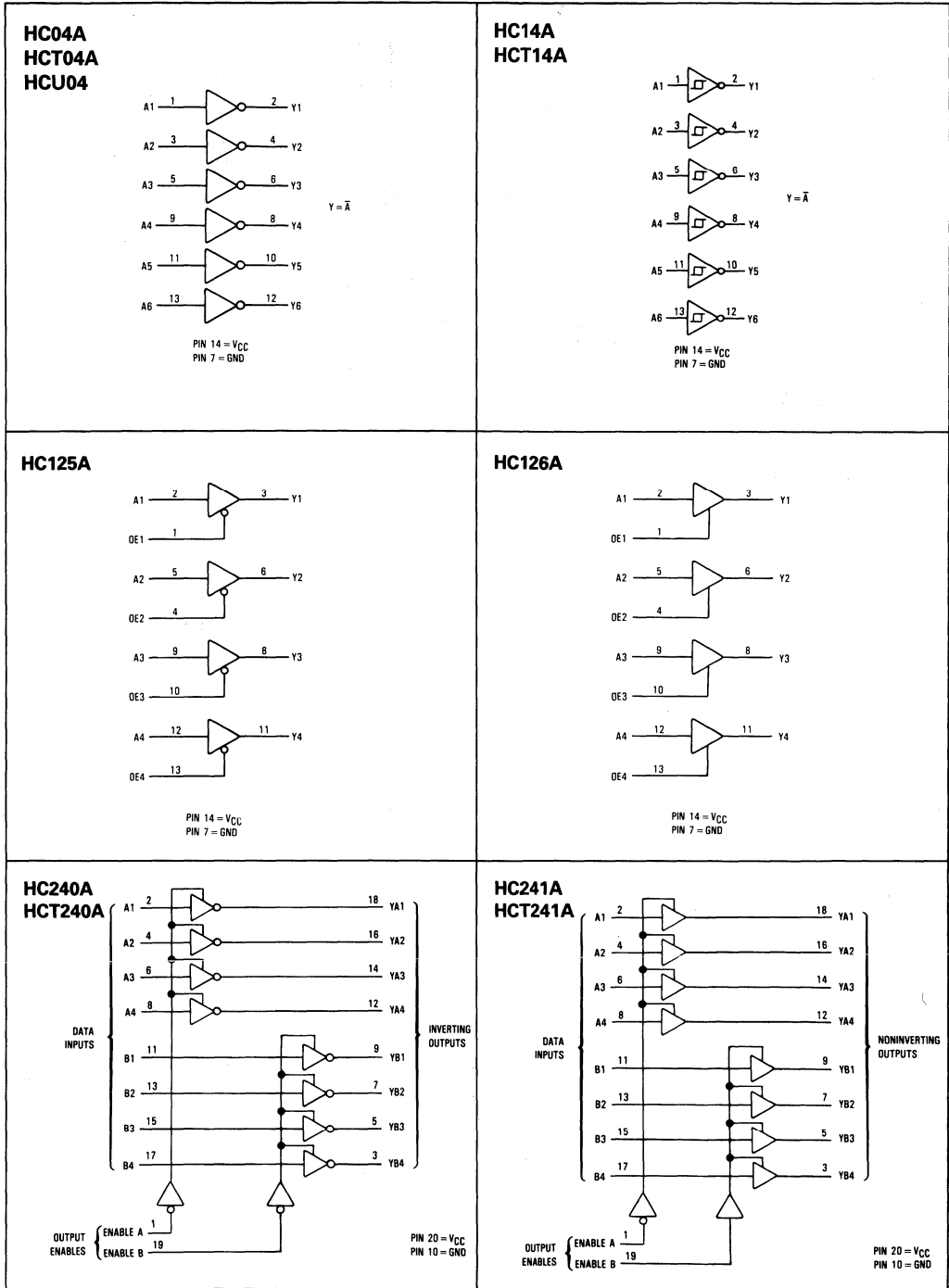
HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HC HCT 245A	HC 365	HC 366	HC 367	HC 368	HC 540	HC HCT 541	HC 640A
# Pins	20	16	16	16	16	20	20	20
Quad Device		•	•	•	•			
Hex Device	•					•	•	•
Octal Device								
Nine-Wide Device								
Noninverting Outputs	•	•		•			•	
Inverting Outputs			•		•	•		•
Single Stage (unbuffered)								
Schmitt Trigger								
3-State Outputs	•	•	•	•	•	•	•	•
Open-Drain Outputs								
Common Output Enables	•	•	•			•	•	•
Active-Low Output Enables	•	•	•	•	•	•	•	•
Active-High Output Enables								
Separate 4-Bit Sections				•	•			
Separate 2-Bit and 4-Bit Sections								
Transceiver	•							•
Direction Control	•							•
Logic-Level Down Converter								

HC Devices Have CMOS-Compatible Inputs.  
HCT Devices Have LSTTL-Compatible Inputs.

Device	HC 4049	HC 4050
# Pins	16	16
Quad Device		
Hex Device	•	•
Octal Device		
Nine-Wide Device		
Noninverting Outputs		•
Inverting Outputs	•	
Single Stage (unbuffered)		
Schmitt Trigger		
3-State Outputs		
Open-Drain Outputs		
Common Output Enables		
Active-Low Output Enables		
Active-High Output Enables		
Separate 4-Bit Sections		
Separate 2-Bit and 4-Bit Sections		
Transceiver		
Direction Control		
Logic-Level Down Converter	•	•

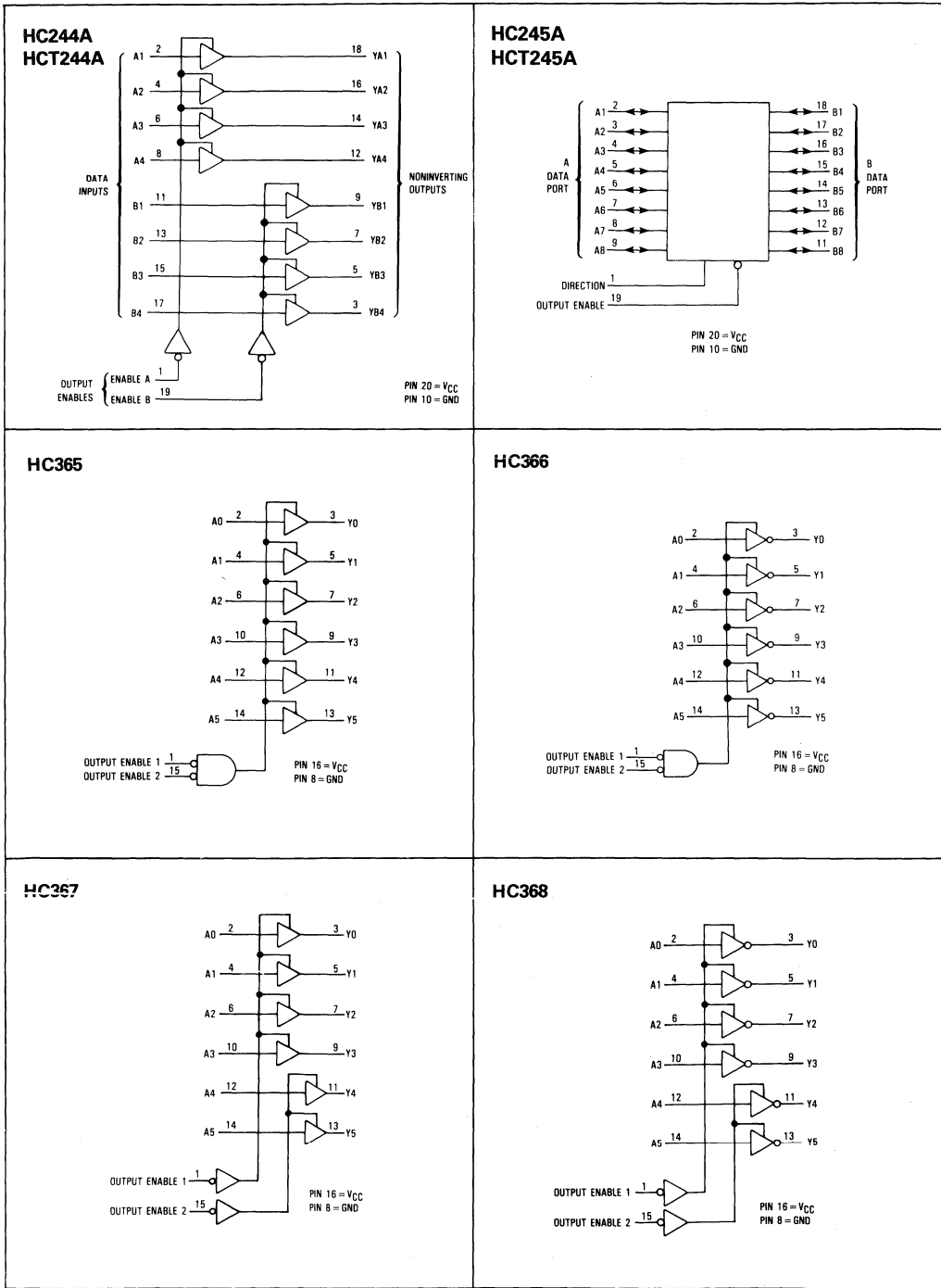
# BUFFERS/INVERTERS (Continued)



2

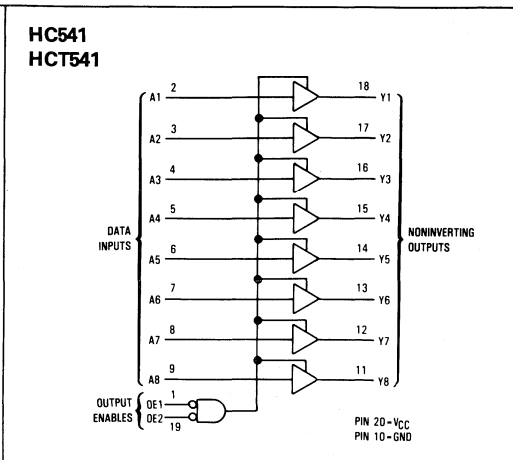
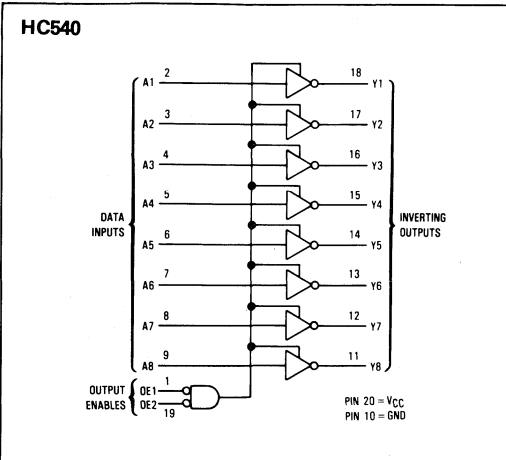
# BUFFERS/INVERTERS (Continued)

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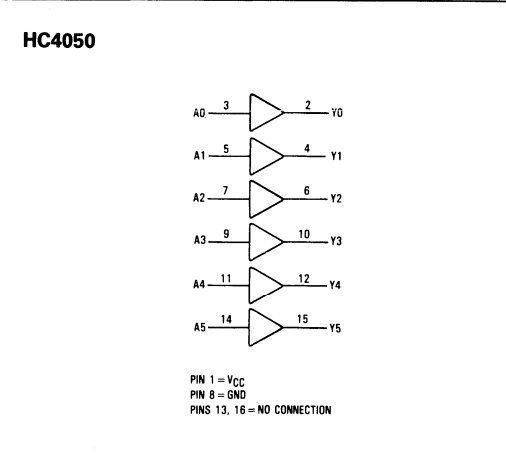
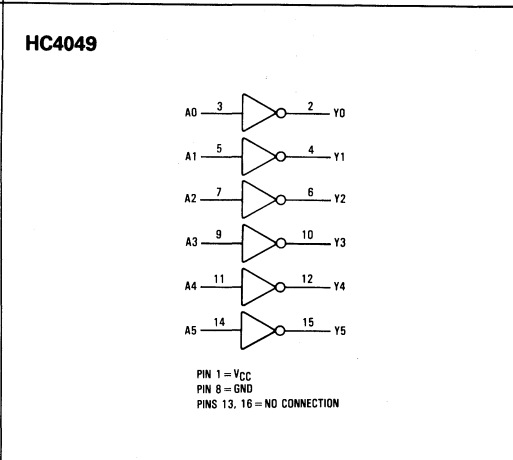
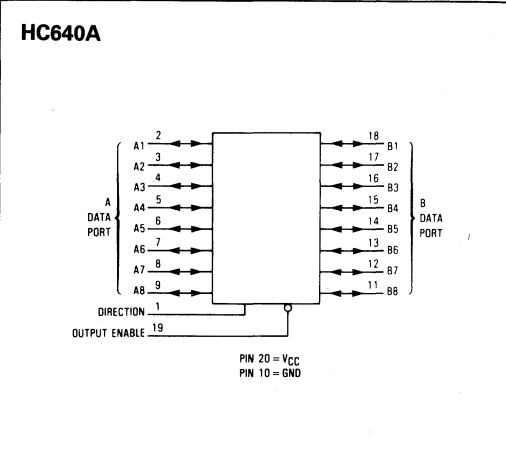




# BUFFERS/INVERTERS (Continued)



2



# GATES

**2**

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC00A	Quad 2-Input NAND Gate	LS00	4011	LS	14
HCT00A	Quad 2-Input NAND Gate with LSTTL-Compatible Inputs	LS00	4001	LS	14
HC02A	Quad 2-Input NOR Gate	LS02	4001	LS	14
HC03A	Quad 2-Input NAND Gate with Open-Drain Outputs	LS03	*4011	LS	14
HC08A	Quad 2-Input AND Gate	LS08	4081	LS	14
HCT08A	Quad 2-Input AND Gate with LSTTL-Compatible Inputs	LS08	4081	LS	14
HC10	Triple 3-Input NAND Gate	LS10	4023	LS	14
HC11	Triple 3-Input AND Gate	LS11	4073	LS	14
HC20	Dual 4-Input NAND Gate	LS20	4012	LS	14
HC27	Triple 3-Input NOR Gate	LS27	4025	LS	14
HC30	8-Input NAND Gate	LS30	4068	LS	14
HC32A	Quad 2-Input OR Gate	LS32	4071	LS	14
HCT32A	Quad 2-Input OR Gate with LSTTL-Compatible Inputs	LS32	4071	LS	14
HC51	2-Wide, 2-Input/2-Wide, 3-Input AND-NOR Gates	LS51	*4506	LS	14
★HC58	2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates		*4506		14
HC86	Quad 2-Input Exclusive OR Gate	LS86	4070	LS	14
HC132A	Quad 2-Input NAND Gate with Schmitt-Trigger Inputs	LS132	4093	LS	14
HC133	13-Input NAND Gate	LS133		LS	16
HC4002	Dual 4-Input NOR Gate	*LS25	4002	CMOS	14
HC4075	Triple 3-Input OR Gate		4075	CMOS	14
HC4078	8-Input NOR/OR Gate		4078	CMOS	14
★HC7266	Quad 2-Input Exclusive NOR Gate	*LS266	4077	LS/CMOS	14

\*Suggested alternative

★Exclusive High-Speed CMOS design

## GATES (Continued)

HC Devices Have CMOS-Compatible Inputs.

Device	HC HCT 00A	HC 02A	HC 03A	HC HCT 08A	HC 10	HC 11	HC 20	HC 27	HC 30	HC HCT 32A
# Pins	14	14	14	14	14	14	14	14	14	14
Single Device										
Dual Device							•		•	
Triple Device	•	•	•	•	•	•		•		•
Quad Device										
NAND	•		•		•		•		•	
NOR		•						•		
AND				•		•				
OR										•
Exclusive OR										
Exclusive NOR										
AND-NOR										
AND-OR										
2-Input	•	•	•	•						•
3-Input					•	•		•		
4-Input							•			
8-Input									•	
13-Input										
Schmitt-Trigger Inputs										
Open-Drain Outputs			•							

HC Devices Have CMOS-Compatible Inputs.

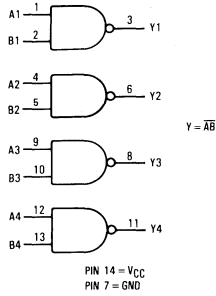
Device	HC 51	HC 58	HC 86	HC 132A	HC 133	HC 4002	HC 4075	HC 4078	HC 7266
# Pins	14	14	14	14	16	14	14	14	14
Single Device						•		•	
Dual Device	•	•							
Triple Device				•	•	•	•		
Quad Device									•
NAND					•				
NOR						•		•	
AND							•		
OR								•	
Exclusive OR				•					
Exclusive NOR									•
AND-NOR	•								
AND-OR		•							
2-Input	•	•	•	•					•
3-Input	•	•							
4-Input						•	•		
8-Input								•	
13-Input					•				
Schmitt-Trigger Inputs				•					
Open-Drain Outputs									

2

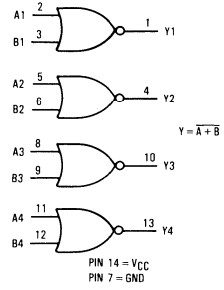
# GATES (Continued)

2

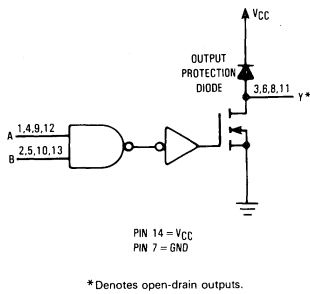
## HC00A HCT00A



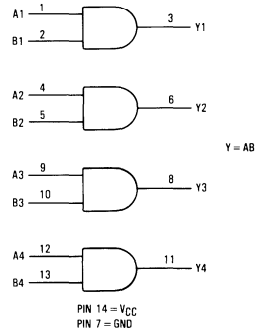
## HC02A



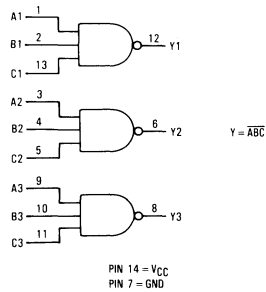
## HC03A



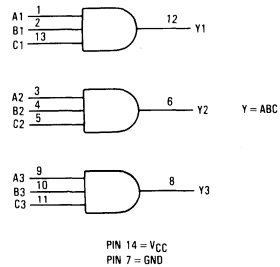
## HC08A HCT08A



## HC10

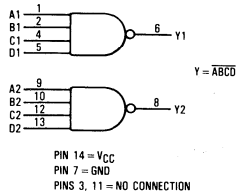


## HC11

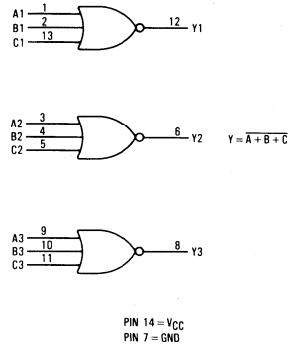


# GATES (Continued)

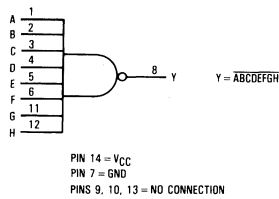
## HC20



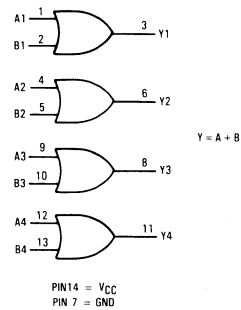
## HC27



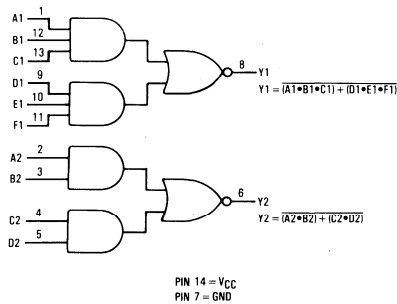
## HC30



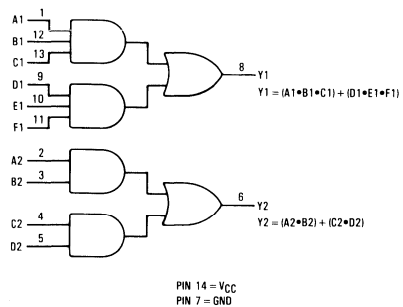
## HC32A HCT32A



## HC51

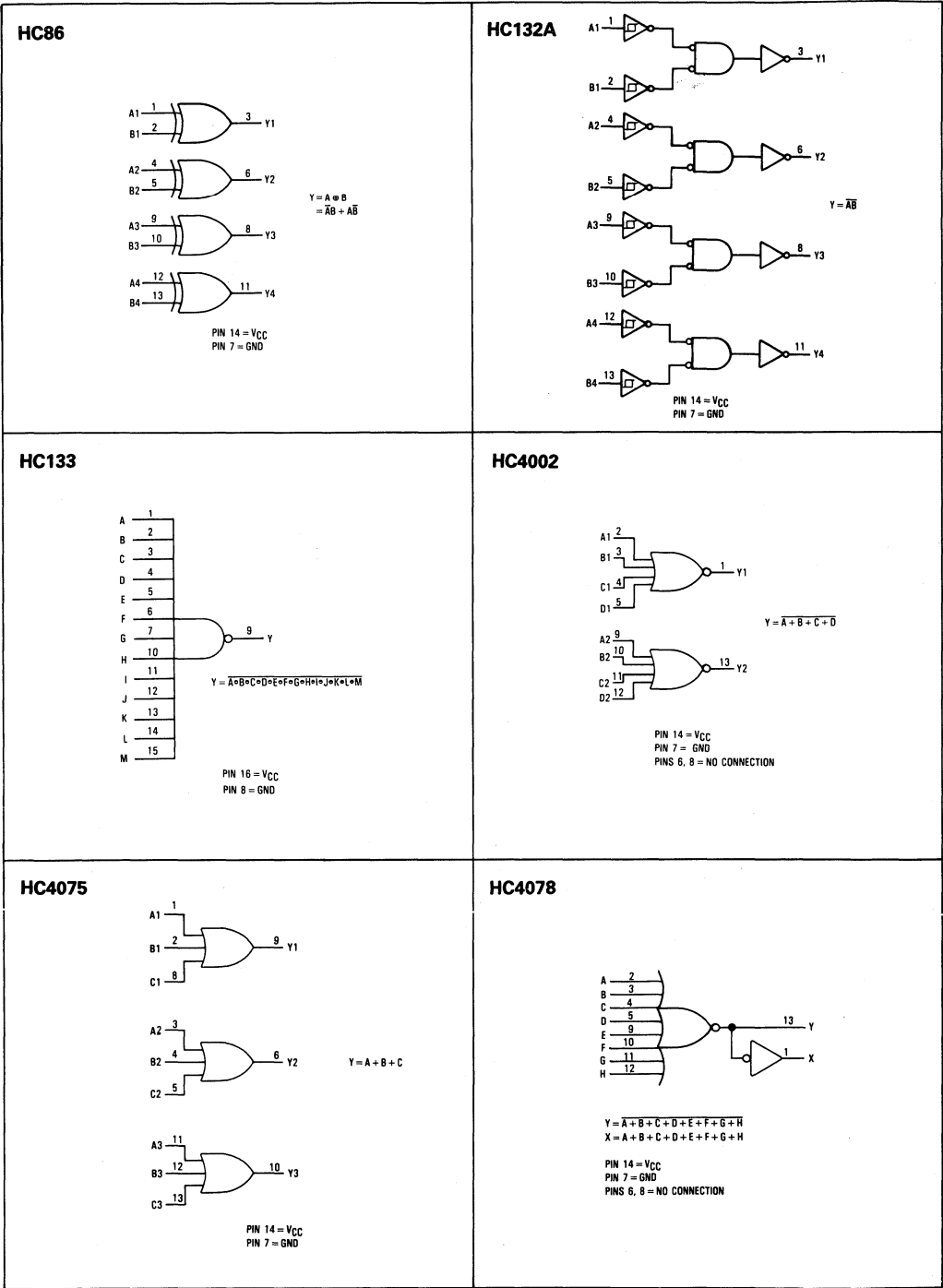


## HC58

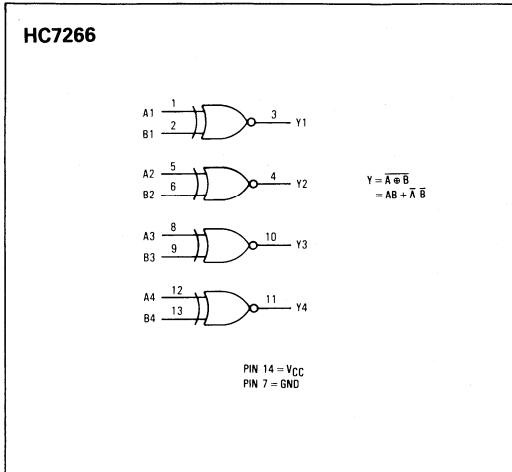


# GATES (Continued)

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## GATES (Continued)

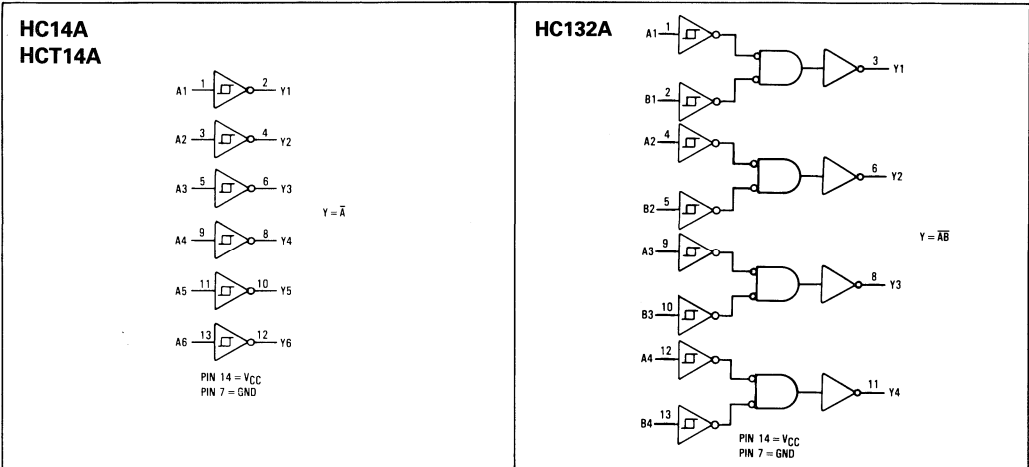


2

# SCHMITT TRIGGERS

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC14A	Hex Schmitt-Trigger Inverter	LS14	4584	LS/CMOS	14
HCT14A	Hex Schmitt-Trigger Inverter with LSTTL-Compatible Inputs	LS14	4584	LS	14
HC132A	Quad 2-Input NAND Gate with Schmitt-Trigger Inputs	LS132	4093	LS	14

2





# BUS TRANSCEIVERS

2

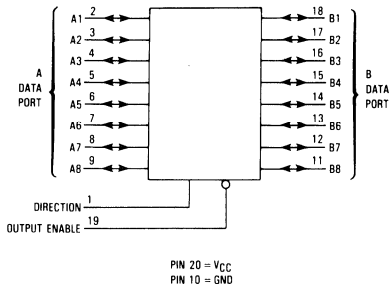
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC245A	Octal 3-State Noninverting Bus Transceiver	LS245		LS	20
HCT245A	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS245		LS	20
HC640A	Octal 3-State Inverting Bus Transceiver	LS640		LS	20
HC646	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS646		LS	24

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

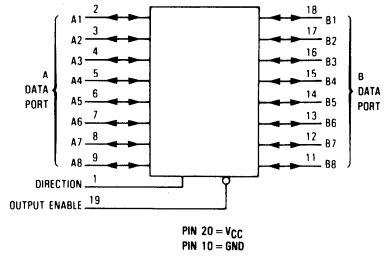
Device	HC HCT 245A	HC HCT 640A	HC 646
# Pins	20	20	24
Quad Device			
Octal Device	•	•	•
Buffer	•	•	•
Storage Capability			•
Inverting Outputs		•	
Noninverting Outputs	•		•
Common Output Enable	•	•	•
Active-Low Output Enable	•	•	•
Active-High Output Enable			
Direction Control	•	•	•

# BUS TRANSCEIVERS (Continued)

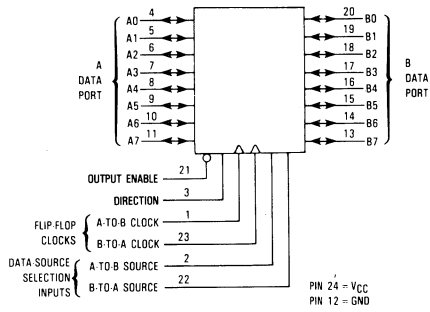
## HC245 HCT245A



## HC640A



## HC646



2

# LATCHES

2

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC75	Dual 2-Bit Transparent Latch	LS75		LS	16
HC259	8-Bit Addressable Latch/1-of-8 Decoder	LS259		LS	16
HC373A	Octal 3-State Noninverting Transparent Latch	LS373,LS573		LS373	20
HCT373A	Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs	LS373,LS573		LS373	20
HC563	Octal 3-State Inverting Transparent Latch	LS533,LS563		LS563	20
HC573A	Octal 3-State Noninverting Transparent Latch	LS373,LS573		LS573	20
HCT573A	Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs	LS373,LS573		LS573	20

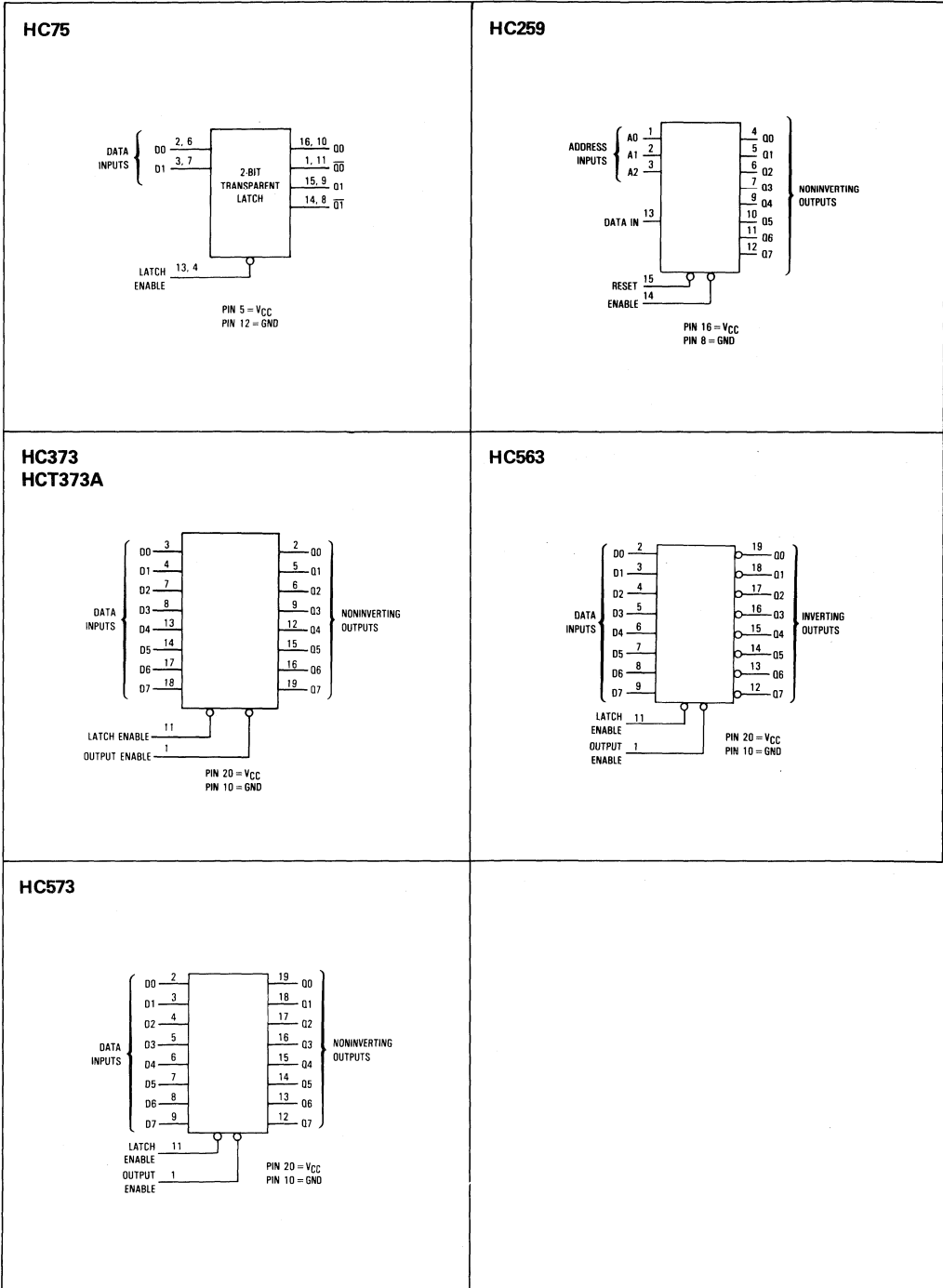
HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HC 75	HC 259	HC HCT 373A	HC 563	HC HCT 573A
# Pins	16	16	20	20	20
Single Device		•			
Dual Device	•				
Octal Device			•	•	•
Number of Bits Controlled by Latch Enable:					
2	•				
8			•	•	•
Transparent	•		•	•	•
Addressable		•			
Readback Capability				•	•
Noninverting Outputs	•	•	•		•
Inverting Outputs	•			•	
Common Latch Enable, Active-Low	•		•	•	•
3-State Outputs			•	•	•
Common Output Enable, Active-Low			•	•	•

These devices are identical in function and are different in pinout only: HC/HCT373A and HC/HCT573A

# LATCHES (Continued)

2



# FLIP-FLOPS

2

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC73	Dual J-K Flip-Flop with Reset	LS73,LS73A,LS107,LS107A	*4027	LS73,LS73A	14
HC74A	Dual D Flip-Flop with Set and Reset	LS74,LS74A	*4013	LS	14
HCT74A	Dual D Flip-Flop with Set and Reset with LSTTL-Compatible Inputs	LS74,LS74A	4013	LS	14
HC107	Dual J-K Flip-Flop with Reset	LS73,LS73A,LS107,LS107A	*4027	LS107,LS107A	14
HC109	Dual J-K̄ with Set and Reset	LS109,LS109A	*4027	LS	16
HC112	Dual J-K Flip-Flop with Set and Reset	LS76,LS76A,LS112,LS112A	*4027	LS112,LS112A	16
HC173	Quad 3-State D Flip-Flop with Common Clock and Reset	LS173,LS173A	4076	LS/CMOS	16
HC174A	Hex D Flip-Flop with Common Clock and Reset	LS174	4174	LS/CMOS	16
HCT174A	Hex D Flip-Flop with Common Clock and Reset with LSTTL-Compatible Inputs	LS174	4174	LS	16
HC175	Quad D Flip-Flop with Common Clock and Reset	LS175	4175	LS/CMOS	16
HC273A	Octal D Flip-Flop with Common Clock and Reset	LS273		LS	20
HCT273A	Octal D Flip-Flop with Common Clock and Reset with LSTTL-Compatible Inputs	LS273		LS	20
HC374A	Octal 3-State Noninverting D Flip-Flop	LS374,LS574		LS374	20
HCT374A	Octal 3-State Noninverting D Flip-Flop with LSTTL-Compatible Inputs	LS374,LS574		LS374	20
HC534A	Octal 3-State Inverting D Flip-Flop	LS534,LS564		LS534	20
HC564	Octal 3-State Inverting D Flip-Flop	LS534,LS564		LS564	20
HC574A	Octal 3-State Noninverting D Flip-Flop	LS374,LS574		LS574	20
HCT574A	Octal 3-State Noninverting D Flip-Flop with LSTTL-Compatible Inputs	LS374,LS574		LS	20
HC646	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS646		LS	24

\*Suggested alternative

## FLIP-FLOPS (Continued)

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HC 73	HC HCT 74A	HC 107	HC 109	HC 112	HC 173	HC HCT 174A	HC 175
# Pins	14	14	14	16	16	16	16	16
Type	J-K	D	J-K	J- $\bar{K}$	J-K	D	D	D
Dual Device	•	•	•	•	•	•	•	•
Quad Device								
Hex Device								
Octal Device								
Common Clock						•	•	•
Negative-Transition Clocking	•		•		•	•	•	•
Positive-Transition Clocking		•		•		•	•	•
Common, Active-Low Data Enables						•		
Noninverting Outputs	•	•	•	•	•	•	•	•
Inverting Outputs	•	•	•	•	•	•	•	•
3-State Outputs						•		
Common, Active-Low Output Enables						•		
Common Reset						•	•	•
Active-Low Reset	•	•	•	•	•	•	•	•
Active-High Reset						•		
Active-Low Set		•		•	•			
Transceiver Direction Control								

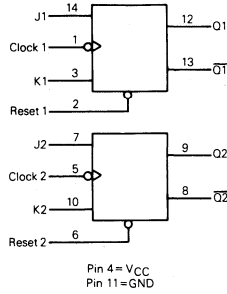
HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HC HCT 273A	HC HCT 374A	HC 534A	HC 564	HC HCT 574A	HC 646
# Pins	20	20	20	20	20	24
Type	D	D	D	D	D	D
Dual Device						
Quad Device						
Hex Device						
Octal Device	•	•	•	•	•	•
Common Clock	•	•	•	•	•	•
Negative-Transition Clocking						
Positive-Transition Clocking	•	•	•	•	•	•
Common, Active-Low Data Enables						
Noninverting Outputs	•	•		•	•	•
Inverting Outputs			•	•		
3-State Outputs		•	•	•	•	•
Common, Active-Low Output Enables		•	•	•	•	•
Common Reset	•					
Active-Low Reset	•					
Active-High Reset						
Active-Low Set						
Transceiver Direction Control						• •

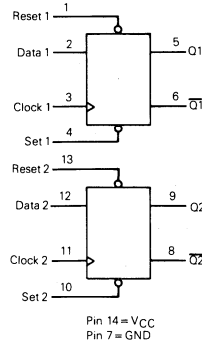
These devices are identical in function and are different in pinout only: HC73 and HC107  
 HC374 and HC574  
 HC534 and HC564

# FLIP-FLOPS (Continued)

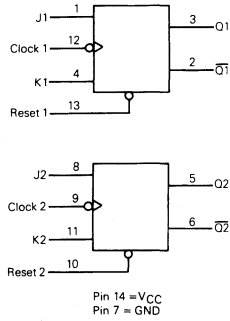
**HC73**



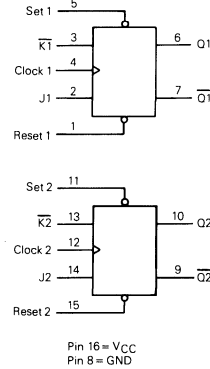
**HC74A  
HCT74A**



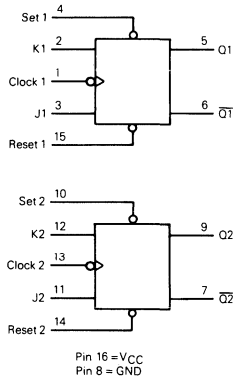
**HC107**



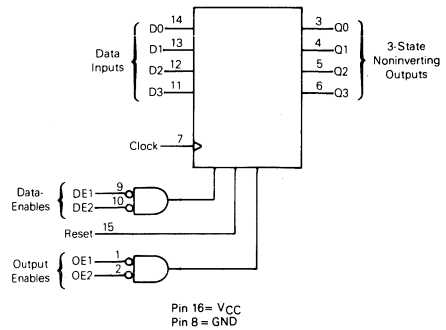
**HC109**



**HC112**

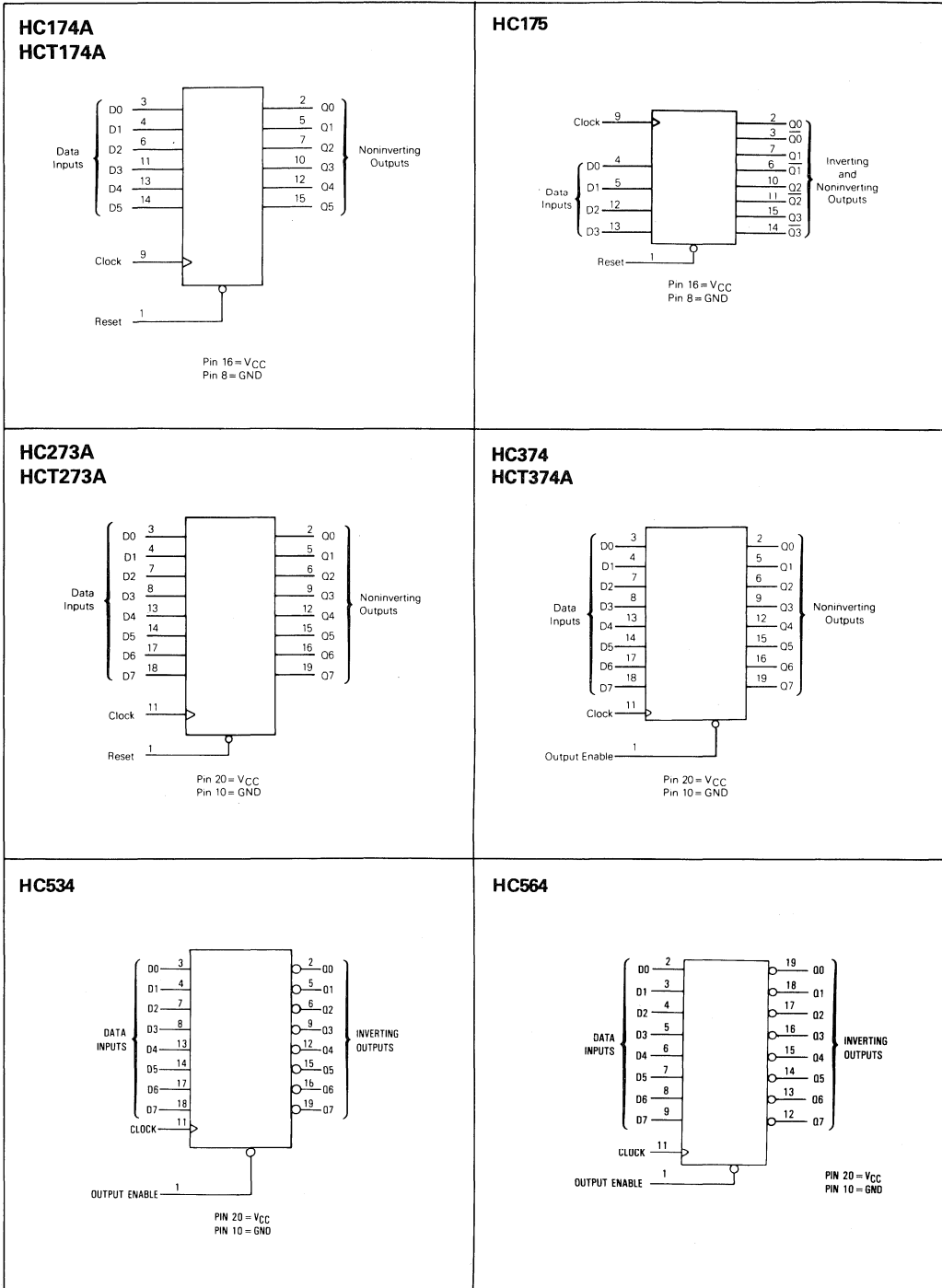


**HC173**



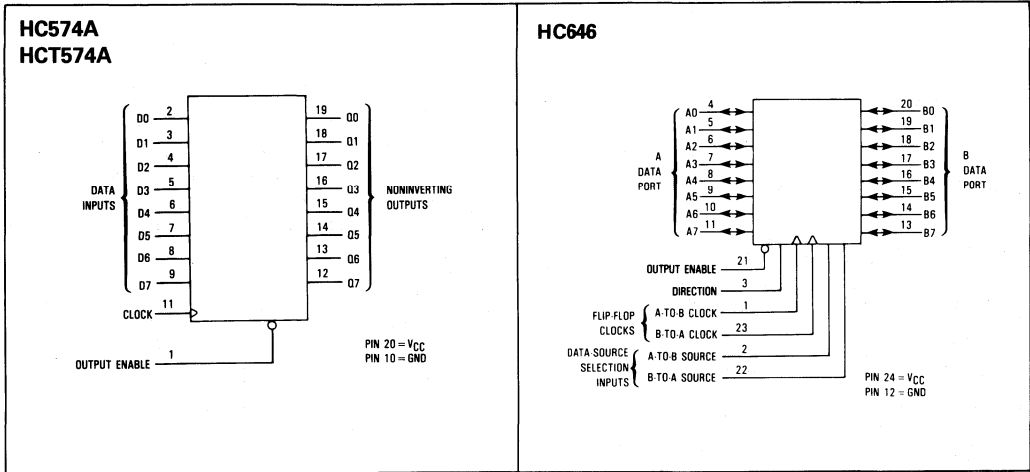
## FLIP-FLOPS (Continued)

2





## FLIP-FLOPS (Continued)



2

## DIGITAL DATA SELECTORS/MULTIPLEXERS

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC151	8-Input Data Selector/Multiplexer	LS151	*4512	LS	16
HC153	Dual 4-Input Data Selector/Multiplexer	LS153	4539	LS/CMOS	16
HC157A	Quad 2-Input Noninverting Data Selector/Multiplexer	LS157	*4519	LS	16
HCT157A	Quad 2-Input Data Selector/Multiplexer with LSTTL-Compatible Inputs	LS157	*4519	LS	16
HC251	8-Input Data Selector/Multiplexer with 3-State Outputs	LS251	*4512	LS	16
HC253	Dual 4-Input Data Selector/Multiplexer with 3-State Outputs	LS253	*4539	LS/CMOS	16
HC257	Quad 2-Input Data Selector/Multiplexer with 3-State Outputs	LS257	*4519	LS	16

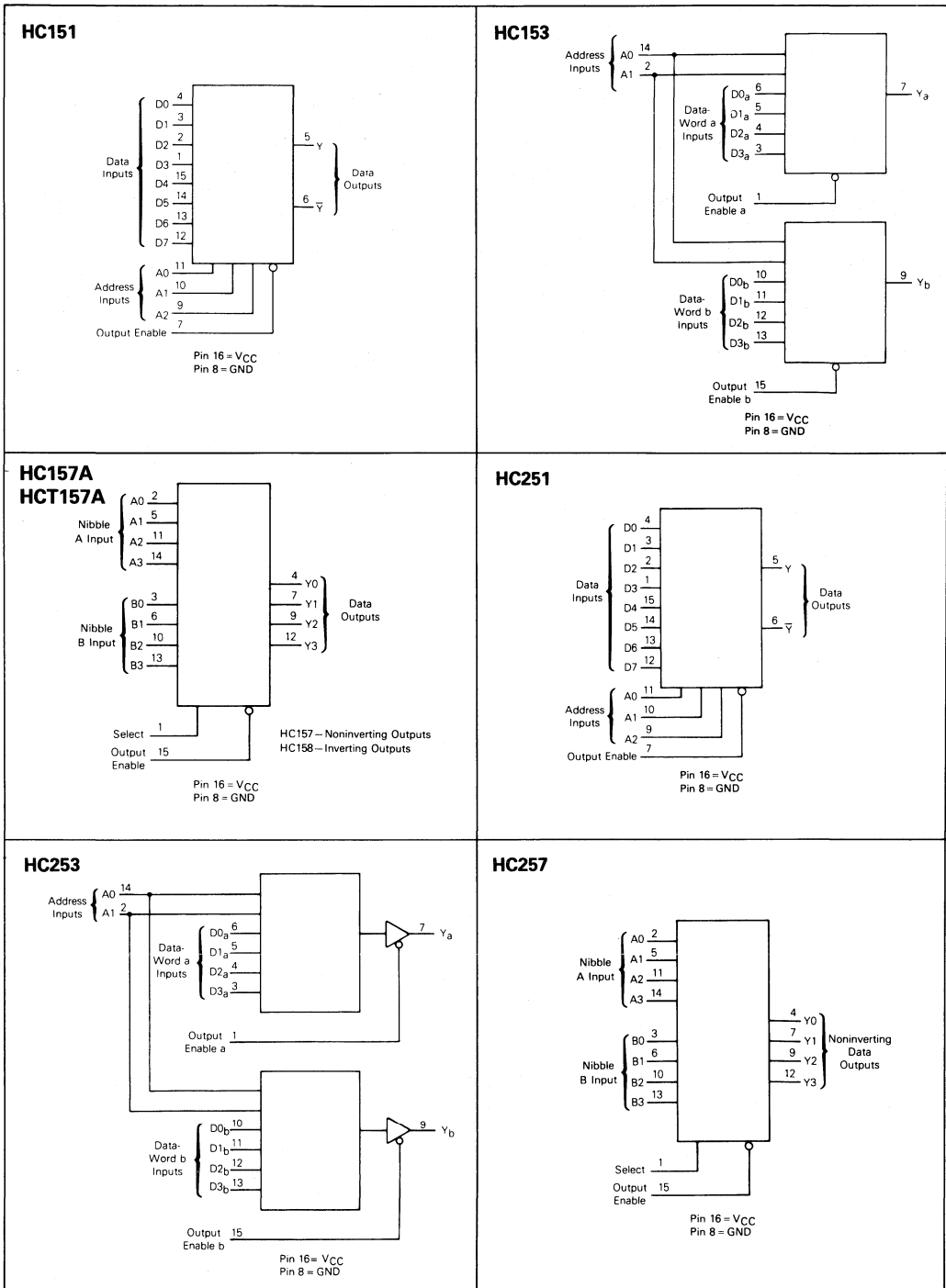
\*Suggested alternative

HC Devices Have CMOS-Compatible Inputs.

Device	HC 151	HC 153	HC HCT 157A	HC 251	HC 253	HC 257
# Pins	16	16	16	16	16	16
Description	One of 8 inputs is selected	One of 4 inputs is selected	One of two 4-bit words is selected	One of 8 inputs is selected	One of 4 inputs is selected	One of two 4-bit words is selected
Single Device	•	•		•	•	
Dual Device						
Quad Device			•			•
Data Latch with Active-Low Latch Enable						
Common Address		•	•		•	•
1-Bit Binary Address			•			•
2-Bit Binary Address		•			•	
3-Bit Binary Address	•			•		
Address Latch (Transparent)						•
Address Latch (Non-transparent)						
Active-Low Address Latch Enable						
Noninverting Output	•	•	•	•	•	•
Inverting Output	•			•		
3-State Outputs				•	•	•
Common Output Enable			•			•
Active-High Output Enable						
Active-Low Output Enable	•	•	•	•	•	•

•• implies the device has two such enables

# DIGITAL DATA SELECTORS/MULTIPLEXERS (Continued)



# DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS

2

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC42	1-of-10 Decoder	LS42	*4028	LS	16
HC137	1-of-8 Decoder/Demultiplexer with Address Latch	LS137	*4028	LS	16
HC138A	1-of-8 Decoder/Demultiplexer	LS138	*4028	LS	16
HCT138A	1-of-8 Decoder/Demultiplexer with LSTTL-Compatible Inputs	LS138	*4028	LS	16
HC139A	Dual 1-of-4 Decoder/Demultiplexer	LS139	4556	LS/CMOS	16
HC147	Decimal-to-BCD Encoder	LS147		LS	16
HC154	1-of-16 Decoder/Demultiplexer	LS154,*LS159	*4515	LS	24
★HC237	1-of-8 Decoder/Demultiplexer with Address Latch	*LS137	*4208		16
HC259	8-Bit Addressable Latch/1-of-8 Decoder	LS259		LS	16
HC4511	BCD-to-Seven-Segment Latch/Decoder/Display Driver	*LS47,*LS48, *LS49	4511	CMOS	16
HC4514	1-of-16 Decoder/Demultiplexer with Address Latch	*LS154,*LS159	4514,*4515	CMOS	24

\*Suggested alternative

★Exclusive High-Speed CMOS design

## DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS (Continued)

HC Devices Have CMOS-Compatible Inputs.

Device	HC 42	HC 137	HC HCT 138A	HC 139A	HC 147	HC 154
# Pins	16	16	16	16	16	24
Input Description	BCD Address	3-Bit Binary Address	3-Bit Binary Address	2-Bit Binary Address	Any Combination of 9 Inputs	4-Bit Binary Address
Output Description	One of 10	One of 8	One of 8	One of 4	BCD Address of Highest Input	One of 16
Single Device Dual Device	• •	• •	• •	• •	• •	• •
Address Input Latch Active-High Latch Enable Active-Low Latch Enable		• •				
Active-Low Inputs					•	
Active-Low Outputs Active-High Outputs	• •	• •	• •	• •	• •	• •
Active-Low Output Enable Active-High Output Enable		• •	•• •	•		••
Active-Low Reset						
Active-Low Blanking Input Active-High Blanking Input						
Active-Low Lamp-Test Input						
Phase Input (for LCD's)						

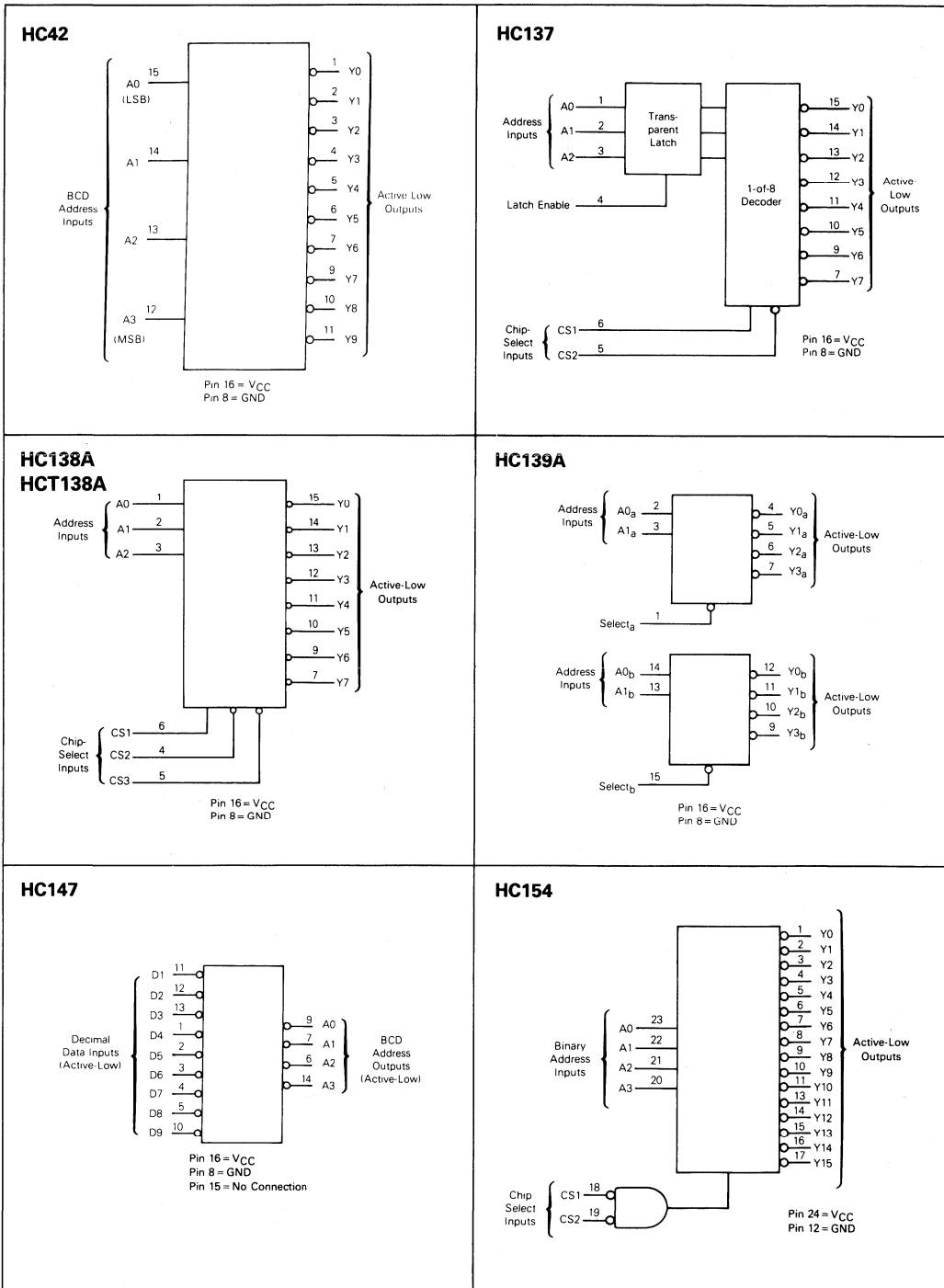
••implies the device has two such enables

HC Devices Have CMOS-Compatible Inputs.

Device	HC 237	HC 259	HC 4511	HC 4514
# Pins	16	16	16	24
Input Description		3-Bit Binary Address	3-Bit Binary Address	BCD Data
Output Description		One of 8	One of 8	7-Segment Display
Single Device Dual Device	• •	• •	• •	• •
Address Input Latch Active-High Latch Enable Active-Low Latch Enable		• •	• •	• •
Active-Low Inputs				
Active-Low Outputs Active-High Outputs		• •	• •	• •
Active-Low Output Enable Active-High Output Enable		• •	•	•
Active-Low Reset			•	
Active-Low Blanking Input Active-High Blanking Input			•	
Active-Low Lamp-Test Input			•	
Phase Input (for LCD's)				

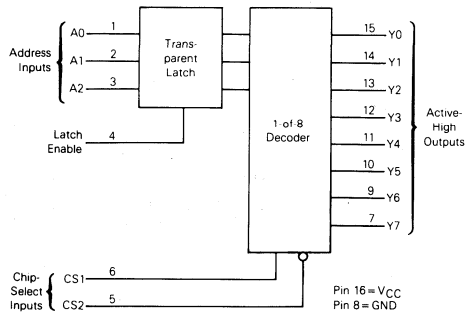
# DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS (Continued)

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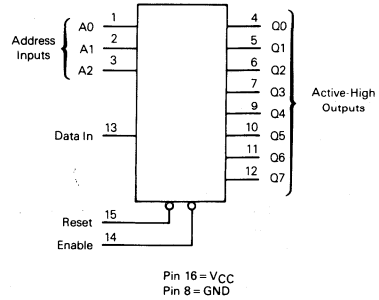


# DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS (Continued)

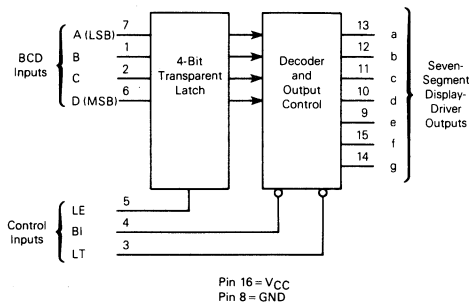
**HC237**



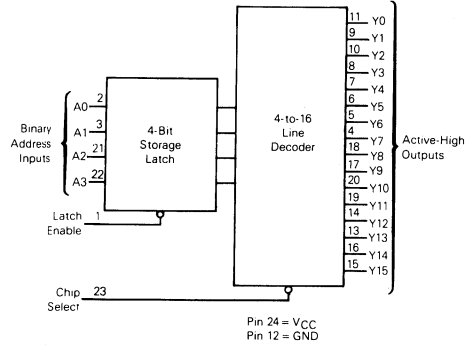
**HC259**



**HC4511**



**HC4514**



2

# ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS

2

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC4016	Quad Analog Switch/Multiplexer/Demultiplexer		4016,4066	CMOS	14
HC4051	8-Channel Analog Multiplexer/Demultiplexer		4051	CMOS	16
HC4052	Dual 4-Channel Analog Multiplexer/Demultiplexer		4052	CMOS	16
HC4053	Triple 2-Channel Analog Multiplexer/Demultiplexer		4053	CMOS	16
HC4066	Quad Analog Switch/Multiplexer/Demultiplexer		4066,4016	CMOS	14
★HC4316	Quad Analog Switch/Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies		*4016		16
★HC4351	8-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4051		20
★HC4353	Triple 2-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4053		20

\*Suggested alternative  
 ★High-Speed CMOS design only



## ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS (Continued)

HC Devices Have CMOS-Compatible Inputs.

Device	HC 4016	HC 4051	HC 4052	HC 4053	HC 4066
# Pins	14	16	16	16	14
Description	4 Independently Controlled Switches	A 3-Bit Address Selects One of 8 Switches	A 2-Bit Address Selects One of 4 Switches	A 3-Bit Address Selects Varying Combinations of the 6 Switches	4 Independently Controlled Switches
Single Device Dual Device Triple Device Quad Device	•	•	•	•	•
1-to-1 Multiplexing 2-to-1 Multiplexing 4-to-1 Multiplexing 8-to-1 Multiplexing	•	•	•	•	•
Active-High ON/OFF Control	•				•
Common Address Inputs 2-Bit Binary Address 3-Bit Binary Address Address Latch with Active-Low Latch Enable		•	•	•	
Common Switch Enable Active-Low Enable Active-High Enable		•	•	•	
Separate Analog and Control Reference Power Supplies		•	•	•	
Switched Tubs (for R <sub>ON</sub> and Prop. Delay Improvement)					•

2

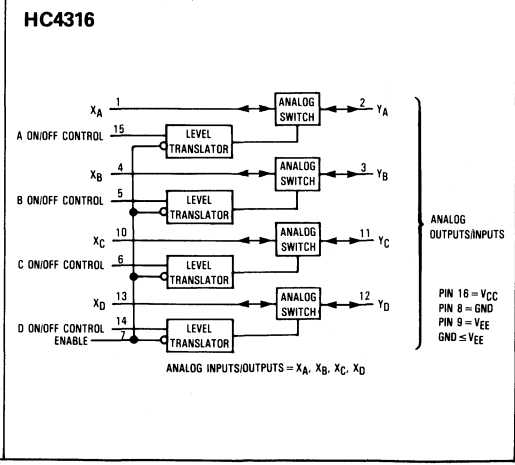
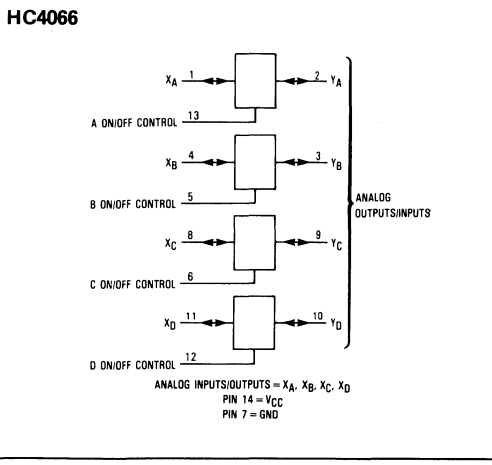
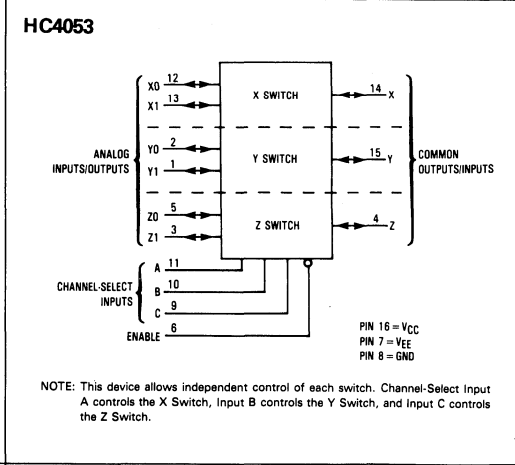
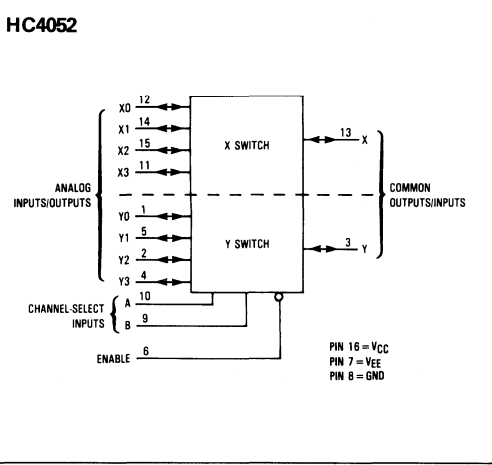
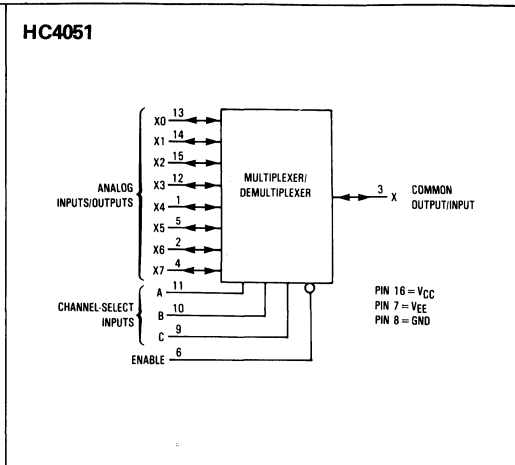
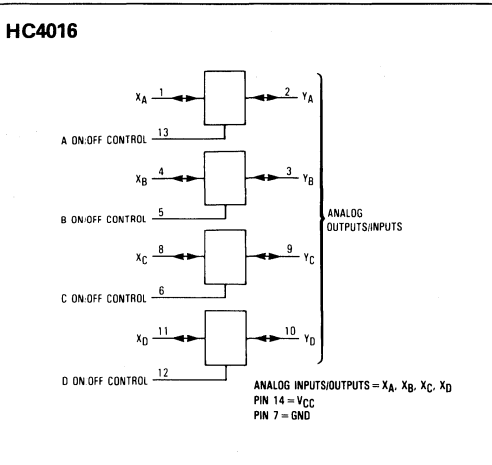
HC Devices Have CMOS-Compatible Inputs.

Device	HC 4316	HC 4351	HC 4353
# Pins	16	20	20
Description	4 Independently Controlled Switches (Has a Separate Analog Lower Power Supply)	A 3-Bit Address Selects One of 8 Switches (Has an Address Latch)	A 3-Bit Address Selects Varying Combinations of the 6 Switches (Has an Address Latch)
Single Device Dual Device Triple Device Quad Device	•	•	•
1-to-1 Multiplexing 2-to-1 Multiplexing 4-to-1 Multiplexing 8-to-1 Multiplexing	•	•	•
Active-High ON/OFF Control	•		
Common Address Inputs 2-Bit Binary Address 3-Bit Binary Address Address Latch with Active-Low Latch Enable		•	•
Common Switch Enable Active-Low Enable Active-High Enable	•	••	••
Separate Analog and Control Reference Power Supplies	•	•	•
Switched Tubs (for R <sub>ON</sub> and Prop. Delay Improvement)			

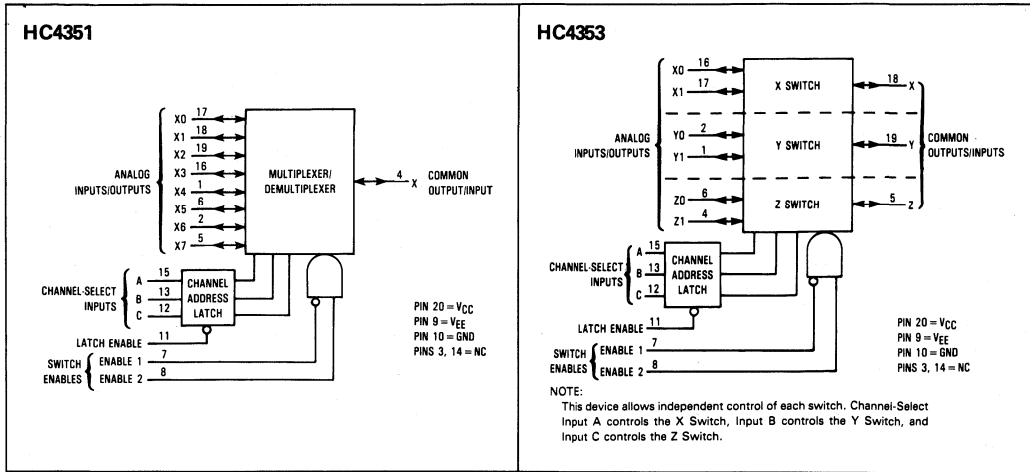
••implies the device has two such enables

# ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS (Continued)

2



# ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS (Continued)



# SHIFT REGISTERS

2

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC164	8-Bit Serial-Input/Parallel-Output Shift Register	LS164	*4034	LS	14
HC165	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register	LS165	*4021	LS	16
HC194	4-Bit Bidirectional Universal Shift Register	LS194,LS194A	4194	LS/CMOS	16
HC195	4-Bit Universal Shift Register	LS196,LS195A	*4035	LS	16
HC299	8-Bit Bidirectional Universal Shift Register with Parallel I/O	LS299		LS	20
HC589	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with 3-State Output	LS589		LS	16
HC595A	8-Bit Serial-Input/Serial- or Parallel-Output Shift Register with Latched 3-State Outputs	LS595	*4034	LS	16
HC597	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with Input Latch	LS597		LS	16

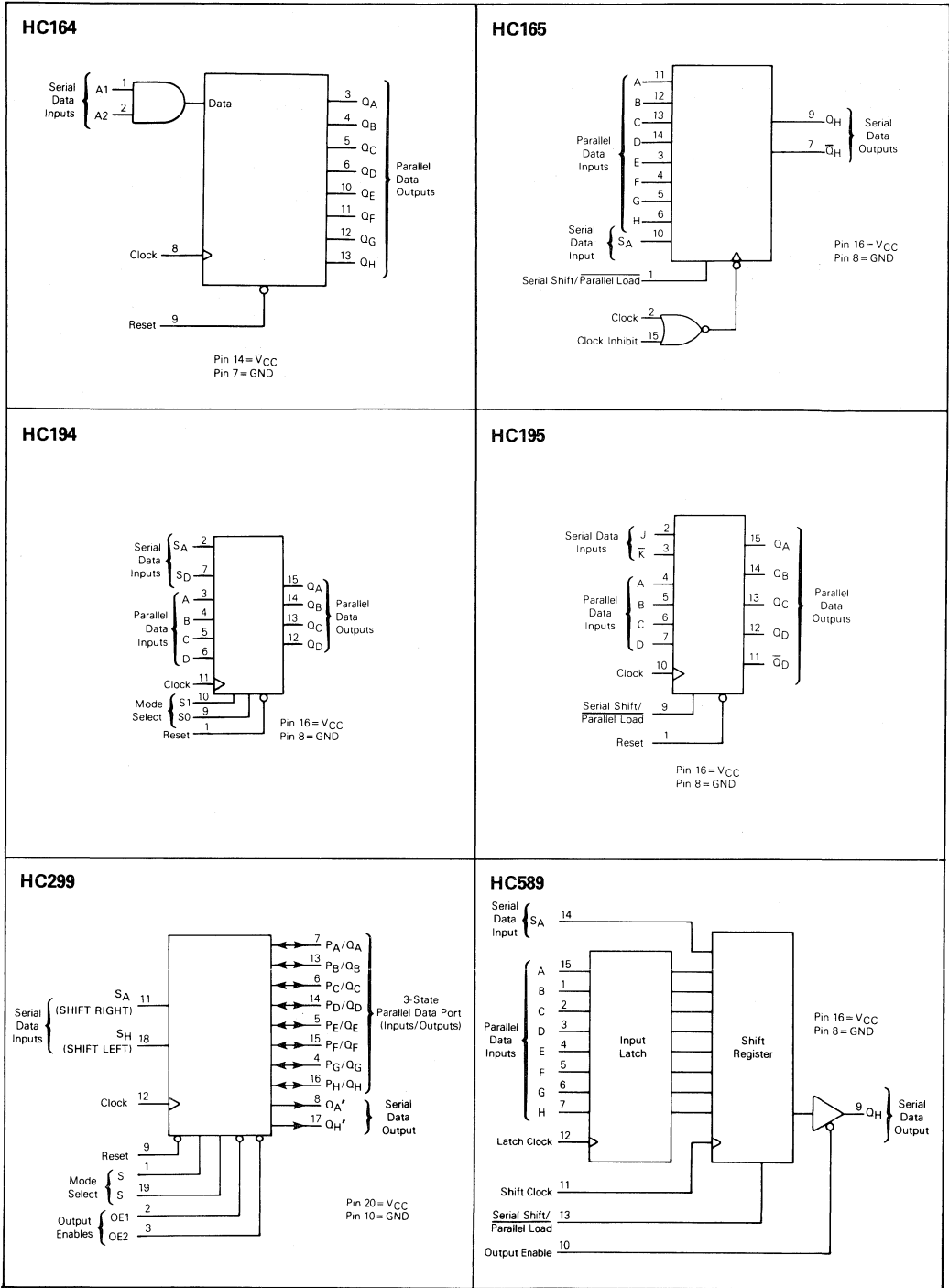
\*Suggested alternative

★Exclusive High-Speed CMOS design

HC Devices Have CMOS-Compatible Inputs.

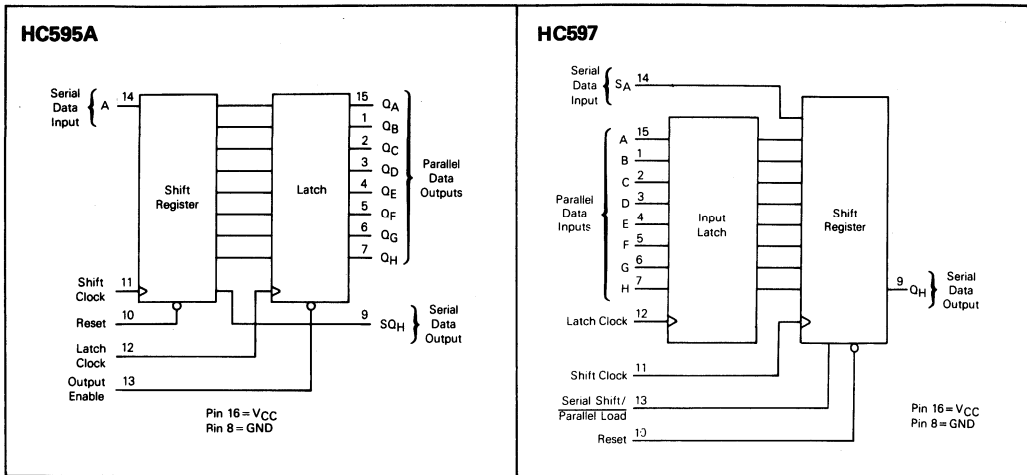
Device	HC 164	HC 165	HC 194	HC 195	HC 299	HC 589	HC 595A	HC 597
# Pins	14	16	16	16	20	16	16	16
4-Bit Register	•	•	•	•	•	•	•	•
8-Bit Register	•	•	•	•	•	•	•	•
Serial Data Input	•	•	•	•	••	•	•	•
Parallel Data Inputs	•	•	•	•	•	•	•	•
Serial Output Only	•	•	•	•	•	•	•	•
Parallel Outputs	•	•	•	•	•	•	•	•
Inverting Output	•	•	•	•	•	•	•	•
Noninverting Output	•	•	•	•	•	•	•	•
Serial Shift/Parallel Load Control	•	•	•	•	•	•	•	•
Shifts One Direction Only	•	•	•	•	•	•	•	•
Shifts Both Directions	•	•	•	•	•	•	•	•
Positive-Transition Clocking	•	•	•	•	•	•	•	•
Active-High Clock Enable	•	•	•	•	•	•	•	•
Input Data Enable	•							
Data Latch with Active-High Latch Clock						•		•
Output Latch with Active-High Latch Clock							•	
3-State Outputs					•	•	•	
Active-Low Output Enable					••	•	•	
Active-Low Reset	•		•	•	•		•	•

# SHIFT REGISTERS (Continued)



# SHIFT REGISTERS (Continued)

2



# COUNTERS

2

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC160 HC161A	Presetable BCD Counter with Asynchronous Reset Presetable 4-Bit Binary Counter with Asynchronous Reset	LS160,LS160A LS161,LS161A	4160 4161	LS/CMOS LS/CMOS	16 16
HC162 HC163A HC390	Presetable BCD Counter with Synchronous Reset Presetable 4-Bit Binary Counter with Synchronous Reset Dual 4-Stage Binary Ripple Counter with ÷ 2 and ÷ 5 Sections	LS162,LS162A LS163,LS163A LS390	4162 4163	LS/CMOS LS/CMOS LS	16 16 16
HC393 HC4017 HC4020 HC4024 HC4040	Dual 4-Stage Binary Ripple Counter Decade Counter 14-Stage Binary Ripple Counter 7-Stage Binary Ripple Counter 12-Stage Binary Ripple Counter	LS393	*4520 4017 4020 4024 4040	LS CMOS CMOS CMOS CMOS	14 16 16 14 16
HC4060	14-Stage Binary Ripple Counter with Oscillator		4060	CMOS	16

\*Suggested alternative

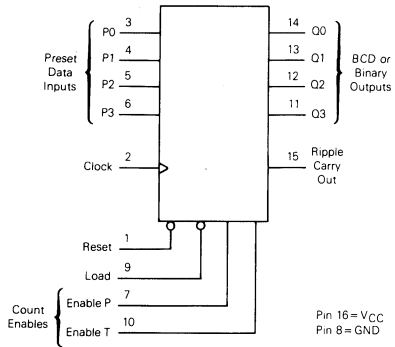
HC Devices Have CMOS-Compatible Inputs.

Device	HC 160	HC 161A	HC 162	HC 163A	HC 390	HC 393	HC 4017	HC 4020	HC 4024	HC 4040	HC 4060
# Pins	16	16	16	16	16	14	16	16	14	16	16
Single Device	•	•	•	•	•	•	•	•	•	•	•
Dual Device											
Ripple Counter					•	•		•	•	•	•
Number of Ripple Counter Internal Stages					4	4		14	7	12	14
Number of Stages with Available Outputs					4	4		12	7	12	10
Count Up	•	•	•	•	•	•	•	•	•	•	•
4-Bit Binary Counter		•		•		•					
BCD Counter	•		•		•						
Decimal Counter							•				
Separate ÷ 2 Section					•						
Separate ÷ 5 Section					•						
On-Chip Oscillator Capability											•
Positive-Transition Clocking	•	•	•	•			•				
Negative-Transition Clocking					•	•	•	•	•	•	•
Active-High Clock Enable							•				
Active-Low Clock Enable							•				
Active-High Count Enable	••	••	••	••							
Active-High Reset	•	•	•	•	•	•	•	•	•	•	•
4-Bit Binary Preset Data Inputs		•		•							
BCD Preset Data Inputs	•		•								
Active-Low Load Preset	•	•	•	•							
Carry Output	•	•	•	•							

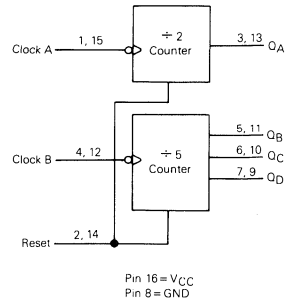
••implies the device has two such enables

# COUNTERS (Continued)

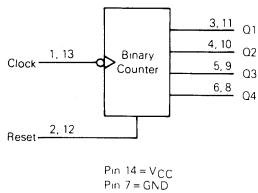
**HC160 HC162**  
**HC161A HC163A**



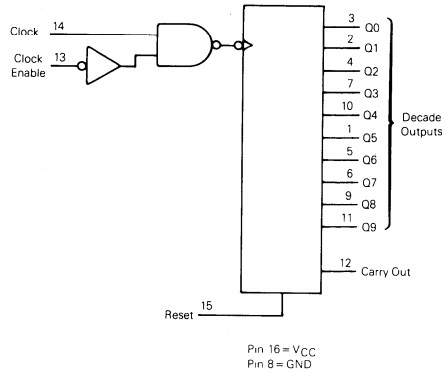
**HC390**



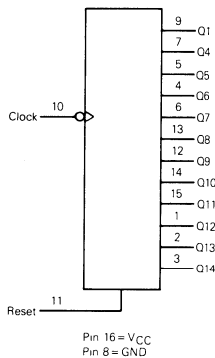
**HC393**



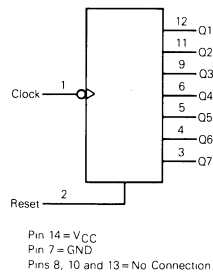
**HC4017**



**HC4020**

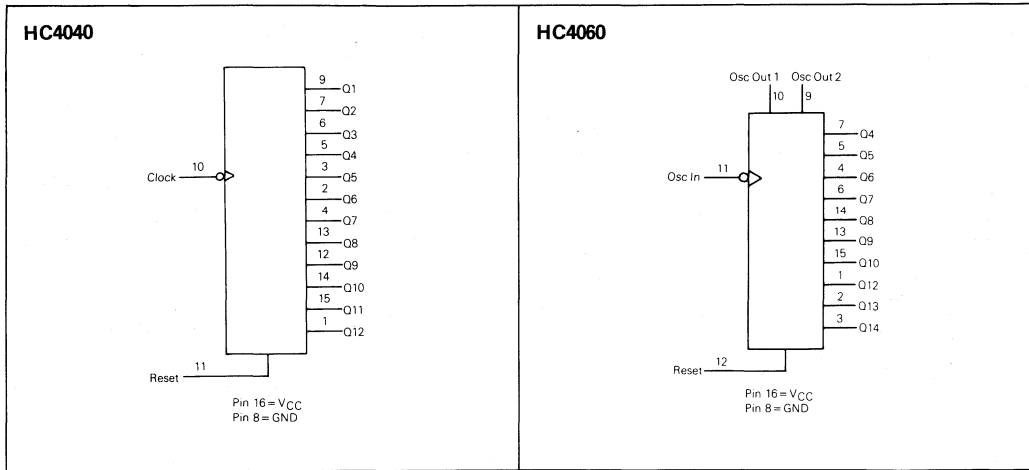


**HC4024**





## COUNTERS (Continued)

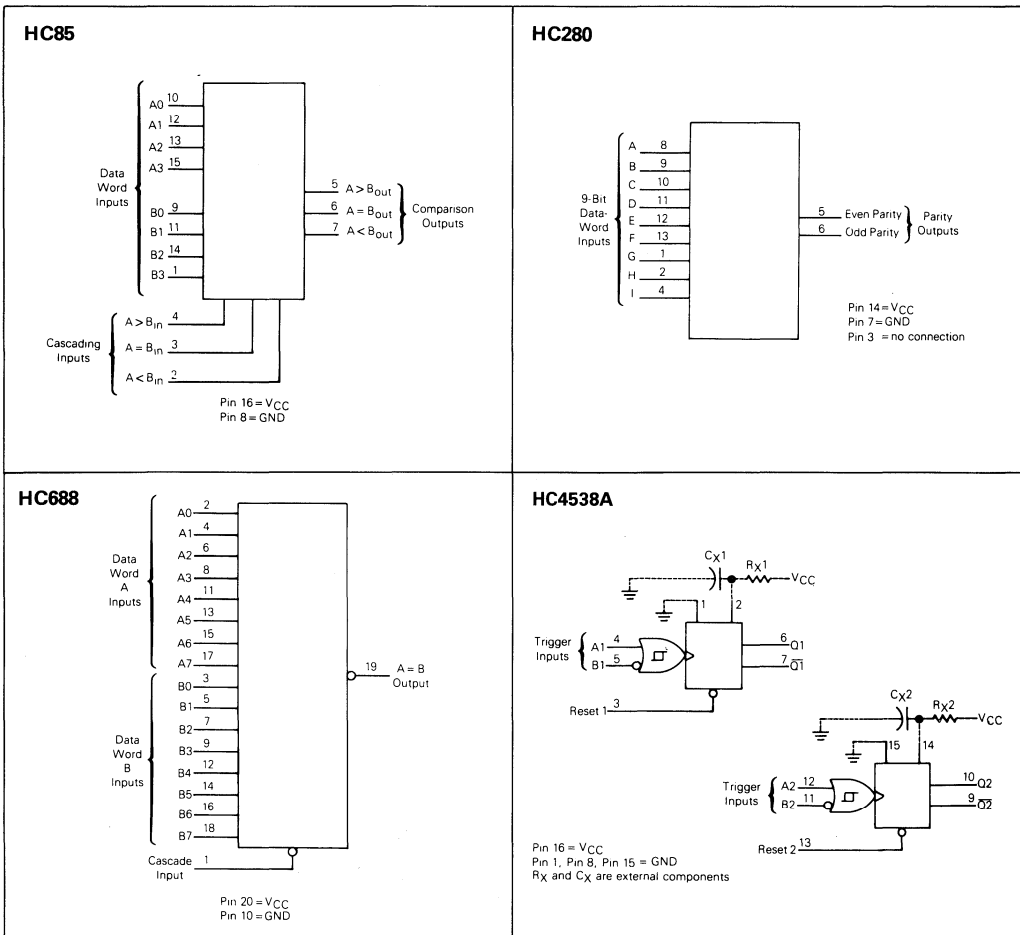


2

# MISCELLANEOUS DEVICES

2

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC85	4-Bit Magnitude Comparator	LS85	*4585	LS	16
HC280	9-Bit Odd/Even Parity Generator/Checker	LS280	*4531	LS	14
HC688	8-Bit Equality Comparator	LS688		LS	20
HC4538A	Dual Precision Monostable Multivibrator (Retriggerable, Resettable)	*LS423	4538,4528	CMOS	16



# Definitions and Glossary of Terms

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## HC vs. HCT

Motorola's High-Speed CMOS is intended to give the designer an alternative to LSTTL. HSCMOS, with the faster speed advantage over metal-gate CMOS (MC14000 series) and the lower power consumption advantage over LSTTL, is an optimum choice for new midrange designs. With the advent of high-speed CMOS microprocessors and memories, the ability to design a 100% CMOS system is now possible.

HCT devices offer a short-term solution to the TTL/NMOS-to-CMOS interface problem. To achieve this interface capability, some CMOS advantages had to be compromised. These compromises include power consumption, operating voltage range, and noise immunity.

In most cases HCT devices are drop-in replacements of TTL devices with significant advantages over the TTL devices. However, in some cases, an equivalent HCT device may not replace a TTL device without some form of circuit modification.

The wise designer uses HCT devices to perform logic level conversions only. In new designs, the designer wants all the advantages of a true CMOS system and designs using only HC devices.

## "A" versus "Non-A"

**"A" Versus "Non-A"** — Motorola has an on-going device performance enhancement program for the Hi-Speed CMOS family. This is indicated by the "A" suffix of the device identification. Some of the characteristics of this "A" enhancement program are improved design, a better quality process, faster performing AC propagation delays and enhancements to various DC characteristics

The old "Non-A" process was a 5 micron process that was modified to run a 3.5 micron family. The new "A" process is a true 3 micron process and gives better process control, with improved performance and quality.

## GLOSSARY OF TERMS

**C<sub>in</sub>** **Input Capacitance** — The parasitic capacitance associated with a given input pin.

**C<sub>L</sub>** **Load Capacitance** — The capacitor value which loads each output during testing and/or evaluation. This capacitance is assumed to be attached to each output in a system. This includes all wiring and stray capacitance.

**C<sub>out</sub>** **Output Capacitance** — The capacitance associated with a three-state output in the high-impedance state.

**C<sub>PD</sub>** **Power Dissipation Capacitance** — Used to determine device dynamic power dissipation, i.e.,  $P_D = C_{PD}V_{CC}^2f + V_{CC}I_{CC}$ . See **POWER SUPPLY SIZING** for a discussion of C<sub>PD</sub>.

**f<sub>max</sub>** **Maximum Clock Frequency** — The maximum clocking frequency attainable with the following input and output conditions being met:

**Input Conditions** — (HC)  $t_r = t_f = 6$  ns, voltage swing from GND to V<sub>CC</sub> with 50% duty cycle. (HCT)  $t_r = t_f = 6$  ns, voltage swing from GND to 3.0 V with 50% duty cycle.

**Output Conditions** — (HC and HCT) waveform must swing from 10% of (V<sub>OH</sub> - V<sub>OL</sub>) to 90% of (V<sub>OH</sub> - V<sub>OL</sub>) and be functionally correct under the given load condition: C<sub>L</sub> = 50 pF, all outputs.

**V<sub>CC</sub>** **Positive Supply Voltage** — +dc supply voltage (referenced to GND). The voltage range over which ICs are functional.

**V<sub>in</sub>** **Input Voltage** — DC input voltage (referenced to GND).

**V<sub>out</sub>** **Output Voltage** — DC output voltage (referenced to GND).

**V<sub>IH</sub>** **Minimum High Level Input Voltage** — The worst case voltage that is recognized by a device as the HIGH state.

**V<sub>IL</sub>** **Maximum Low Level Input Voltage** — The worst case voltage that is recognized by a device as the LOW state.

**V<sub>OH</sub>** **Minimum High Level Output Voltage** — The worst case high-level voltage at an output for a given output current (I<sub>out</sub>) and supply voltage (V<sub>CC</sub>).

**V<sub>OL</sub>** **Maximum Low Level Output Voltage** — The worst case low-level voltage at an output for a given output current (I<sub>out</sub>) and supply voltage (V<sub>CC</sub>).

**V<sub>T+</sub>** **Positive-Going Input Threshold Voltage** — The minimum input voltage of a device with hysteresis which is recognized as a high level. (Assumes ramp up from previous low level.)

**V<sub>T-</sub>** **Negative-Going Input Threshold Voltage** — The maximum input voltage of a device with hysteresis which is recognized as a low level. (Assumes ramp down from previous high level.)

**V<sub>H</sub>** **Hysteresis Voltage** — The difference between V<sub>T+</sub> and V<sub>T-</sub> of a given device with hysteresis. A measure of noise rejection.

**I<sub>CC</sub>** **IC Quiescent Supply Current** — The current into the V<sub>CC</sub> pin when the device inputs are static at V<sub>CC</sub> or GND and outputs are not connected.

**ΔI<sub>CC</sub>** **Additional Quiescent Supply Current** — The current into the V<sub>CC</sub> pin when one of the device inputs is at 2.4 V with respect to GND and the other inputs are static at V<sub>CC</sub> or GND. The outputs are not connected.

**I<sub>in</sub>** **Input Current** — The current into an input pin with the respective input forced to V<sub>CC</sub> or GND. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).

**I<sub>out</sub>** **Output Current** — The current out of an output pin. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).

- I<sub>IH</sub> Input Current (High)** — The input current when the input voltage is forced to a high level.
- I<sub>IL</sub> Input Current (Low)** — The input current when the input voltage is forced to a low level.
- I<sub>OH</sub> Output Current (High)** — The output current when the output voltage is at a high level.
- I<sub>OL</sub> Output Current (Low)** — The output current when the output voltage is at a low level.
- I<sub>OZ</sub> Three-State Leakage Current** — The current into or out of a three-state output in the high-impedance state with that respective output forced to V<sub>CC</sub> or GND.
- t<sub>PLH</sub> Low-to-High Propagation Delay (HC)** — The time interval between the 0.5 V<sub>CC</sub> level of the controlling input waveform and the 50% level of the output waveform, with the output changing from low level to high level. **(HCT)** — The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from low level to high level.
- t<sub>PHL</sub> High-to-Low Propagation Delay (HC)** — The time interval between the 0.5 V<sub>CC</sub> level of the controlling input waveform and the 50% level of the output waveform, with the output changing from high level to low level. **(HCT)** — The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from high level to low level.
- t<sub>PLZ</sub> Low-Level to High-Impedance Propagation Delay (Disable Time)** — The time interval between the 0.5 V<sub>CC</sub> level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 10% level of the output waveform, with the output changing from the low level to high-impedance (off) state.
- t<sub>PHZ</sub> High-Level to High-Impedance Propagation Delay (Disable Time)** — The time interval between the 0.5 V<sub>CC</sub> level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 90% level of the output waveform, with the output changing from the high level to high-impedance (off) state.
- t<sub>PZL</sub> High-Impedance to Low-Level Propagation Delay (Enable Time)** — The time interval between 0.5 V<sub>CC</sub> level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.
- t<sub>PZH</sub> High-Impedance to High-Level Propagation Delay (Enable Time)** — The time interval between the 0.5 V<sub>CC</sub> level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a high level.
- t<sub>TLH</sub> Output Low-to-High Transition Time** — The time interval between the 10% and 90% voltage levels of the rising edge of a switching output.
- t<sub>THL</sub> Output High-to-Low Transition Time** — The time interval between the 90% and 10% voltage levels of the falling edge of a switching output.
- t<sub>su</sub> Setup Time** — The time interval immediately preceding the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative setup time indicates that the data at the input may be applied sometime after the active clock or latch transition and still be recognized. For HC devices, the setup time is measured from the 50% level of the data waveform to the 50% level of the clock or latch input waveform. For HCT devices, the setup time is measured from the 1.3 V level (with respect to GND) of the data waveform to the 1.3 V level (with respect to GND) of the clock or latch input waveform.
- t<sub>h</sub> Hold Time** — The time interval immediately following the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative hold time indicates that the data at the input may be changed prior to the active clock or latch transition and still be recognized. For HC devices, the hold time is measured from the 50% level of the clock or latch input waveform to the 50% level of the data waveform. For HCT devices, the hold time is measured from the 1.3 V level (with respect to GND) of the clock or latch input waveform to the 1.3 V level (with respect to GND) of the data waveform.
- t<sub>rec</sub> Recovery Time (HC)** — The time interval between the 50% level of the transition from active to inactive state of an asynchronous control input and the 50% level of the active clock or latch enable edge required to guarantee proper operation of a device. **(HCT)** — The time interval between the 1.3 V level (with respect to GND) of the transition from active to inactive state of an asynchronous control input and the 1.3 V level (with respect to GND) of the active clock or latch edge required to guarantee proper operation of a logic device.
- t<sub>w</sub> Pulse Width (HC)** — The time interval between 50% levels of an input pulse required to guarantee proper operation of a logic device. **(HCT)** — The time interval between 1.3 V levels (with respect to GND) of an input pulse required to guarantee proper operation of a logic device.
- t<sub>r</sub> Input Rise Time (HC)** — The time interval between the 10% and 90% voltage levels on the rising edge of an input signal. **(HCT)** — The time interval between the 0.3 V level and 2.7 V level (with respect to GND) on the rising edge of an input signal.
- t<sub>f</sub> Input Fall Time (HC)** — The time interval between the 90% and 10% voltage levels on the falling edge of an input signal. **(HCT)** — The time interval between the 2.7 V level and 0.3 V level (with respect to GND) on the falling edge of an input signal.

# Design Considerations

4

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## INTRODUCTION

CMOS devices have been used for many years in applications where the primary concerns were low power consumption, wide power-supply range, and high noise immunity. However, metal-gate CMOS (MC14000 series) is too slow for many applications. Applications requiring high-speed devices, such as microprocessor memory decoding, had to go to the faster families such as LSTTL. This meant sacrificing the best qualities of CMOS. The next step in the logic evolution was to introduce a family of devices that were fast enough for such applications, while retaining the advantages of CMOS. The results of this change can be seen in Table 1 where HSCMOS devices are compared to standard (metal-gate) CMOS, LSTTL, and ALS.

The Motorola CMOS evolutionary process shown in Figure 1 indicates that one advantage of the silicon-gate process is device size. The High-Speed CMOS (HSCMOS) device is about half the size of the metal-gate predecessor, yielding significant chip area savings. The silicon-gate process allows smaller gate or channel lengths due to the self-aligning gate feature. This process uses the gate to define the channel during processing, eliminating registration errors and, therefore, the need for gate overlaps. The elimination of the gate overlap significantly lowers the gate capacitance, resulting in higher speed capability. The smaller gate length also results in higher drive capability per unit gate width, ensuring more efficient use of chip area. Immunity enhancements to electrostatic discharge (ESD) damage and latch up are ongoing. Precautions should still be taken, however, to guard against electrostatic discharge and latch up.

Motorola's High-Speed CMOS family has a broad range of functions from basic gates, flip-flops, and counters to bus-compatible devices. The family is made up of devices that are identical in pinout and are functionally equivalent to LSTTL devices, as well as the most popular metal-gate devices not available in TTL. Thus, the designer has an excellent alternative to existing families without having to become familiar with a new set of device numbers.

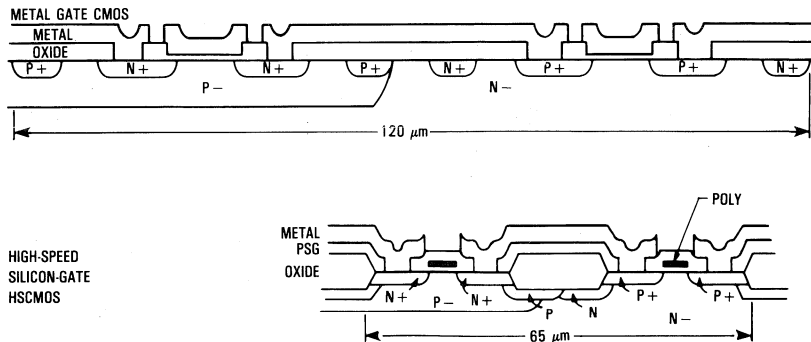


Figure 1. CMOS Evolution

## HANDLING PRECAUTIONS

High-Speed CMOS devices, like all MOS devices, have an insulated gate that is subject to voltage breakdown. The gate oxide for HSCMOS devices breaks down at a gate-source potential of about 100 volts. All device inputs are protected by a resistor-diode network (Figure 2). Using the test setup shown in Figure 3, the inputs typically withstand a >2 kV discharge.

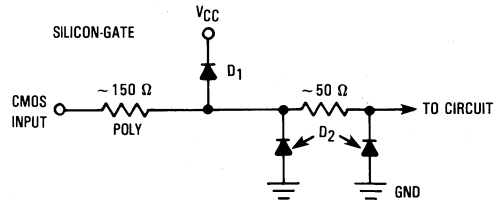


Figure 2. Input Protection Network

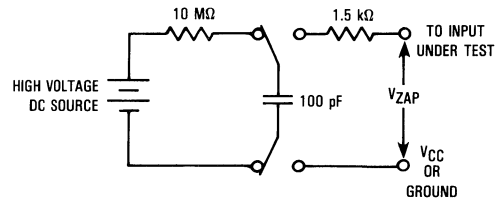


Figure 3. Electrostatic Discharge Test Circuit

Table 1. Logic Family Comparisons

General Characteristics (1) (All Maximum Ratings)

Characteristic	Symbol	TTL		CMOS		Unit
		LS	ALS	MC14000	Hi-Speed	
Operating Voltage Range	V <sub>CC/EE/DD</sub>	5±5%	5±5%	3.0 to 18	2.0 to 6.0	V
Operating Temperature Range	T <sub>A</sub>	0 to +70	0 to +70	-40 to +85	-55 to +125	°C
Input Voltage (limits)	V <sub>IH</sub> min	2.0	2.0	3.5 <sup>4</sup>	3.5 <sup>4</sup>	V
	V <sub>IL</sub> max	0.8	0.8	1.5 <sup>4</sup>	1.0 <sup>4</sup>	V
Output Voltage (limits)	V <sub>OH</sub> min	2.7	2.7	V <sub>DD</sub> -0.05	V <sub>CC</sub> -0.1	V
	V <sub>OL</sub> max	0.5	0.5	0.05	0.1	V
Input Current	I <sub>INH</sub>	20	20	±0.3	±1.0	μA
	I <sub>INL</sub>	-400	-200			
Output Current @ V <sub>O</sub> (limit) unless otherwise specified	I <sub>OH</sub>	-0.4	-0.4	-2.1 @ 2.5 V	-4.0 @ V <sub>CC</sub> -0.8 V	mA
	I <sub>OL</sub>	8.0	8.0	0.44 @ 0.4 V	4.0 @ 0.4 V	mA
DC Noise Margin Low/High	DCM	0.3/0.7	0.3/0.7	1.45 <sup>4</sup>	0.90/1.35 <sup>4</sup>	V
DC Fanout	—	20	20	>50(1) <sup>2</sup>	50(10) <sup>2</sup>	—

Speed/Power Characteristics (1) (All Typical Ratings)

Characteristic	Symbol	TTL		CMOS		Unit
		LS	ALS	MC14000	Hi-Speed	
Quiescent Supply Current/Gate	I <sub>G</sub>	0.4	0.2	0.0001	0.0005	mA
Power/Gate (Quiescent)	P <sub>G</sub>	2.0	1.0	0.0006	0.001	mW
Propagation Delay	t <sub>p</sub>	9.0	7.0	125	8.0	ns
Speed Power Product	—	18	7.0	0.075	0.01	pJ
Clock Frequency (D-F/F)	f <sub>max</sub>	33	35	4.0	40	MHz
Clock Frequency (Counter)	f <sub>max</sub>	40	45	5.0	40	MHz

Propagation Delay (1)

Characteristic		TTL		CMOS		Unit
		LS	ALS	MC14000	Hi-Speed	
<b>Gate, NOR or NAND:</b>	Product No.	SN74LS00	SN74ALS00	MC14001B	74HC00	—
t <sub>PLH</sub> /t <sub>PHL</sub> <sup>(5)</sup>	Typical	(10) <sup>3</sup>	(5) <sup>3</sup>	25	(8) <sup>3</sup> 10	ns
	Maximum	(15) <sup>3</sup>	10	250	(15) <sup>3</sup> 20	
<b>Flip-Flop, D-type:</b>	Product No.	SN74LS74	SN74ALS74	MC14013B	74HC74	—
t <sub>PLH</sub> /t <sub>PHL</sub> <sup>(5)</sup> (Clock to Q)	Typical	(25) <sup>3</sup>	(12) <sup>3</sup>	175	(23) <sup>2</sup> 25	ns
	Maximum	(40) <sup>3</sup>	20	350	(30) <sup>3</sup> 32	
<b>Counter:</b>	Product No.	SN74LS163	SN74ALS163	MC14163B	74HC163	—
t <sub>PLH</sub> /t <sub>PHL</sub> <sup>(5)</sup> (Clock to Q)	Typical	(18) <sup>3</sup>	(10) <sup>3</sup>	350	(20) <sup>3</sup> 22	ns
	Maximum	(27) <sup>3</sup>	24	700	(27) <sup>3</sup> 29	

NOTES:

- Specifications are shown for the following conditions:
  - V<sub>DD</sub> (CMOS) = 5.0 V ± 10% for dc tests, 5.0 V for ac tests; V<sub>CC</sub> (TTL) = 5.0 V ± 5% for dc tests, 5.0 V for ac tests
  - Basic Gates: LS00 or equivalent
  - T<sub>A</sub> = 25°C
  - C<sub>L</sub> = 50 pF (ALS, HC), 15 pF (LS, 14000 and Hi-Speed)
  - Commercial grade product
- ( ) fanout to LSTTL
- ( ) C<sub>L</sub> = 15 pF
- DC input voltage specifications are proportional to supply voltage over operating range.
- The number specified is the larger of t<sub>PLH</sub> and t<sub>PHL</sub> for each device.

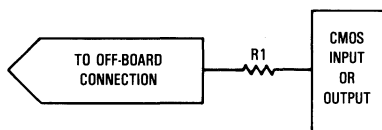
The input protection network uses a polysilicon resistor in series with the input and before the protection diodes. This series resistor slows down the slew rate of static discharge spikes to allow the protection diodes time to turn on. Outputs have a similar ESD protection network except for the series resistor. Although the on-chip protection circuitry guards against ESD damage, additional protection may be necessary once the chip is placed in circuit. Both an external series resistor and ground and  $V_{CC}$  diodes, similar to the input protection structure, are recommended if there is a potential of ESD, voltage transients, etc. Several monolithic diode arrays are available from Motorola, such as the MAD130 (dual 10 diode array) or the MAD1104 (dual 8 diode array). These diodes, in chip form, not only provide the necessary protection, but also save board space as opposed to using discrete diodes.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged pins are the easiest to detect. An ESD-damaged pin that has been completely destroyed may exhibit a low-impedance path to  $V_{CC}$  or GND. Another common failure mode is a fused or open circuit. The effect of both failure modes is that the device no longer properly responds to input signals. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Generally, another effect of static damage is increased chip leakage currents ( $I_{CC}$ ).

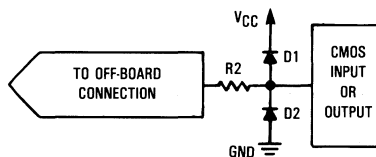
Although the input network does offer significant protection, these devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4 to 15 kV range (depending

on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

1. Wrist straps and equipment logs should be maintained and audited on a regular basis. Wrist straps malfunction and may go unnoticed. Also, equipment gets moved from time to time and grounds may not be reconnected properly.
2. Do not exceed the Maximum Ratings specified by the data sheet.
3. All unused device inputs should be connected to  $V_{CC}$  or GND.
4. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
5. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connectors to a PC board are connected to an input or output of a CMOS device, a resistor should be used in series with the input or output. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. The delay is caused by the time constant formed by the series resistor and input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 4, two possible networks are shown using a series resistor to reduce ESD damage. For convenience, an equation is given for added propagation delay and rise time effects due to series resistance size.



- Advantage: Requires minimal board area
- Disadvantage:  $R1 > R2$  for the same level of protection; therefore, rise and fall times, propagation delays, and output drives are severely affected.



- Advantage:  $R2 < R1$  for the same level of protection. Impact on ac and dc characteristics is minimized.
- Disadvantage: More board area, higher initial cost.

NOTE: These networks are useful for protecting the following:

- |                              |                           |
|------------------------------|---------------------------|
| A digital inputs and outputs | C 3-state outputs         |
| B analog inputs and outputs  | D bidirectional I/O ports |

#### Propagation Delay and Rise Time vs. Series Resistance

$$R \approx \frac{t}{C \cdot k}$$

where:

- R = the maximum allowable series resistance in ohms
- t = the maximum tolerable propagation delay or rise time in seconds
- C = the board capacitance plus the driven device's input capacitance in farads
- k = 0.7 for propagation delay calculations
- k = 2.3 for rise time calculations

Figure 4. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility

6. All CMOS devices should be stored or transported in materials that are antistatic or conductive. CMOS devices must not be inserted into conventional plastic "snow", styrofoam, or plastic trays, but should be left in their original container until ready for use.
7. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, because a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are essential and should be tested daily. See Figure 5 for an example of a typical work station.
8. Nylon or other static generating materials should not come in contact with CMOS devices.
9. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static buildup by using ionized air blowers, anti-static sprays, and room humidifiers. All conductive parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to earth ground.
10. Cold chambers using CO<sub>2</sub> for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
11. When lead straightening or hand soldering is necessary, provide ground straps for the apparatus used and be sure that soldering iron tips are grounded.
12. The following steps should be observed during wave solder operations:
  - a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to earth ground.
  - b. The loading and unloading work benches should have conductive tops grounded to earth ground.
  - c. Operators must comply with precautions previously explained.
  - d. Completed assemblies should be placed in antistatic or conductive containers prior to being moved to subsequent stations.
13. The following steps should be observed during board-cleaning operations:
  - a. Vapor degreasers and baskets must be grounded to earth ground.
  - b. Brush or spray cleaning should not be used.
  - c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic or conductive container.
  - d. Cleaned assemblies should be placed in antistatic or conductive containers immediately after removal from the cleaning basket.
  - e. High velocity air movement or application of solvents and coatings should be employed only when a static eliminator using ionized air is directed at the printed circuit board.
14. The use of static detection meters for production line surveillance is highly recommended.
15. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
16. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
17. Double check test equipment setup for proper polarity of V<sub>CC</sub> and GND before conducting parametric or functional testing.
18. Do not recycle shipping rails. Repeated use causes deterioration of their antistatic coating. Exception: carbon rails (black color) may be recycled to some extent. This type of rail is conductive and antistatic.

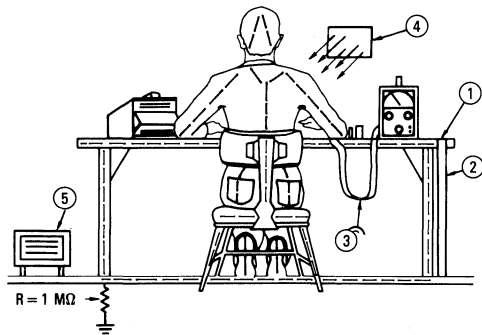
**RECOMMENDED READING**

"Total Control of the Static in Your Business"

Available by writing to:  
 3M Company  
 Static Control Systems  
 P.O. Box 2963  
 Austin, Texas 78769-2963

Or by calling:  
 1-800-328-1368

S. Cherniak, "A Review of Transients and Their Means of Suppression", Application Note-843, Motorola Semiconductor Products Inc., 1982.



**NOTES:**

1. 1/16 inch conductive sheet stock covering bench-top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside a building to be less than outside humidity.

Figure 5. Typical Manufacturing Work Station

## POWER SUPPLY SIZING

CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive power supplies without cooling fans. In addition, batteries may be used as either a primary power source or as a backup.

The maximum recommended power supply voltage for HC devices is 6.0 V and 5.5 V for HCT devices. Figure 6 offers some insight as to how this specification was derived. In the figure,  $V_S$  is the maximum power supply voltage and  $I_S$  is the sustaining current for the latch-up mode. The value of  $V_S$  was chosen so that the secondary breakdown effect may be avoided. The low-current junction avalanche region is between 10 and 14 volts at  $T_A = 25^\circ\text{C}$ .

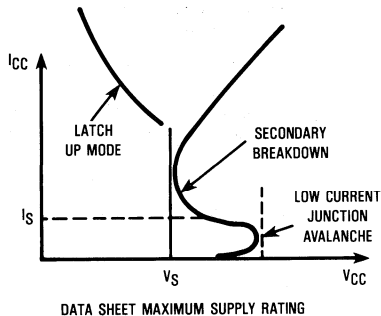


Figure 6. Secondary Breakdown Characteristics

In an ideal system design, the power supply should be designed to deliver only enough current to ensure proper operation of all devices. The obvious benefit of this type of design is cost savings.

## BATTERY SYSTEMS

HSCMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery-operated systems.

1. The recommended power supply voltages should be observed. For battery backup systems such as the one in Figure 7, the battery voltage must be at least 2.7 volts (2 volts for the minimum power supply voltage and 0.7 volts to account for the voltage drop across the series diode).
2. Inputs that might go above the battery backup voltage should use the HC4049 or HC4050 buffers (Figure 8). If line power is interrupted, CMOS System A and Buffer A lose power. However, CMOS System B and Buffer B remain active due to the battery backup. Buffer A protects System A from System B by blocking active inputs while the circuit is not powered up. Also, if the power supply voltage drops below the battery voltage, Buffer A acts as a level translator for the outputs from System B. Buffer B acts to protect System B from any overvoltages which might exist. Both buffers may be replaced with current-limiting resistors, however power consumption is increased and propagation delays are lengthened.
3. Outputs that are subject to voltage levels above  $V_{CC}$  or below GND should be protected with a series resistor and/or clamping diodes to limit the current to an acceptable level.

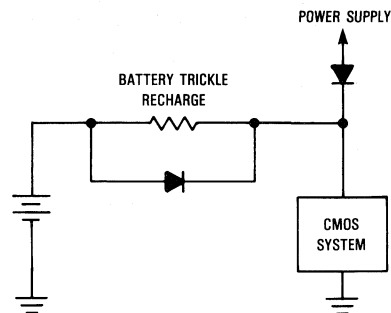


Figure 7. Battery Backup System

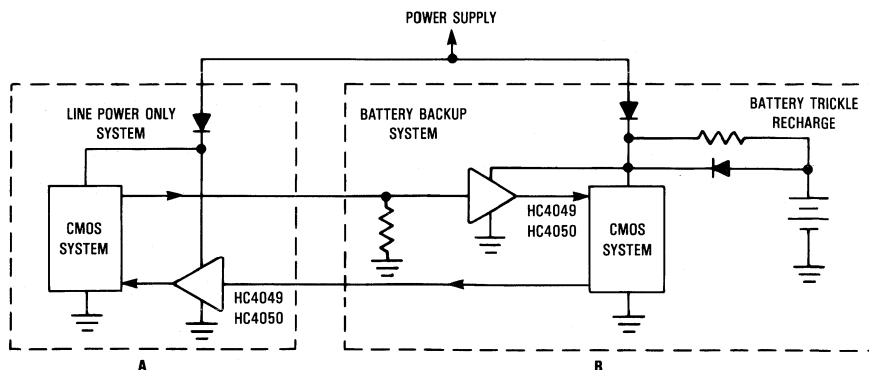


Figure 8. Battery Backup Interface

## CPD POWER CALCULATION

Power consumption for HSCMOS is dependent on the power-supply voltage, frequency of operation, internal capacitance, and load. The power consumption may be calculated for each package by summing the quiescent power consumption,  $I_{CC} \cdot V_{CC}$ , and the switching power required by each device within the package. For large systems, the most timely method is to bread-board the circuit and measure the current required under a variety of conditions.

The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD}) V_{CC}^2 f$$

where:  $P_D$  = power dissipated in  $\mu W$   
 $C_L$  = total load capacitance present at the output in pF  
 $C_{PD}$  = a measure of internal capacitances, called power dissipation capacitance, given in pF  
 $V_{CC}$  = supply voltage in volts  
 $f$  = frequency in MHz

If the devices are tested at a sufficiently high frequency, the dc supply current contributes a negligible amount to the overall power consumption and can therefore be ignored. For this reason, the power consumption is measured at 1 MHz and the following formula is used to determine the device's  $C_{PD}$  value:

$$C_{PD} = \frac{I_{CC} \text{ (dynamic)}}{V_{CC} \cdot f} - C_L$$

The resulting power dissipation is calculated using  $C_{PD}$  as follows under no-load conditions.

$$(HC) \quad P_D = C_{PD} V_{CC}^2 f + V_{CC} I_{CC}$$

$$(HCT) \quad P_D = C_{PD} V_{CC}^2 f + V_{CC} I_{CC} + \Delta I_{CC} V_{CC} \\ (\delta_1 + \delta_2 + \dots + \delta_n)$$

where the previously undefined variable,  $\delta_n$  is the duty cycle of each input applied at TTL/NMOS levels.

The power dissipation for analog switches switching digital signals is the following:

$$(HC) \quad P_D = C_{PD} V_{CC}^2 f_{in} + (C_S + C_L) V_{CC}^2 f_{out} + V_{CC} I_{CC}$$

where:  $C_S$  = digital switch capacitance, and  
 $f_{out}$  = output frequency

In order to determine the  $C_{PD}$  of a single section of a device (i.e., one of four gates, or one of two flip-flops in a package), Motorola uses the following procedures as defined by JEDEC. Note: "biased" as used below means "tied to  $V_{CC}$  or GND."

**Gates:** Switch one input while the remaining input(s) are biased so that the output(s) switch.  
**Latches:** Switch the enable and data inputs such that the latch toggles.  
**Flip-Flops:** Switch the clock pin while changing the data pin(s) such that the output(s) change with each clock cycle.

**Decoders/ Demultiplexers:** Switch one address pin which changes two outputs.  
**Data Selectors/ Multiplexers:** Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.  
**Analog Switches:** Switch one address/select pin which changes two switches. The switch inputs/outputs should be left open. For digital applications where the switch inputs/outputs change between  $V_{CC}$  and GND, the respective switch capacitance should be added to the load capacitance.  
**Counters:** Switch the clock pin with the other inputs biased so that the device counts.  
**Shift Registers:** Switch the clock while alternating the input so that the device shifts alternating 1s and 0s through the register.  
**Transceivers:** Switch only one data input. Place transceivers in a single direction.  
**Monostables:** The pulse obtained with a resistor and no external capacitor is repeatedly switched.  
**Parity Generators:** Switch one input.  
**Encoders:** Switch the lowest priority output.  
**Display Drivers:** Switch one input so that approximately one-half of the outputs change state.  
**ALUs/Adders:** Switch the least significant bit. The remaining inputs are biased so that the device is alternately adding 0000 (binary) or 0001 (binary) to 1111 (binary).

On HSCMOS data sheets,  $C_{PD}$  is a typical value and is given either for the package or for the individual device (i.e., gates, flip-flops, etc.) within the package. An example of calculating the package power requirement is given using the 74HC00, as shown in Figure 9.

From the data sheet:

$$I_{CC} = 2 \mu A \text{ at room temperature (per package)}$$

$$C_{PD} = 22 \text{ pF per gate}$$

$$P_D = (C_{PD} + C_L) V_{CC}^2 f + V_{CC} I_{CC}$$

$$P_{D1} = (22 \text{ pF} + 50 \text{ pF})(5 \text{ V})^2(1 \text{ kHz}) = 1.8 \mu W$$

$$P_{D2} = (22 \text{ pF} + 50 \text{ pF})(5 \text{ V})^2(1 \text{ MHz}) = 1800 \mu W$$

$$P_{D3} = (22 \text{ pF})(5 \text{ V})^2(0 \text{ Hz}) = 0 \mu W$$

$$P_{D4} = (22 \text{ pF})(5 \text{ V})^2(0 \text{ Hz}) = 0 \mu W$$

$$P_D(\text{total}) = V_{CC} I_{CC} + P_{D1} + P_{D2} + P_{D3} + P_{D4}$$

$$= 10 \mu W + 1.8 \mu W + 1800 \mu W + 0 \mu W$$

$$= 1812 \mu W$$

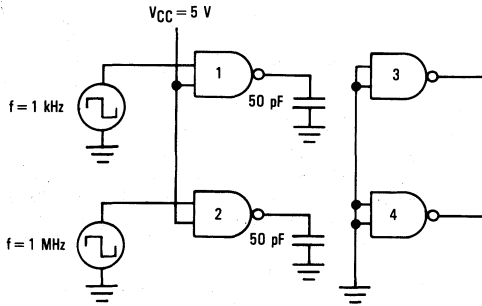


Figure 9. Power Consumption Calculation Example

As seen by this example, the power dissipated by CMOS devices is dependent on frequency. When operating at very high frequencies, HSCMOS devices can consume as much power as LSTTL devices, as shown in Figure 10. The power savings of HSCMOS is realized when used in a system where only a few of the devices are actually switching at the system frequency. The power consumption savings comes from the fact that for CMOS, only the devices that are switching consume significant power.

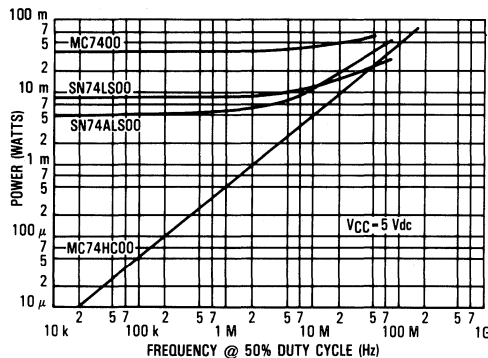


Figure 10. Power Consumption vs. Input Frequency for TTL, LSTTL, ALS, and HSCMOS

## INPUTS

A basic knowledge of input and output structures is essential to the HSCMOS designer. This section deals with the various input characteristics and application rules regarding their use. Output characteristics are discussed in the section titled **Outputs**.

All standard HC, HCU and HCT inputs, while in the recommended operating range ( $GND \leq V_{in} \leq V_{CC}$ ), can be modeled as shown in Figure 11. For input voltages in this range, diodes D1 and D2 are modeled as resistors representing the high-impedance of reverse biased diodes. The maximum input current is  $1 \mu A$ , worst case over temperature, when the inputs are at  $V_{CC}$  or  $GND$ , and  $V_{CC} = 6 V$ .

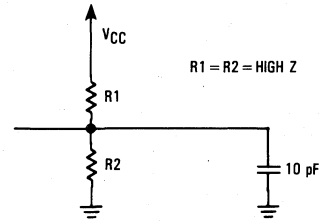


Figure 11. Input Model for  $GND \leq V_{in} \leq V_{CC}$

When CMOS inputs are left open-circuited, the inputs may be biased at or near the typical CMOS switchpoint of  $0.45 V_{CC}$  for HC devices or  $1.3 V$  for HCT devices. At this switchpoint, both the P-channel and the N-channel transistors are conducting, causing excess current drain. Due to the high gain of the buffered devices (see Figure 12), the device can go into oscillation from any noise in the system, resulting in even higher current drain.

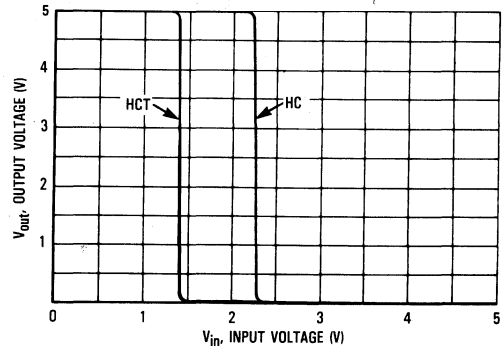


Figure 12. Typical Transfer Characteristics for Buffered Devices

For these reasons, all unused HC/HCT inputs should be connected either to  $V_{CC}$  or  $GND$ . For applications with inputs going to edge connectors, a  $100 k\Omega$  resistor to  $GND$  should be used, as well as a series resistor ( $R_S$ ) for static protection and current limiting (see **Handling Precautions**, this chapter, for series resistor consideration). The resistors should be configured as in Figure 13.

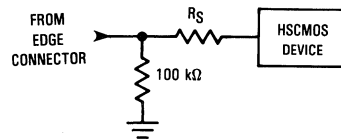


Figure 13. External Protection

For inputs outside of the recommended operating range, the CMOS input is modeled as in Figure 14. The enhanced resistor-diode protection network allows the user greater freedom when designing a worst case system.

Current flows through diode D1 or D2 whenever the input voltage exceeds  $V_{CC}$  or drops below GND enough to forward bias either D1 or D2. The device inputs are guaranteed to withstand from GND  $-1.5$  V to  $V_{CC} + 1.5$  V and a maximum current of 20 mA. If this maximum rating is exceeded, the device could go into a latch-up condition. (See **CMOS Latch Up**, this chapter.) Voltage should never be applied to any input or output pin before power has been applied to the device's power pins. Bias on input or output pins should be removed before removing the power. However, if the input current is limited to less than 20 mA, and this current only lasts for a brief period of time ( $<100$  ms), no damage to the device occurs.

Another specification that should be noted is the maximum input rise ( $t_r$ ) and fall ( $t_f$ ) times. Figure 15 shows the results of exceeding the maximum rise and fall times recommended by Motorola or contained in JEDEC Standard No. 7A. The reason for the oscillation on the output is that as the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input line is amplified, and is passed through to the output. This oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed the maximum specified rise or fall times, Schmitt-triggered devices such as Motorola's HC14 and HC132 are recommended.

#### OUTPUTS

All HSCMOS outputs, with the exception of the HCU04, are buffered to ensure consistent output voltage and current specifications across the family. All buffered outputs

have guaranteed output voltages of  $V_{OL} = 0.1$  V and  $V_{OH} = V_{CC} - 0.1$  V for  $|I_{out}| \leq 20$   $\mu$ A ( $\leq 20$  HSCMOS loads). The output drives for standard drive devices are such that 54HC/HCT and 74HC/HCT devices can drive ten LSTTL loads and maintain a  $V_{OL} \leq 0.4$  V and  $V_{OH} \geq V_{CC} - 0.8$  V across the full temperature range; bus-driver devices can drive fifteen LSTTL loads under the same conditions.

The outputs of all HSCMOS devices are limited to externally forced output voltages of  $-0.5 \leq V_{out} \leq V_{CC} + 0.5$  V. For externally forced voltages outside this range a latch up condition could be triggered. (See **CMOS Latch Up**, this chapter.)

The maximum rated output current given on the individual data sheets is 25 mA for standard outputs and 35 mA for bus drivers. The output short circuit currents of these devices typically exceed these limits. The outputs can, however, be shorted for short periods of time for logic testing, if the maximum package power dissipation is not violated. (See individual data sheets for maximum power dissipation ratings.)

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), devices within the same package may be paralleled. Paralleling devices in different packages may result in devices switching at different points on the input voltage waveform, creating output short circuits and yielding undesirable output voltage waveforms.

As a design aid, output characteristic curves are given for both P-channel source and N-channel sink currents. The curves given include expected minimum curves for  $T_A = 25^\circ\text{C}$ ,  $85^\circ$ , and  $125^\circ\text{C}$ , as well as typical values for  $T_A = 25^\circ\text{C}$ . For temperatures  $<25^\circ\text{C}$ , use the  $25^\circ\text{C}$  curves. These curves, Figures 16 through 27, are intended as design aids, not as guarantees. Unused output pins should be open-circuited (floating).

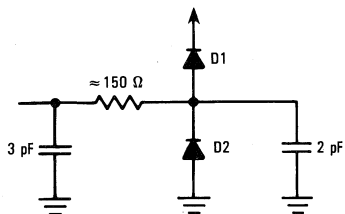


Figure 14. Input Model for  $V_{in} > V_{CC}$  or  $V_{in} < GND$

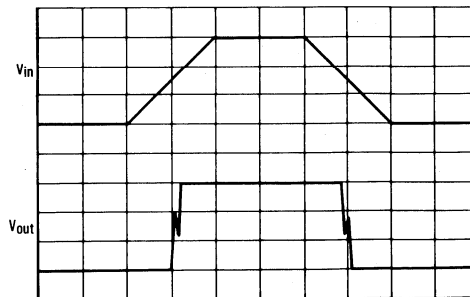


Figure 15. Maximum Rise Time Violation



## STANDARD OUTPUT CHARACTERISTICS

**N-CHANNEL SINK CURRENT**

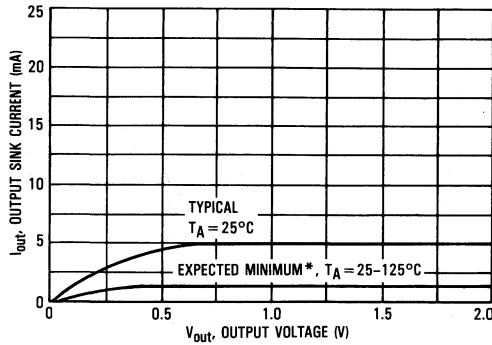


Figure 16.  $V_{GS} = 2.0\text{ V}$

**P-CHANNEL SOURCE CURRENT**

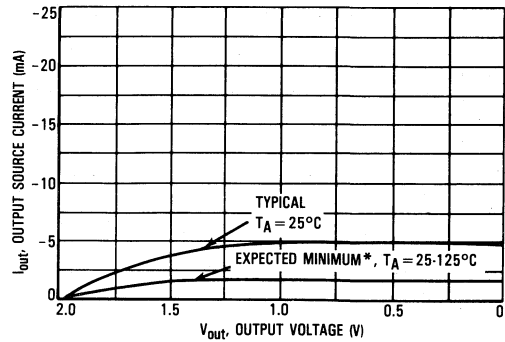


Figure 17.  $V_{GS} = -2.0\text{ V}$

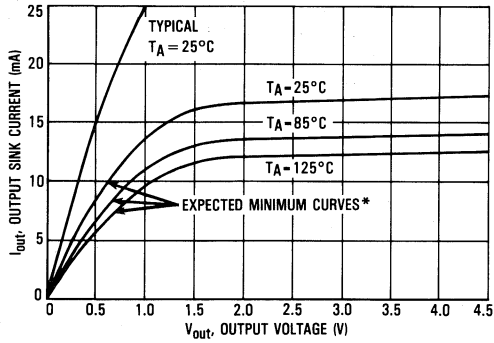


Figure 18.  $V_{GS} = 4.5\text{ V}$

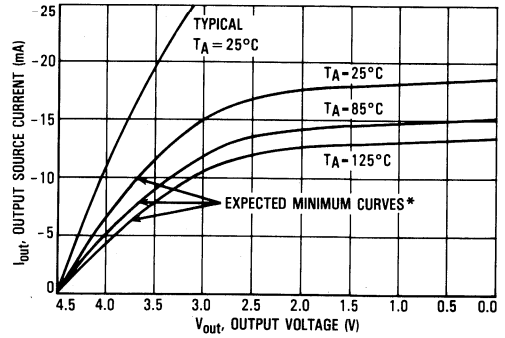


Figure 19.  $V_{GS} = -4.5\text{ V}$

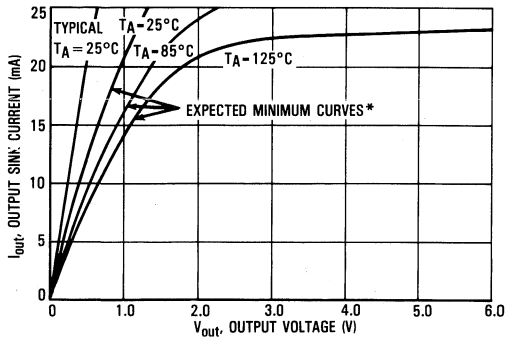


Figure 20.  $V_{GS} = 6.0\text{ V}$

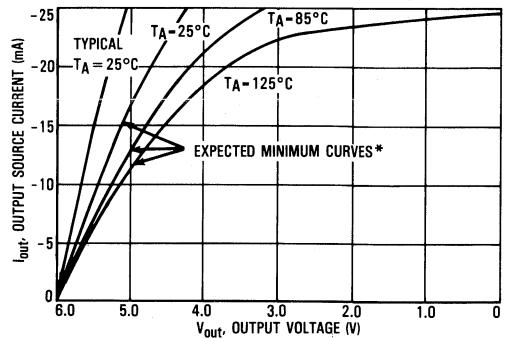


Figure 21.  $V_{GS} = -6.0\text{ V}$

\*The expected minimum curves are not guarantees but are design aids.

## BUS-DRIVER OUTPUT CHARACTERISTICS

### N-CHANNEL SINK CURRENT

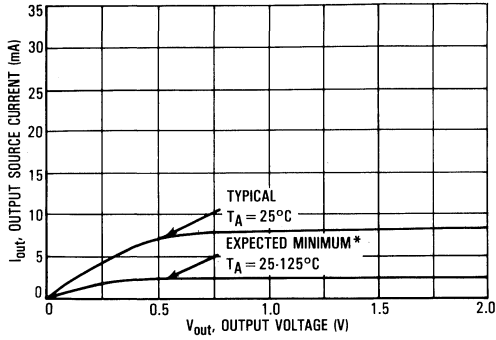


Figure 22.  $V_{GS} = 2.0$  V

### P-CHANNEL SOURCE CURRENT

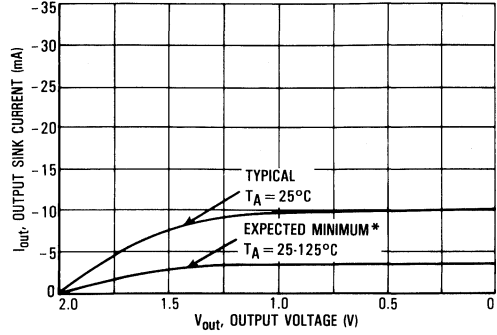


Figure 23.  $V_{GS} = -2.0$  V

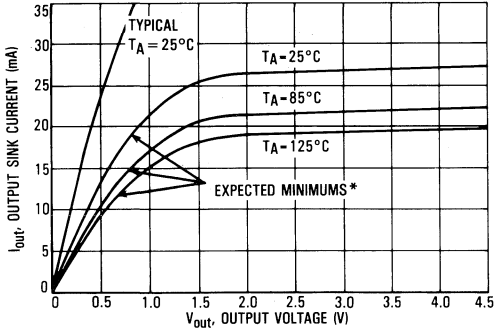


Figure 24.  $V_{GS} = 4.5$  V

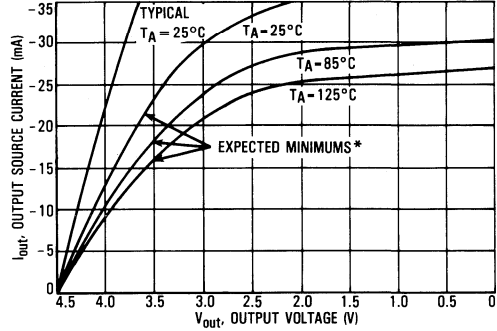


Figure 25.  $V_{GS} = -4.5$  V

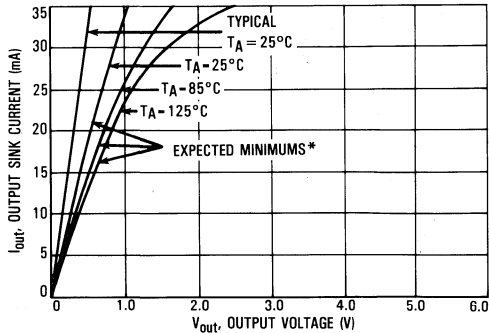


Figure 26.  $V_{GS} = 6.0$  V

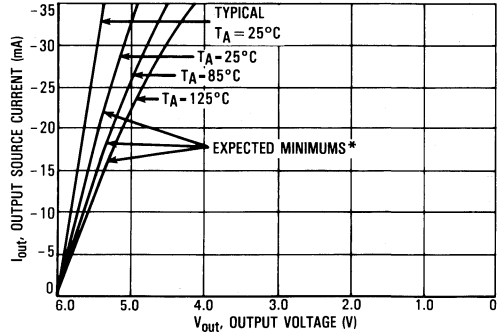


Figure 27.  $V_{GS} = -6.0$  V

\*The expected minimum curves are not guarantees, but are design aids.

### 3-STATE OUTPUTS

Some HC/HCT devices have outputs that can be placed into a high-impedance state. These 3-state output devices are very useful for gang connecting to a common line or bus. When enabled, these output pins can be considered as ordinary output pins; as such, all specifications and precautions of standard output pins should be followed. When disabled (high-impedance state), these outputs can be modeled as in Figure 28. Output leakage current ( $10 \mu\text{A}$  worst case over temperature) as well as 3-state output capacitance must be considered in any bus design.

When power is interrupted to a 3-state device, the bus voltage is forced to between GND and  $V_{CC} + 0.7 \text{ V}$  regardless of the previous output state.

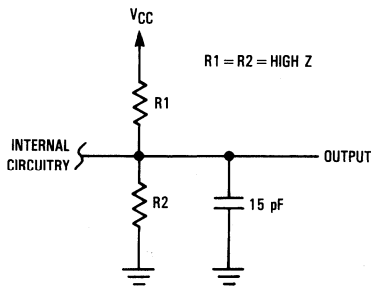


Figure 28. Model for Disabled Outputs

### OPEN-DRAIN OUTPUTS

Motorola provides several devices that are designed only to sink current to GND. These open-drain output devices are fabricated using only an N-channel transistor and a diode to  $V_{CC}$  (Figure 29). The purpose of the diode is to provide ESD protection. Open-drain outputs can be modeled as shown in Figure 30.

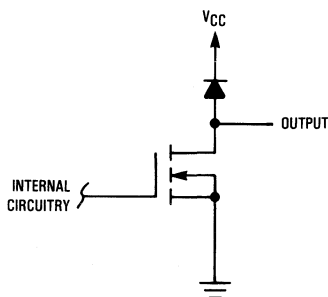


Figure 29. Open-Drain Output

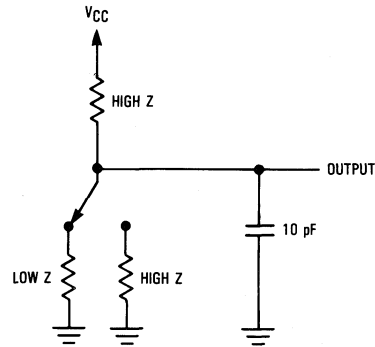


Figure 30. Model of Open-Drain Output

### INPUT/OUTPUT PINS

Some HC/HCT devices contain pins that serve both as inputs and outputs of digital logic. These pins are referred to as digital I/O pins. The logic level applied to a control pin determines whether these I/O pins are selected as inputs or outputs.

When I/O pins are selected as outputs, these pins may be considered as standard CMOS outputs. When selected as inputs, except for an increase in input leakage current and input capacitance, these pins should be considered as standard CMOS inputs. These increases come from the fact that a digital I/O pin is actually a combination of an input and a 3-state output tied together (see Figure 31).

As stated earlier, all HC/HCT inputs must be connected to an appropriate logic level. This could pose a problem if an I/O pin is selected as an input while connected to an improperly terminated bus.

Motorola recommends terminating HC/HCT-type buses with resistors to  $V_{CC}$  or GND of between  $1 \text{ k}\Omega$  to  $1 \text{ M}\Omega$  in value. The choice of resistor value is a trade-off between speed and power consumption (see **Bus Termination**, this chapter).

Some Motorola devices have analog I/O pins. These analog I/O pins should not be confused with digital I/O pins. Analog I/O pins may be modeled as in Figure 32. These devices can be used to pass analog signals, as well as digital signals, in the same manner as mechanical switches.

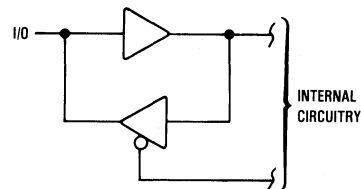


Figure 31. Typical Digital I/O Pin

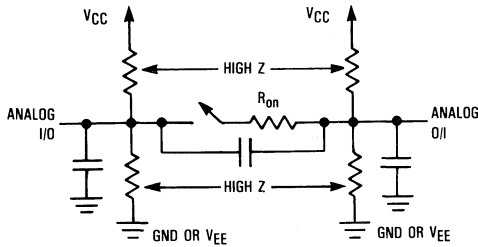


Figure 32. Analog I/O Pin

### BUS TERMINATION

Because buses tend to operate in harsh, noisy environments, most bus lines are terminated via a resistor to  $V_{CC}$  or ground. This low impedance to  $V_{CC}$  or ground (depending on preference of a pull-up or pull-down logic level) reduces bus noise pickup. In certain cases a bus line may be released (put in a high-impedance state) by disabling all the 3-state bus drivers (see Figure 33). In this condition all HC/HCT inputs on the bus would be allowed to float. A CMOS input or I/O pin (when selected as an input) should never be allowed to float. (This is one reason why an HCT device may not be a drop-in replacement of an LSTTL device.) A floating CMOS input can put the device into the linear region of operation. In this region excessive current can flow and the possibility of logic errors due to oscillation may occur (see **Inputs**, this chapter). Note that when a bus is properly terminated with pull-up resistors, HC devices, instead of HCT devices, can be driven by an NMOS or LSTTL bus driver. HC devices are preferred over HCT devices in bus applications because of their higher low-level input noise margin. (With a 5 V supply the typical HC switch point is 2.3 V while the switch point of HCT is only 1.3 V.)

Some popular LSTTL bus termination designs may not work for HSCMOS devices. The outputs of HSCMOS may not be able to drive the low value of termination used by some buses. (This is another reason why an HCT device may not be a drop-in replacement for an LSTTL device.) However, because low power operation is one of the main reasons for using CMOS, an optimized CMOS bus termination is usually advantageous.

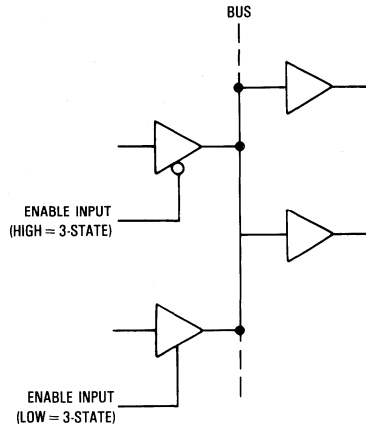


Figure 33. Typical Bus Line with 3-State Bus Drivers

The choice of termination resistances is a trade-off between speed and power consumption. The speed of the bus is a function of the RC time constant of the termination resistor and the parasitic capacitance associated with the bus. Power consumption is a function of whether a pull-up or pull-down resistor is used and the output state of the device that has control of the bus (see Figure 34). The lower the termination resistor the faster the bus operates, but more power is consumed. A large value resistor wastes less power, but slows the bus down. Motorola recommends a termination resistor value between 1 k $\Omega$  and 1 M $\Omega$ . An alternative to a passive resistor termination would be an active-type termination (see Figure 35). This type termination holds the last logic level on the bus until a driver can once again take control of the bus. An active termination has the advantage of consuming a minimal amount of power. Most HC/HCT bus drivers do not have built-in hysteresis. Therefore, heavily loaded buses can slow down rise and fall signals and exceed the input rise/fall time defined in JEDEC Standard No. 7A. In this event, devices with Schmitt-triggered inputs should be used to condition these slow signals.

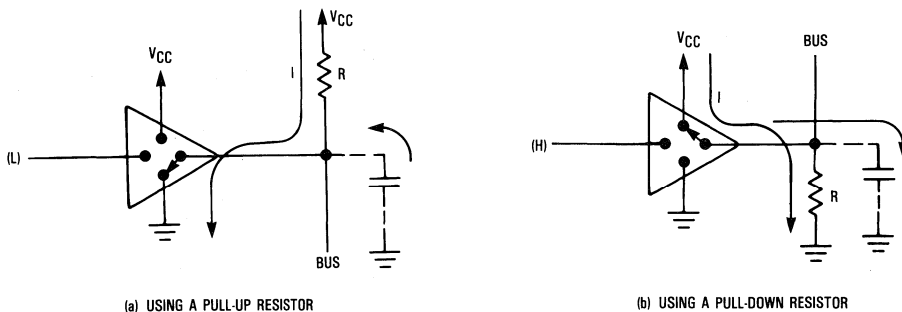


Figure 34

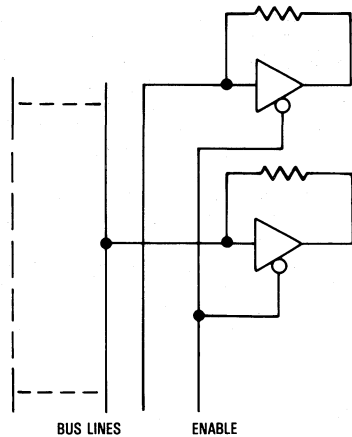


Figure 35. Using Active Termination (HC125)

#### TRANSMISSION LINE TERMINATION

When data is transmitted over long distances, the line on which the data travels can be considered a transmission line. (Long distance is relative to the data rate being transmitted.) Examples of transmission lines include high-speed buses, long PCB lines, coaxial and ribbon cables. All transmission lines should be properly terminated into a low-impedance termination. A low-impedance termination helps eliminate noise, ringing, overshoot, and crosstalk problems. Also a low-impedance termination reduces signal degradation because the small values of parasitic line capacitance and inductance have lesser effect on a low-impedance line.

The value of the termination resistor becomes a trade-off between power consumption, data rate speeds, and transmission line distance. The lower the resistor value, the faster data can be presented to the receiving device, but the more power the resistor consumes. The higher the resistor value, the longer it will take to charge and discharge the transmission line through the termination resistor ( $T = R \cdot C$ ).

Transmission line distance becomes more critical as data rates increase. As data rates increase, incident (and reflective) waves begin to resemble that of RF transmission line theory. However, due to the nonlinearity of CMOS digital logic, conventional RF transmission theory is not applicable.

HC devices are preferred over HCT devices due to the fact that HC devices have higher switch points than HCT devices. This higher switch point allows HC devices to achieve better incident wave switching on lower impedance lines.

HC/HCT may not have enough drive capability to interface with some of the more popular LSTTL transmission lines. (Possible reason why an HCT device may not be a drop-in replacement of an equivalent TTL device.) This does not pose a major problem since having larger value termination resistors is desirable for CMOS type transmission lines.

By increasing the termination resistance value, the CMOS advantage of low power consumption can be realized. Motorola recommends a minimum termination resistor value as shown in Figure 36. The termination resistor should be as close to the receiving unit as possible. Another method of

terminating the line driver, as well as the receiving unit, is shown in Figure 37. Note that the resistor values in Figure 37 are twice the resistor value of Figure 36; this gives a net equivalent termination value of Figure 36. Even higher values of resistors may be used for either termination method. This reduces power consumption, but at the expense of speed and possible signal degradation.

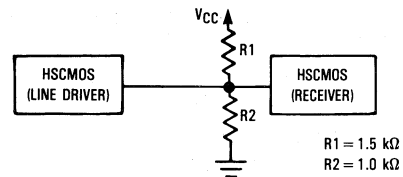


Figure 36. Termination Resistors at the Receiver

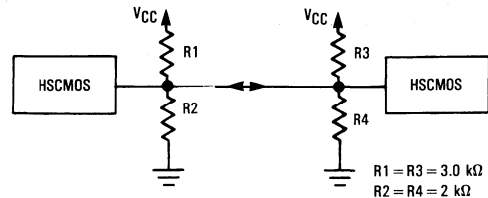


Figure 37. Termination Resistors at Both the Line Driver and Receiver

#### CMOS LATCH UP

Typically, HSCMOS devices do not latch up with currents of 75 mA forced into or out of the inputs or 300 mA for the outputs under worst case conditions ( $T_A = 125^\circ\text{C}$  and  $V_{CC} = 6\text{ V}$ ). Under dc conditions for the inputs, the input protection network typically fails, due to grossly exceeding the maximum input voltage rating of  $-1.5$  to  $V_{CC} + 1.5\text{ V}$  before latch-up currents are reached. For most designs, latch up will not be a problem, but the designer should be aware of it, what causes it, and how it can be prevented.

Figure 38 shows the layout of a typical CMOS inverter and Figure 39 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the device on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than  $V_{CC} + 0.5\text{ V}$  or less than  $-0.5\text{ V}$  and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device can be destroyed or its reliability can be degraded. Ways to prevent such an occurrence are listed below.

1. Industrial controllers driving relays or motors is an environment in which latch up is a potential problem. Also, the ringing due to inductance of long transmission lines in an industrial setting could provide enough energy to latch up CMOS devices. Opto-isolators, such as Motorola's MOC3011, are recommended to reduce chances of latch up. See the Motorola Semiconductor Master Selection Guide for a complete listing of Motorola opto-isolators.
2. Ensure that inputs and outputs are limited to the maximum rated values.

$$-1.5 \leq V_{in} \leq V_{CC} + 1.5 \text{ V referenced to GND}$$

$$-0.5 \leq V_{out} \leq V_{CC} + 0.5 \text{ V referenced to GND}$$

$$|I_{in}| \leq 20 \text{ mA}$$

$$|I_{out}| \leq 25 \text{ mA for standard outputs}$$

$$|I_{out}| \leq 35 \text{ mA for bus-driver outputs}$$

3. If voltage transients of sufficient energy to latch up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another

method of protection is to use a series resistor to limit the expected worst case current to the maximum ratings value.

See **Handling Precautions** for other possible protection circuits and a discussion of ESD prevention.

4. Sequence power supplies so that the inputs or outputs of HSCMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug-in board applications).
5. Voltage regulating and filtering should be used in board design and layout to ensure that power supply lines are free of excessive noise.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power-supply filtering network or with a current-limiting regulator.

#### RECOMMENDED READING

Paul Mannone, "Careful Design Methods Prevent CMOS Latch-Up", EDN, January 26, 1984.

4

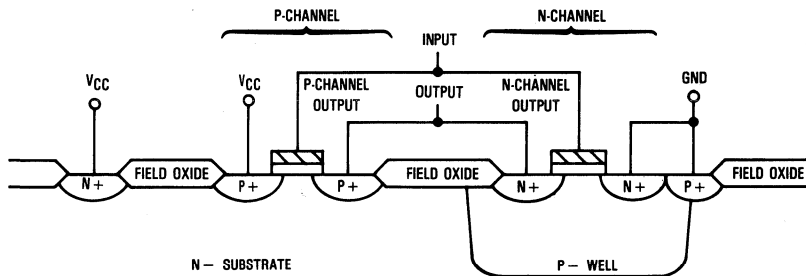


Figure 38. CMOS Wafer Cross Section

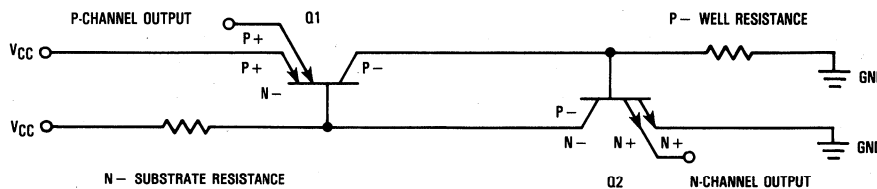


Figure 39. Latch-Up Circuit Schematic

## MAXIMUM POWER DISSIPATION

The maximum power dissipation for Motorola HSCMOS packages is 750 mW for both ceramic and plastic DIPs and 500 mW for SOIC packages. The deratings are  $-10 \text{ mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  for plastic DIPs,  $-10 \text{ mW}/^\circ\text{C}$  from  $100^\circ\text{C}$  for ceramic packages, and  $-7 \text{ mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  for SOIC packages. This is illustrated in Figure 40.

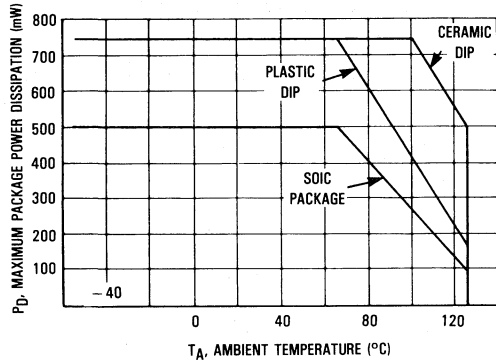


Figure 40. Maximum Package Power Dissipation versus Temperature

Internal heat generation in HSCMOS devices comes from two sources, namely, the quiescent power and dynamic power consumption.

In the quiescent state, either the P-channel or N-channel transistor in each complementary pair is off except for small source-to-drain leakage due to the inputs being either at  $V_{CC}$  or ground. Also, there are the small leakage currents flowing in the reverse-biased input protection diodes and the parasitic diodes on the chip. The specification which takes all leakage into account is called Maximum Quiescent Supply Current (per package), or  $I_{CC}$ , and is shown on all data sheets.

The three factors which directly affect the value of quiescent power dissipation are supply voltage, device complexity, and temperature. On the data sheets,  $I_{CC}$  is specified only at  $V_{CC}=6.0 \text{ V}$  because this is the worst-case supply voltage condition. Also, larger or more complex devices consume more quiescent power because these devices contain a proportionally greater reverse-biased diode junction area and more off (leaky) FETs.

Finally, as can be seen from the data sheets, temperature increases cause  $I_{CC}$  increases. This is because at higher temperatures, leakage currents increase.

### HC QUIESCENT POWER DISSIPATION

When HC device inputs are virtually at  $V_{CC}$  or GND potential (as in a totally CMOS system), quiescent power dissipation is minimized. The equation for HC quiescent power dissipation is given by:

$$P_D = V_{CC} I_{CC}$$

Worst-case  $I_{CC}$  occurs at  $V_{CC}=6.0 \text{ V}$ . The value of  $I_{CC}$  at  $V_{CC}=6.0 \text{ V}$ , as specified in the data sheets, is used for all power supply voltages from 2 to 6 V.

### HCT QUIESCENT POWER DISSIPATION

Although HCT devices belong to the CMOS family, their input voltage specifications are identical to those of LSTTL. HCT parts can therefore be either judiciously substituted for or mixed with LS devices in a system.

TTL output voltages are  $V_{OL}=0.4 \text{ V}$  (max) and  $V_{OH}=2.4$  to  $2.7 \text{ V}$  (min).

Slightly higher  $I_{CC}$  current exists when an HCT device is driven with  $V_{OL}=0.4 \text{ V}$  (max) because this voltage is high enough to partially turn on the N-channel transistor. However, when being driven with a TTL  $V_{OH}$ , HCT devices exhibit large additional current flow ( $\Delta I_{CC}$ ) as specified on HCT device data sheets.  $\Delta I_{CC}$  current is caused by the off-rail input voltage turning on both the P and N channels of the input buffer. This condition offers a relatively low impedance path from  $V_{CC}$  to GND. Therefore, the HCT quiescent power dissipation is dependent on the number of inputs applied at the TTL  $V_{IH}$  logic voltage level.

The equation for HCT quiescent power dissipation is given by:

$$P_D = I_{CC} V_{CC} + \eta \Delta I_{CC} V_{CC}$$

where  $\eta$  = the number of inputs at the TTL  $V_{IH}$  level.

### HC AND HCT DYNAMIC POWER DISSIPATION

Dynamic power dissipation is calculated in the same way for both HC and HCT devices. The three major factors which directly affect the magnitude of dynamic power dissipation are load capacitance, internal capacitance, and switching transient currents.

The dynamic power dissipation due to capacitive loads is given by the following equation:

$$P_D = C_L V_{CC}^2 f$$

where  $P_D$  = power in  $\mu\text{W}$ ,  $C_L$  = capacitive load in pF,  $V_{CC}$  = supply voltage in volts, and  $f$  = output frequency driving the load capacitor in MHz.

All CMOS devices have internal parasitic capacitances that have the same effect as external load capacitors. The magnitude of this internal no-load power dissipation capacitance,  $C_{PD}$ , is specified as a typical value.

Finally, switching transient currents affect the dynamic power dissipation. As each gate switches, there is a short period of time in which both N- and P-channel transistors are partially on, creating a low-impedance path from  $V_{CC}$  to ground. As switching frequency increases, the power dissipation due to this effect also increases.

The dynamic power dissipation due to  $C_{PD}$  and switching transient currents is given by the following equation:

$$P_D = C_{PD} V_{CC}^2 f$$

Therefore, the total dynamic power dissipation is given by:

$$P_D = (C_L + C_{PD}) V_{CC}^2 f$$

Total power dissipation for HC and HCT devices is merely a summation of the dynamic and quiescent power dissipation elements. When being driven by CMOS logic voltage levels (rail to rail), the total power dissipation for both HC and HCT devices is given by the equation:

$$P_D = V_{CC}I_{CC} + (C_L + C_{PD})V_{CC}^2f$$

When being driven by LSTTL logic voltage levels, the total power dissipation for HCT devices is given by the equation:

$$P_D = V_{CC}I_{CC} + V_{CC}\Delta I_{CC}(\delta_1 + \delta_2 + \dots + \delta_n) + (C_L + C_{PD})V_{CC}^2f$$

where  $\delta_n$  = duty cycle of LSTTL output applied to each input of an HCT device.

### CAPACITIVE LOADING EFFECTS ON PROPAGATION DELAY

In addition to temperature and power-supply effects, capacitive loading effects should be taken into account. The additional propagation delay may be calculated if the short circuit current for the device is known. Expected minimum numbers may be determined from Table 2.

From the equation

$$i = \frac{Cdv_c}{dt}$$

this approximation follows:

$$I = \frac{C\Delta V}{\Delta t}$$

so

$$\Delta t = \frac{C\Delta V}{I}$$

or

$$\Delta t = \frac{C(0.5 V_{CC})}{I}$$

because the propagation delay is measured to the 50% point of the output waveform (typically  $0.5 V_{CC}$ ).

This equation gives the general form of the additional propagation delay. To calculate the propagation delay of a device for a particular load capacitance,  $C_L$ , the following equation may be used.

$$t_{pT} = t_p + 0.5 V_{CC} (C_L - 50 \text{ pF}) / I_{OS}$$

where  $t_{pT}$  = total propagation delay

$t_p$  = specified propagation delay with 50 pF load

$C_L$  = actual load capacitance

$I_{OS}$  = short circuit current (Table 2)

An example is given here for  $t_{PHL}$  of the 74HC00 driving a 150 pF load.

$$V_{CC} = 4.5 \text{ V}$$

$$t_{PHL} (50 \text{ pF}) = 18 \text{ ns}$$

$$C_L = 150 \text{ pF}$$

$$I_{OS} = 17.3 \text{ mA}$$

$$t_{PHL} (150 \text{ pF}) = 18 \text{ ns} + \frac{(0.5)(4.5 \text{ V})(150 \text{ pF} - 50 \text{ pF})}{17.3 \text{ mA}}$$

$$= 18 \text{ ns} + 13 \text{ ns}$$

$$= 31 \text{ ns}$$

Another example for  $C_L = 0$  pF and all other parameters the same.

$$t_{PHL} (0 \text{ pF}) = 18 \text{ ns} + \frac{(0.5)(4.5 \text{ V})(0 \text{ pF} - 50 \text{ pF})}{17.3 \text{ mA}}$$

$$= 18 \text{ ns} + (-6.5 \text{ ns})$$

$$t_{PHL} = 11.5 \text{ ns}$$

This method gives the expected propagation delay and is intended as a design aid, not as a guarantee.

Table 2. Expected Minimum Short Circuit Currents\*

Parameter	V <sub>CC</sub>	Standard Drivers			Bus Drivers			Unit
		25°C	85°C	125°C	25°C	85°C	125°C	
Output Short Circuit Source Current	2.0	1.89	1.83	1.80	3.75	3.64	3.60	mA
	4.5	18.5	15.0	13.4	37.0	30.0	26.6	
	6.0	35.2	28.0	24.6	70.6	56.1	49.2	
Output Short Circuit Sink Current	2.0	1.55	1.55	1.55	2.45	2.45	2.43	mA
	4.5	17.3	14.0	12.5	27.2	22.1	19.6	
	6.0	33.4	26.5	23.2	52.6	41.7	36.5	

\*These values are intended as design aids, not as guarantees.



## TEMPERATURE EFFECTS ON DC AND AC PARAMETERS

One of the inherent advantages of CMOS devices is that characteristics of the N- and P-channel transistors, such as drive current, channel resistance, propagation delay, and output transition time, track each other over a wide temperature range. Figure 41 shows the temperature relationships for these parameters. To illustrate the effects of temperature on noise margin, Figure 42 shows the typical transfer characteristics for devices with buffered inputs and outputs. Note that the typical switch point is at 45% of the supply voltage and is minimally affected by temperature.

The graphs in this section are intended to be design aids, not guarantees.

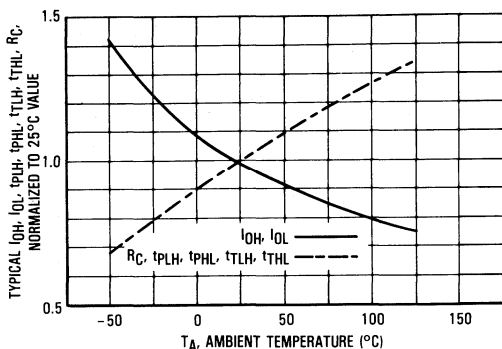


Figure 41. Characteristics of Drive Current, Channel Resistance, and AC Parameters Over Temperature

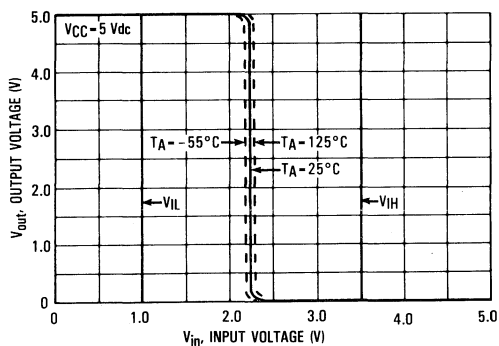


Figure 42. Temperature Effects on the HC Transfer Characteristics

## SUPPLY VOLTAGE EFFECTS ON DRIVE CURRENT AND PROPAGATION DELAY

The transconductive gain,  $I_{out}/V_{in}$ , of MOSFETs is proportional to the gate voltage minus the threshold voltage,  $V_G - V_T$ . The gate voltage at the input of the final stage of buffered devices is approximately the power supply voltage,  $V_{CC}$  or GND. Because  $V_G = V_{CC}$  or GND, the output drive current is proportional to the supply voltage. Propagation delays for CMOS devices are also affected by the power supply voltage, because most of the delay is due to charging and discharging internal capacitances. Figures 43 and 44 show the typical variation of current drive and propagation delay, normalized to  $V_{CC} = 4.5$  V for  $2.0 \leq V_{CC} \leq 6.0$  V. These curves may be used with the tables on each data sheet to arrive at parametric values over the voltage range.

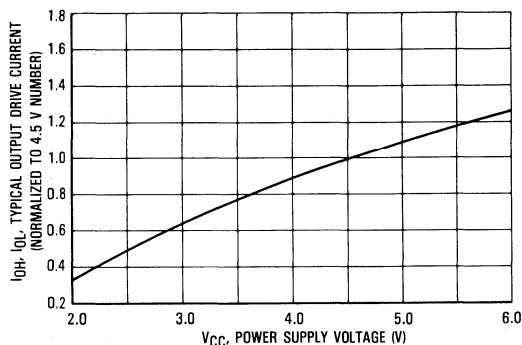


Figure 43. Drive Current versus  $V_{CC}$

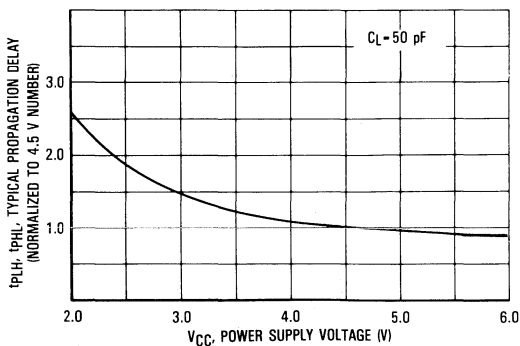


Figure 44. Propagation Delay versus  $V_{CC}$

4

## DECOUPLING CAPACITORS

The switching waveforms shown in Figures 45 and 46 show the current spikes introduced to the power supply and ground lines. This effect is shown for a load capacitance of less than 5 pF and for 50 pF. For ideal power supply lines with no series impedance, the spikes would pose no problem. However, actual power supply and ground lines do possess series impedance, giving rise to noise problems. For this reason, care should be taken in board layouts, ensuring low impedance paths to and from logic devices.

To absorb switching spikes, the following HSCMOS devices should be bypassed with good quality 0.022  $\mu\text{F}$  to 0.1  $\mu\text{F}$  decoupling capacitors:

1. Bypass every device driving a bus with all outputs switching simultaneously.
2. Bypass all synchronous counters.
3. Bypass devices used as oscillator elements.
4. Bypass Schmitt-trigger devices with slow input rise and fall times. The slower the rise and fall time, the larger the bypass capacitor. Lab experimentation is suggested.

Bypass capacitors should be distributed over the circuit board. In addition, boards could be decoupled with a 1  $\mu\text{F}$  capacitor.

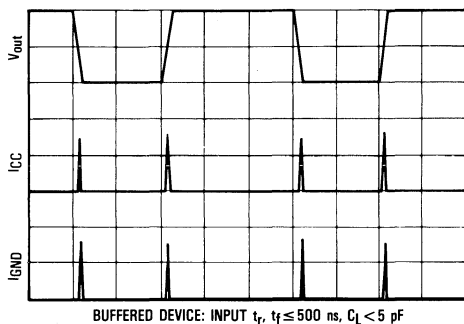


Figure 45. Switching Currents for  $C_L < 5$  pF

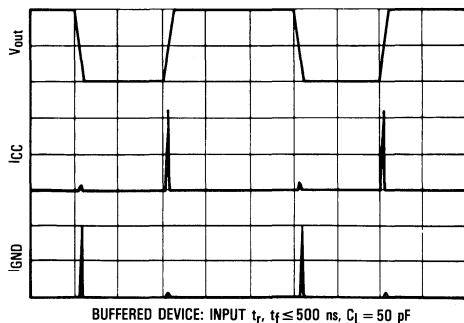


Figure 46. Switching Currents for  $C_L = 50$  pF

## INTERFACING

HSCMOS devices have a wide operating voltage range ( $V_{CC} = 2$  to 6 V) and sufficient current drive to interface with most other logic families available today. In this section, various interface schemes are given to aid the designer (see Figures 47 through 52). The various types of CMOS devices with their input/output levels and comments are given in Table 3.

Motorola presently has available several CMOS memories and microprocessors (see Table 4) which are designed to directly interface with High-Speed CMOS. With these devices now available, the designer has an attractive alternative to LSTTL/NMOS, and a total HSCMOS system is now possible. (See SG102, CMOS System IC Selection Guide, for more information.)

Device designators are as follows:

- HC** This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs. The numbering of devices with this designator follows the LSTTL numbering sequence. These devices are functional and pinout equivalents of LSTTL devices (e.g., HC00, HC688, etc.). Exceptions to this are devices that are functional and pinout equivalents to metal-gate CMOS devices (e.g., HC4002, HC4538A, etc.).
- HCU** This is an unbuffered high-speed CMOS device with only one stage between the input and output. Because this is an unbuffered device, input and output levels may differ from buffered devices. At present, the family contains only one unbuffered device, the HCU04A.
- HCT** This is a high-speed CMOS device with an LSTTL-to-CMOS input buffer stage. These devices are designed to interface with LSTTL outputs operating at  $V_{CC} = 5 \text{ V} \pm 10\%$ . HCT devices have fully buffered CMOS outputs that directly drive HSCMOS or LSTTL devices.

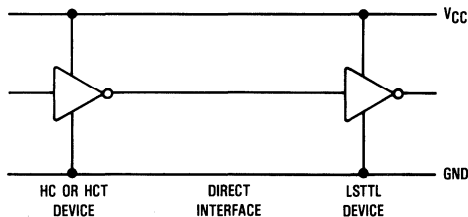


Figure 47. HC to LSTTL Interfacing

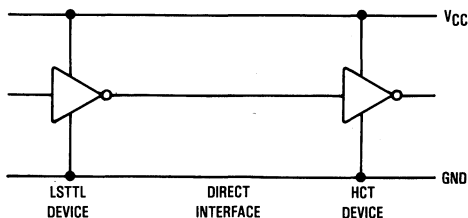


Figure 48. LSTTL to HCT Interfacing

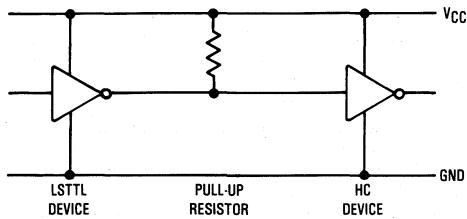


Figure 49. LSTTL to HC Interfacing

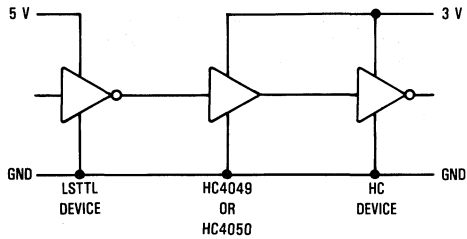
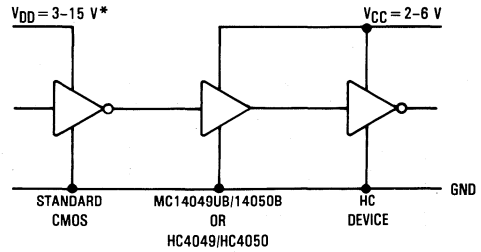


Figure 50. LSTTL to Low-Voltage HSCMOS



\* $V_{OH}$  must be greater than  $V_{IH}$  of low voltage Device;  $V_{DD}$  = 3-18 V may be used if interfacing to 14049UB/14050B.

Figure 51. High Voltage CMOS to HSCMOS

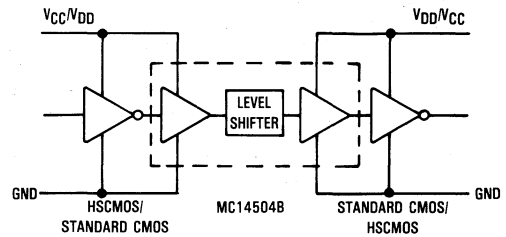


Figure 52. Up/Down Level Shifting Using the MC14504B

Table 3. Interfacing Guide

Device	Input Level	Output Level	Comments
HCXXX	CMOS	CMOS	LSTTL Functional and Pinout Equivalent Devices
HC4XXX	CMOS	CMOS	CMOS Functional and Pinout Equivalent Devices
HCUXX	CMOS	CMOS	Used in Linear Applications
HCTXXX	TTL	CMOS	HSCMOS Device with TTL-to-CMOS Input Buffering
HC4049, HC4050	$-0.5 \leq V_{in} \leq 15$ V	CMOS	High-to-Low Level Translators, CMOS Switching Levels
MC14049UB MC14050B	$-0.5 \leq V_{in} \leq 18$ V	CMOS	Metal-Gate CMOS High-to-Low Level Translators, CMOS Switching Levels
MC14504B	CMOS or TTL	CMOS	Metal-Gate CMOS High-to-Low or Low-to-High Level Translator

Table 4. CMOS Memories and Microprocessors

CMOS Memories	CMOS Microprocessors
MCM6147	MC68HC01
MCM61L47	MC68HC03
MCM68HC34	MC68HC11A8
	MC68HC11D4
	MC68HC811A2
	MC68HC811D4
	MC68HC04P3
	MC146805E2
	MC146805F2
	MC146805G2
	MC1468705F2
	MC68HC05C4
	MC68HSC05C4
	MC68HC05C8
	MC68HC805C4
	MC68HC000

#### RECOMMENDED READING

S. Craig, "Using High-Speed CMOS Logic for Microprocessor Interfacing", Application Note-868, Motorola Semiconductor Products Inc., 1982.

## TYPICAL PARAMETRIC VALUES

Given a fixed voltage and temperature, the electrical characteristics of High-Speed CMOS devices depend primarily on design, layout, and processing variations inherent in semiconductor fabrication.

A preliminary evaluation of each device type essentially guarantees that the design and layout of the device conforms to the criteria and standards set forth in the design goals. With very few exceptions, device electrical parameters, once established, do not vary due to design and layout.

Of much more concern is processing variation. A digital processing line is allowed to deviate over a fairly broad processing range. This allows the manufacturer to incur reduced processing costs. These reduced processing costs are passed on to the consumer in the form of lower device prices.

Processing variation is the range from worst case to best case processing and is defined as the process window. This window is established with the aid of statistical process control (SPC). With SPC, when a processing parameter approaches the process window limit, that parameter is adjusted toward the middle of the window. This keeps process variations within a predetermined tolerance.

Motorola characterizes each device type over this process window. Each device type is characterized by allowing experimental lots to be processed using worst case and best case processing. The worst case processed lots usually determine the minimum or maximum guaranteed limit. (Whether the limit is a guaranteed minimum or maximum depends on the particular parameter being measured.)

In production, these limits are guaranteed by probe and final test and therefore appear independent of process variation to the end user. However, this does not hold true for the mean value of the total devices processed. The mean value, commonly referred to as a typical value, shifts over processing and therefore varies from lot to lot or even wafer to wafer within a lot.

As with all processing or manufacturing, the total devices being produced fit the normal distribution or bell curve of Figure 53. In order to guarantee a valid typical value, a typical number plus a tolerance, would have to be specified and tested (see Figure 54). However, this would greatly increase processing costs which would have to be absorbed by the consumer.

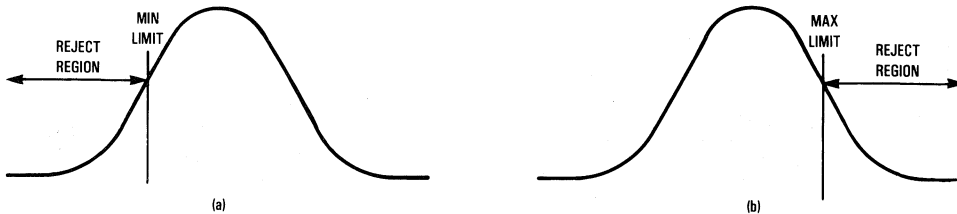


Figure 53

In some cases, the device's actual values are so small that the resolution of the automatic test equipment determines the guaranteed limit. An example of this is quiescent supply current and input leakage current.

Most manufacturers provide typical numbers by one of two methods. The first method is to simply double or halve, depending on the parameter, the guaranteed limit to determine a typical number. This would theoretically put all processed lots in the middle of the process window. Another approach to typical numbers is to use a typical value that is derived from the aforementioned experimental lots. However, neither method accurately reflects the mean value of devices any one consumer can expect to receive.

Therefore, the use of typical parametric numbers for design purposes does not constitute sound engineering design practice. Worst case analysis dictates the use of guaranteed minimum or maximum values. The only possible exception would be when no guaranteed value is given. In this case a typical value may be used as a ballpark figure.

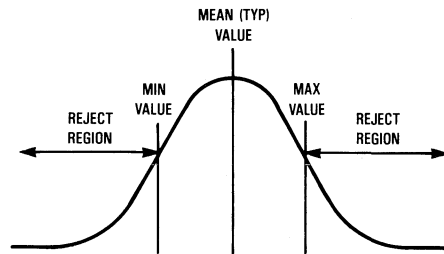


Figure 54

## REDUCTION OF ELECTROMAGNETIC INTERFERENCE (EMI)

Electromagnetic interference (EMI) and radio frequency interference (RFI) are phenomena inherent in all electrical systems covering the entire frequency spectrum. Although the characteristics have been well documented, EMI remains difficult to deal with due to numerous variables. EMI should be considered at the beginning of a design, and taken into account during all stages, including production and beyond.

These entities must be present for EMI to be a factor: (1) a source of EMI, (2) a transmission medium for EMI, and (3) a receiver of EMI. Several sources include relays, FM transmitters, local oscillators in receivers, power lines, engine ignitions, arc welders, and lighting. EMI transmission paths include ground connections, cables, and the space between conductors. Some receivers of EMI are radar receivers, computers, and television receivers.

For microprocessor based equipment, the source of emissions is usually a current loop on a PC board. The chips and their associated loop areas also function as receivers of EMI. The fact is that PC boards which radiate high levels of EMI are also more likely to act as receivers of EMI.

All logic gates are potential transmitters and receivers of emissions. Noise immunity and noise margin are two criterion which measure a gate's immunity to noise which could be caused by EMI. CMOS technology, as opposed to the other commonly used logic families, offers the best value for noise margin, and is therefore an excellent choice when considering EMI.

The electric and magnetic fields associated with ICs are proportional to the current used, the current loop area, and the switching transition times. CMOS technology is preferred due to smaller currents. Also, the current loop area can be reduced by the use of surface mount packages.

In a system where several pieces of equipment are connected by cables, at least five coupling paths should be taken into account to reduce EMI. They are: (1) common ground impedance coupling (a common impedance is shared between an EMI source and receiver), (2) common-mode, field-to-cable coupling (electromagnetic fields enter the loop formed by two pieces of equipment, the cable connecting them, and the ground plane), (3) differential-mode, field-to-cable coupling (electromagnetic fields enter the loop formed by two pieces of equipment and the cable connecting them), (4) crosstalk coupling (signals in one transmission line are coupled into another transmission line), and (5) a conductive path through power lines.

Shielding is a means of reducing EMI. Some of the more commonly used shields against EMI and RFI contain stainless steel fiber-filled polycarbonate, aluminum flake-filled polycarbonate/ABS coated with nickel and copper electrolysis plating or cathode sputtering, nickel coated graphite fiber, and polyester SMC with carbon-fiber veil. Several manufacturers who make conductive compounds and additives are listed below.

## SHIELDING MANUFACTURERS

General Electric Co., Plastics Group, Pittsfield, MA  
Mobay Chemical Corp., Pittsburg, PA  
Wilson-Fiberfil International, Evansville, IN  
American Cyanamid Co., Wayne, NJ  
Fillite U.S.A., Inc., Huntington, WV  
Transnet Corp., Columbus, OH

Motorola does not recommend, or in any way warrant the manufacturers listed here. Additionally, no claim is made that this list is by any means complete.

## RECOMMENDED READING

D. White, K. Atkinson, and J. Osburn, "Taming EMI in Microprocessor Systems", *IEEE Spectrum*, Vol. 22, Number 12, Dec. 1985.

D. White and M. Mardiguian, *EMI Control Methodology and Procedures*, 1985.

H. Denny, *Grounding for the Control of EMI*.

M. Mardiguian, *How to Control Electrical Noise*.

D. White, *Shielding Design Methodology and Procedures*.

For more information on this subject, contact:

Interference Control Technologies  
Don White Consultants, Inc., Subsidiary  
State Route 625  
P.O. Box D  
Gainesville, VA 22065

4

## HYBRID CIRCUIT GUIDELINES

High-Speed CMOS devices, when purchased in chip (die) form, are useful in hybrid circuits. Most high-speed devices are fabricated with P wells and N substrates. Therefore, the substrates should be tied to  $V_{CC}$  (+ supply).

Several devices however, are fabricated with N wells and P substrates. In this case, the substrates should be tied to GND. The best solution to alleviate confusion about the substrate is the use of nonconductive or insulative substrates. This averts the necessity of tying the substrate off to either  $V_{CC}$  or GND.

For more information on hybrid technology, contact:

International Society for Hybrid Microelectronics  
P.O. Box 3255  
Montgomery, AL 36109

## SCHMITT-TRIGGER DEVICES

Schmitt-trigger devices exhibit the effect of hysteresis. Hysteresis is characterized by two different switching threshold levels, one for positive-going input transitions and the other for negative-going input transitions.

Schmitt triggers offer superior noise immunity when compared to standard gates and inverters. Applications for Schmitt triggers include line receivers, sine to square wave converters, noise filters, and oscillators. Motorola offers six versatile Schmitt-trigger devices in the High-Speed CMOS logic family (see Table 5).

The typical voltage transfer characteristics of a standard CMOS inverter and a CMOS Schmitt-trigger inverter are compared in Figures 55 and 56. The singular transfer threshold of the standard inverter is replaced by two distinct thresholds in a Schmitt-trigger inverter. During a positive-going transition of  $V_{in}$ , the output begins to go low after the  $V_{T+}$  threshold is reached. During a negative-going  $V_{in}$  transition,  $V_{out}$  begins to go high after the  $V_{T-}$  threshold is reached. The difference between  $V_{T+}$  and  $V_{T-}$  is defined as  $V_H$ , the hysteresis voltage.

As a direct result of hysteresis, Schmitt-trigger circuits provide excellent noise immunity and the ability to square up signals with long rise and fall times. Positive-going input noise excursions must rise above the  $V_{T+}$  threshold before they

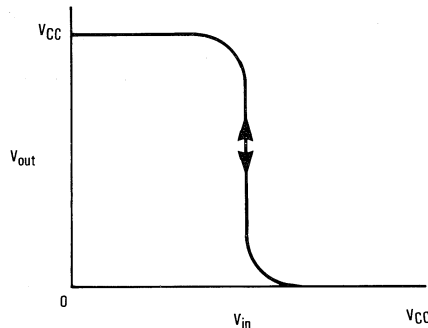
affect the output. Similarly, negative-going input noise excursions must drop below the  $V_{T-}$  threshold before they affect the output.

The HC132A can be used as a direct replacement for the HC00A NAND gate, which does not have Schmitt-trigger capability. The HC132A has the same pin assignment as the HC00A. Schmitt-trigger logic elements act as standard logic elements in the absence of noise or slow rise and fall times, making direct substitution possible.

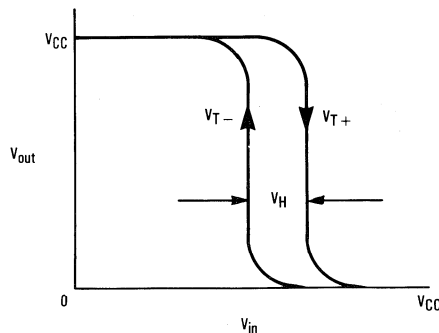
Versatility and low cost are attractive features of CMOS Schmitt triggers. With six Schmitt triggers per HC14A package, one trigger can be used for a noise elimination application while the other five function as standard inverters. Similarly, each of the four triggers in the HC132A can be used as either Schmitt triggers or NAND gates or some combination of both.

**Table 5. Schmitt-Trigger Devices**

HC14A	Hex Schmitt-Trigger Inverter
HC14A	Hex Schmitt-Trigger Inverter
HC132A	Quad 2-Input NAND Gate with Schmitt-Trigger Inputs



**Figure 55. Standard Inverter Transfer Characteristic**



**Figure 56. Schmitt-Trigger Inverter Transfer Characteristic**

## OSCILLATOR DESIGN WITH HIGH-SPEED CMOS

Oscillator design is a fundamental requirement of many systems and several types are discussed in this section. In general, an oscillator is comprised of two parts: an active network and a feedback network. The active network is usually in the form of an amplifier, or an unbuffered inverter, such as the HCU04. The feedback network is mainly comprised of resistors, capacitors, and depending upon the application, a quartz crystal or ceramic resonator.

Buffered inverters are never recommended in oscillator applications due to their high gain and added propagation delay. For this reason Motorola manufactures the HCU04, which is an unbuffered hex inverter.

Oscillators for use in digital systems fall into two general categories, RC oscillators and crystal or ceramic resonator oscillators. Crystal oscillators have the best performance, but are more costly, especially for nonstandard frequencies. RC oscillators are more useful in applications where stability and accuracy are not of prime importance. Where high performance at low frequencies is desired, ceramic resonators are sometimes used.

### RC OSCILLATORS

The circuit in Figure 57 shows a basic RC oscillator using the HCU04. When the input voltage of the first inverter reaches the threshold voltage, the outputs of the two inverters change state, and the charging current of the capacitor changes direction. The frequency at which this circuit oscillates depends upon R1 and C. The equation to calculate these component values is given in Figure 57.

Certain constraints must be met while designing this type of oscillator. Stray capacitance and inductance must be kept to a minimum by placing the passive components as close to the chip as possible. Also, at higher frequencies, the

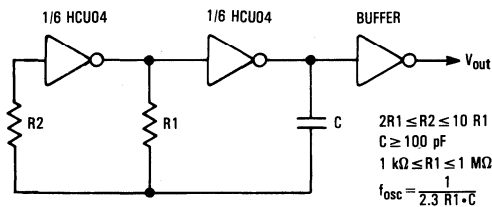
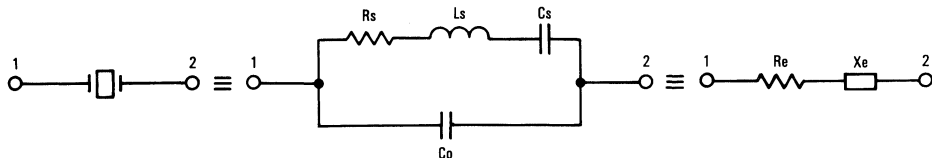


Figure 57. RC Oscillator



Values are supplied by the crystal manufacturer  
(parallel resonant crystal)

Figure 58. Equivalent Crystal Networks

HCU04's propagation delay becomes a dominant effect and affects the cycle time. A polystyrene capacitor is recommended for optimum performance.

### CRYSTAL OSCILLATORS

Crystal oscillators provide the required stability and accuracy which is necessary in many applications. The crystal can be modeled as shown in Figure 58.

The power dissipated in a crystal is referred to as the drive level and is specified in mW. At low drive levels, the resonant resistance of the crystal can be so large as to cause start-up problems. To overcome this problem, the amplifier (inverter) should provide enough amplification, but not too much as to overdrive the crystal.

Figure 59 shows a Pierce crystal oscillator circuit, which is a popular configuration with CMOS.

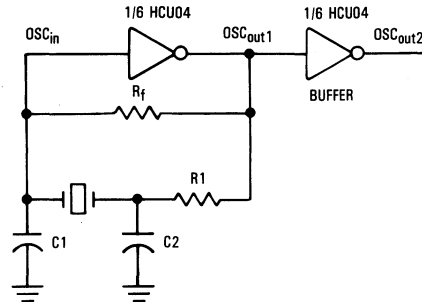


Figure 59. Pierce Crystal Oscillator Circuit

### Choosing R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency at Osc Out 2. The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

### Selecting $R_f$

The feedback resistor ( $R_f$ ) typically ranges up to 20 M $\Omega$ .  $R_f$  determines the gain and bandwidth of the amplifier. Proper bandwidth ensures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone.  $R_f$  must be large enough so as not to affect the phase of the feedback network in an appreciable manner.

### RECOMMENDED READING

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

### PRINTED CIRCUIT BOARD LAYOUT

Noise generators on the power supply lines should be decoupled. The two major sources of noise on the power supply lines are peak current in output stages during switching and the charging and discharging of parasitic capacitances.

A good power distribution network is essential before decoupling can provide any noise reduction. Avoid using jumpers for ground and power connections; the inductance they introduce into the lines permits coupling between outputs. Therefore, use of PC boards with premanufactured ground connections is advised to connect the device pins to ground.

However, the optimum solution is to use multi-layer PC boards where different layers are used for the supply rails and interconnections. Even with double-sided boards, placing the power and ground lines on opposite sides of the board whenever possible is recommended. The multi-wire board is a less expensive approach than the multi-layer PC board, while retaining the same noise reduction characteristics. As a rule of thumb, there should be several ground pins per connector to give good ground distribution.

The precautions for ground lines also apply to  $V_{CC}$  lines: 1) separate power stabilization for each board; 2) isolate noise sources; and 3) avoid the use of large, single voltage regulators.

After all of these precautions, decoupling is an added measure to reduce supply noise. See the **Decoupling Capacitors** section.



# APPLICATIONS ASSISTANCE FORM

In the event that you have any questions or concerns about the performance of any Motorola device listed in this catalog, please contact your local Motorola sales office or the Motorola Help line for assistance. If further information is required, you can request direct factory assistance.

Please fill out as much of the form as is possible if you are contacting Motorola for assistance or are sending devices back to Motorola for analysis. Your information can greatly improve the accuracy of analysis and can dramatically improve the correlation response and resolution time.

Items 4 thru 8 of the following form contain important questions that can be invaluable in analyzing application or device problems. It can be used as a self-help diagnostic guideline or for a baseline of information gathering to begin a dialog with Motorola representatives.

## MOTOROLA Device Correlation/Component Analysis Request Form

– Please fill out entire form and return with devices to MOTOROLA INC., R&QA DEPT., 2200 W. Broadway, Mesa, AZ 85202.

1) Name of Person Requesting Correlation: \_\_\_\_\_

Phone No: \_\_\_\_\_ Job Title: \_\_\_\_\_ Company: \_\_\_\_\_

2) Alternate Contact: \_\_\_\_\_ Phone/Position: \_\_\_\_\_

3) Device Type (user part number): \_\_\_\_\_

4) Industry Generic Device Type: \_\_\_\_\_

5) # of devices tested/sampled: \_\_\_\_\_

# of devices in question\*: \_\_\_\_\_

# returned for correlation: \_\_\_\_\_

\* In the event of 100% failure, does Customer have other date codes of Motorola devices that pass inspection?

Yes \_\_\_\_\_ No \_\_\_\_\_ Please specify passing date code(s) if applicable \_\_\_\_\_

\* If none, does customer have viable alternate vendor(s) for device type?

Yes \_\_\_\_\_ No \_\_\_\_\_ Alternate vendor's name \_\_\_\_\_

6) Date code(s) and Serial Number(s) of devices returned for correlation – If possible, please provide one or two “good” units (Motorola’s and/or other vendor) for comparison: \_\_\_\_\_

7) Describe USER process that device(s) are questionable in:

\_\_\_\_\_ Incoming component inspection {test system = ?}: \_\_\_\_\_

\_\_\_\_\_ Design prototyping: \_\_\_\_\_

\_\_\_\_\_ Board test/burn-in: \_\_\_\_\_

\_\_\_\_\_ Other (please describe): \_\_\_\_\_

8) Please describe the device correlation operating parameters as completely as possible for device(s) in question:

> Describe all pin conditions (e.g., floating, high, low, under test, stimulated but not under test, whatever ...), including any input or output loading conditions (resistors, caps, clamps, driving devices or devices being driven ...). Potentially critical information includes:

\_\_\_\_\_ Input waveform timing relationships

\_\_\_\_\_ Input edge rates

\_\_\_\_\_ Input Overshoot or Undershoot – Magnitude and Duration

\_\_\_\_\_ Output Overshoot or Undershoot – Magnitude and Duration

> Photographs, plots or sketches or relevant inputs and outputs with voltages and time divisions clearly identified for all waveforms are greatly desirable.

> VCC and Ground waveforms should be carefully described as these characteristics vary greatly between applications and test systems. Dynamic characteristics of Ground and VCC during device switching can dramatically effect input and internal operating levels. Ground & VCC measurements should be made as physically close to the device in question as possible.

> Are there specific circumstances that seem to make the questionable unit(s) worse? Better?

\_\_\_\_\_ Temperature \_\_\_\_\_

\_\_\_\_\_ VCC \_\_\_\_\_

\_\_\_\_\_ Input rise/fall time \_\_\_\_\_

\_\_\_\_\_ Output loading (current/capacitance) \_\_\_\_\_

\_\_\_\_\_ Others \_\_\_\_\_

> ATE functional data should include pattern with decoding key and critical parameters such as VCC, input voltages, Func step rate, voltage expected, time to measure.

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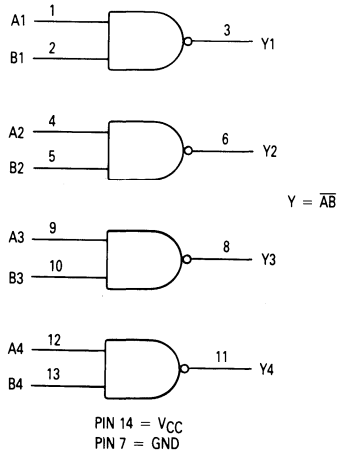
**Data Sheets** **5**

## Quad 2-Input NAND Gate High-Performance Silicon-Gate CMOS

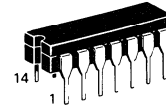
The MC54/74HC00A is identical in pinout to the LS00. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 32 FETs or 8 Equivalent Gates

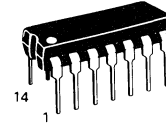
### LOGIC DIAGRAM



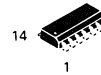
## MC54/74HC00A



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06

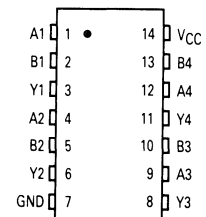


D SUFFIX  
 SOIC  
 CASE 751A-02

### ORDERING INFORMATION

MC74HCXXAN Plastic  
 MC54HCXXAJ Ceramic  
 MC74HCXXAD SOIC  
 T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

# MC54/74HC00A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC00A

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6.0$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V *	pF
		22	

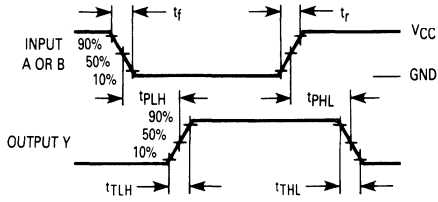
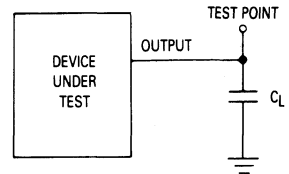


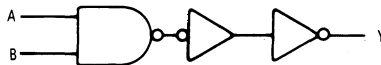
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

## EXPANDED LOGIC DIAGRAM (1/4 of the Device)



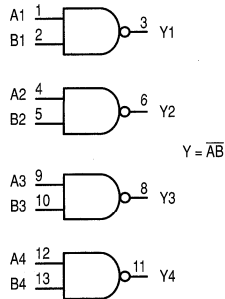
## Quad 2-Input NAND Gate with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT00A may be used as a level converter for interfacing TTL or NMOS outputs to high-speed CMOS inputs.

The HCT00A is identical in pinout to the LS00.

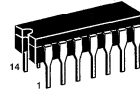
- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates

### LOGIC DIAGRAM

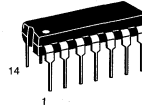


PIN 14 = VCC  
 PIN 7 = GND

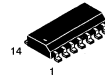
## MC54/74HCT00A



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**

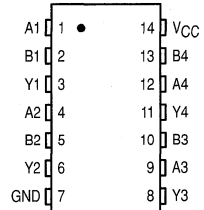


**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

### ORDERING INFORMATION

MC74HCTXXAN	Plastic
MC54HCTXXAJ	Ceramic
MC74HCTXXAD	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

# MC54/74HCT00A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or Plastic DIP) (Ceramic DIP)	260 300	°C °C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS				
Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

DC CHARACTERISTICS FOR THE MC54/74HCT00A (Voltages Referenced to GND)										
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limits						Unit
				25°C to -55°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V I <sub>out</sub> ≤ 20 μA	4.5	2.00		2.00		2.00		V
			5.5	2.00		2.00		2.00		
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V I <sub>out</sub> ≤ 20 μA	4.5		0.80		0.80		0.80	V
			5.5		0.80		0.80		0.80	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>out</sub> ≤ 20 μA	4.5	4.40		4.40		4.40		V
			5.5	5.40		5.40		5.40		
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>out</sub> ≤ 4.0 mA	4.5	3.98		3.84		3.70		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>out</sub> ≤ 20 μA	4.5		0.10		0.10		0.10	V
			5.5		0.10		0.10		0.10	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>out</sub> = 4.0 mA	4.5		0.26		0.33		0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5		±0.10		±1.00		±1.00	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> ≤ 0 μA	5.5		1		10		40	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5		≥ -55°C		25°C to 125°C			
					2.9		2.4			

NOTE: Information on typical parametric values can be found in Chapter 4.

5



# MC54/74HCT00A

AC CHARACTERISTICS FOR THE MC54/74HCT00A ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )									
Symbol	Parameter	Fig.	Guaranteed Limits						Unit
			25°C to -55°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y	1, 2		19		24		28	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output	1, 2		15		19		22	ns
$C_{in}$	Maximum Input Capacitance	—		10		10		10	pF

$C_{PD}$	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$		pF

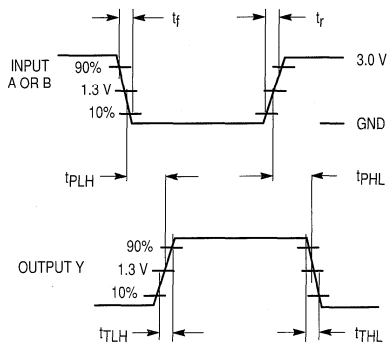
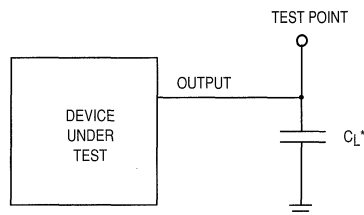


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit



EXPANDED LOGIC DIAGRAM  
(1/4 OF THE DEVICE)

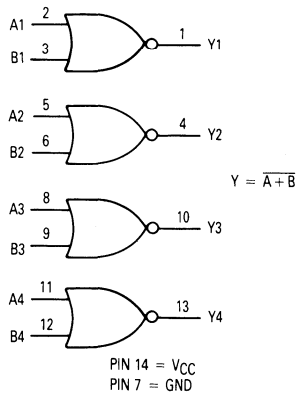
## Quad 2-Input NOR Gate

### High-Performance Silicon-Gate CMOS

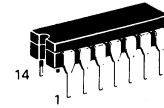
The MC54/74HC02A is identical in pinout to the LS02. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 40 FETs or 10 Equivalent Gates

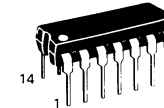
#### LOGIC DIAGRAM



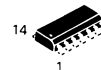
## MC54/74HC02A



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



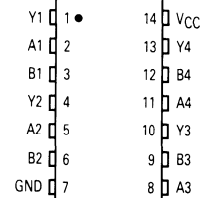
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

#### ORDERING INFORMATION

MC74HCXXAN	Plastic
MC54HCXXAJ	Ceramic
MC74HCXXAD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

# MC54/74HC02A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> = GND I <sub>out</sub> = 0 μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC02A

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6.0$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		22	

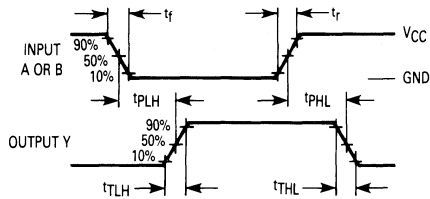
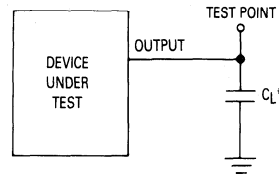


Figure 1. Switching Waveforms

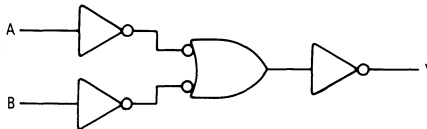


\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

5

## EXPANDED LOGIC DIAGRAM (1/4 of the Device)



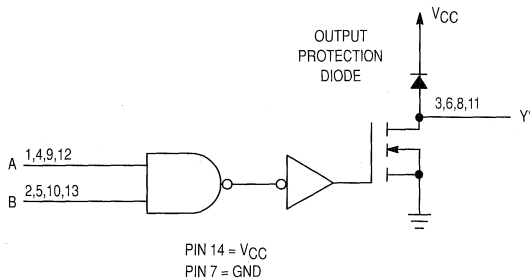
## Quad 2-Input NAND Gate with Open-Drain Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC03A is identical in pinout to the LS03. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC03A NAND gate has, as its output, a high-performance MOS N-Channel transistor. This NAND gate can, therefore, with a suitable pullup resistor, be used in wired-AND applications. Having the output characteristic curves given in this data sheet, this device can be used as an LED driver or in any other application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Outputs Directly Interface to CMOS, NMOS and TTL
- High Noise Immunity Characteristic of CMOS Devices
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 28 FETs or 7 Equivalent Gates

### LOGIC DIAGRAM

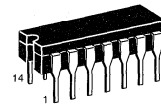


\*Denotes open-drain outputs

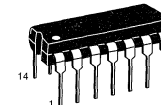
Design Criteria	Value	Unit
Internal Gate Count *	7.0	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	.0075	pJ

\*Equivalent to a two-input NAND gate.

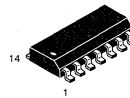
## MC54/74HC03A



**J SUFFIX  
CERAMIC  
CASE 632-08**



**N SUFFIX  
PLASTIC  
CASE 646-06**

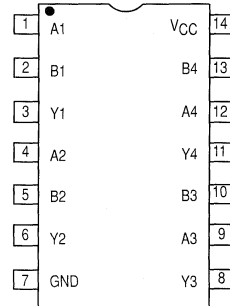


**D SUFFIX  
SOIC  
CASE 751A-02**

### ORDERING INFORMATION

MC74HCXXAN	Plastic
MC54HCXXAJ	Ceramic
MC74HCXXAD	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z = High Impedance

# MC54/74HC03A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C
		300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> ≤ 0 μA	6.0	1.0	10	40	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA

NOTES: Information on typical parametric values along with high frequency or heavy load considerations, can be found in Chapter 4.

5

# MC54/74HC03A

AC ELECTRICAL CHARACTERISTICS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)						
Symbol	Parameter	V <sub>CC</sub> Volts	Temperature Limits for 74HC			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLZ</sub> , t <sub>PZL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance		10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)		10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF	
		8.0				

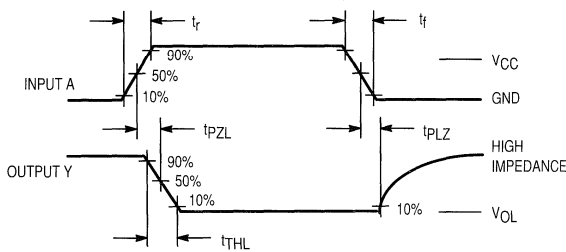
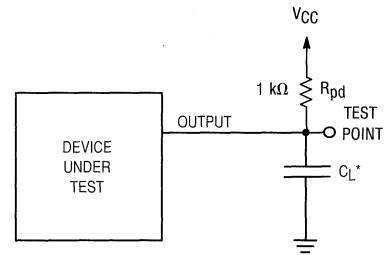
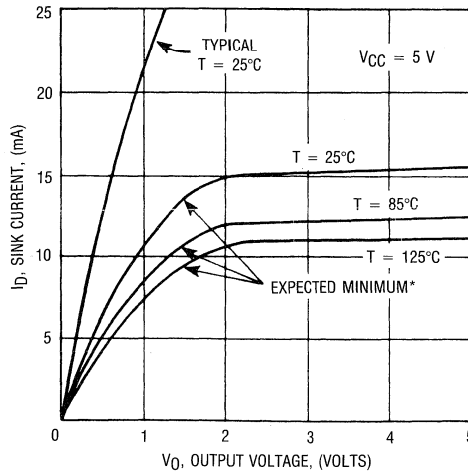


Figure 1. Switching Waveforms



\* Includes all probe and jig capacitance

Figure 2. Test Circuit

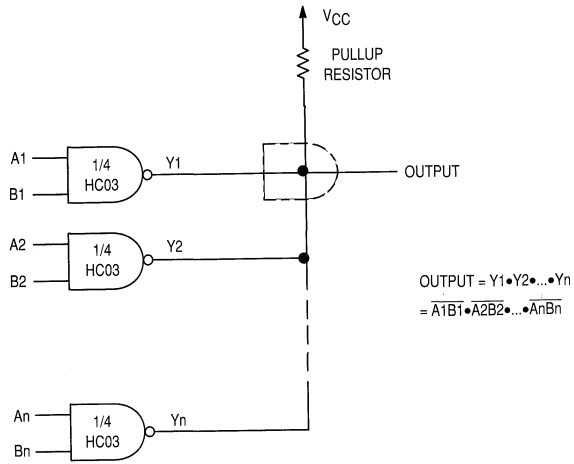


\*The expected minimum curves are not guarantees, but are design aids.

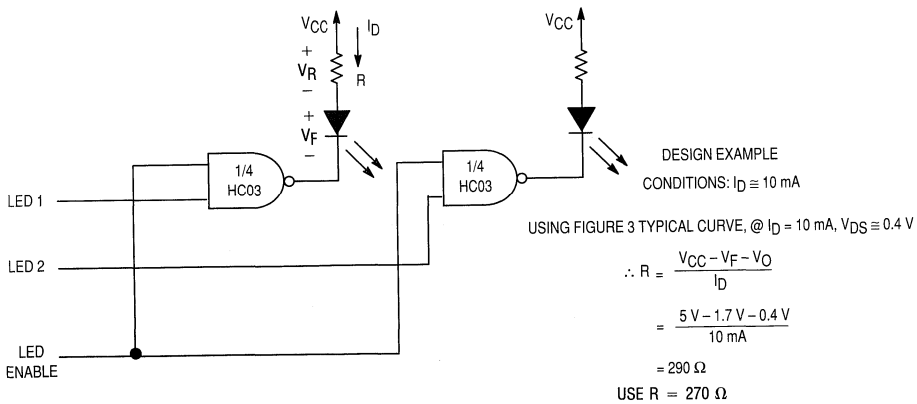
Figure 3. Open-Drain Output Characteristics

# MC54/74HC03A

## Wired AND



## LED Driver with Blanking



5



**MC54/74HC04A**

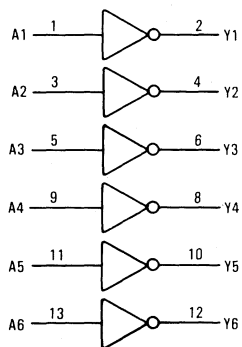
**Hex Inverter**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC04A is identical in pinout to the LS04 and the MC14069. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six three-stage inverters.

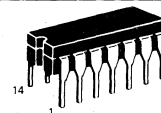
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates

**LOGIC DIAGRAM**

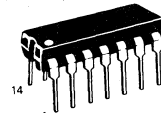


$Y = \bar{A}$

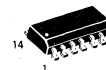
PIN 14 =  $V_{CC}$   
 PIN 7 = GND



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



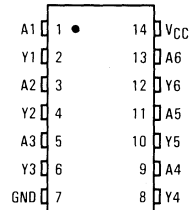
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

**ORDERING INFORMATION**

MC74HCXXAN Plastic  
 MC54HCXXAJ Ceramic  
 MC74HCXXAD SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs A	Outputs Y
L	H
H	L

# MC54/74HC04A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		$V_{in} = V_{IH}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	1	10	40	$\mu\text{A}$

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 4.

# MC54/74HC04A

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		20	

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

## SWITCHING WAVEFORMS

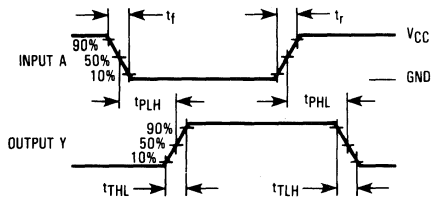
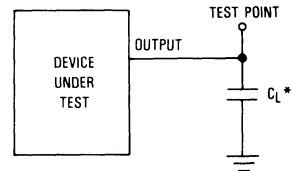


Figure 1



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

## EXPANDED LOGIC DIAGRAM

(1/6 of Device Shown)

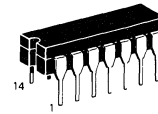


**MC54/74HCT04A**

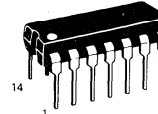
**Hex Inverter with LSTTL-  
 Compatible Inputs**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HCT04A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT04A is identical in pinout to the LS04.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



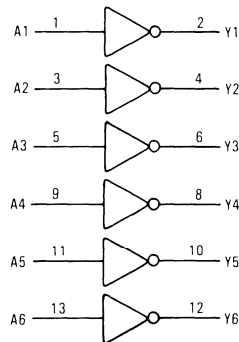
D SUFFIX  
 SOIC  
 CASE 751A-02

**ORDERING INFORMATION**

MC74HCTXXAN	Plastic
MC54HCTXXAJ	Ceramic
MC74HCTXXAD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

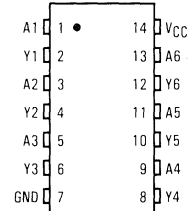
**LOGIC DIAGRAM**



$Y = \bar{A}$

PIN 14 =  $V_{CC}$   
 PIN 7 = GND

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs A	Outputs Y
L	H
H	L

**5**

# MC54/74HCT04A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to +7	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
 Ceramic DIP: - 10 mW/°C from 100° to 125°C  
 SOIC Package: - 7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to - 55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2	2	2	V
			5.5	2	2	2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	4.5	3.98	3.84	3.7	μA
			5.5	0.26	0.33	0.4	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	± 0.1	± 1	± 1	μA
			5.5	1	10	40	

ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	≥ - 55°C		25°C to 125°C	mA
			2.9	2.4		
5.5						

### NOTES:

- Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 4.
- Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

5

# MC54/74HCT04A

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$t_{PLH}$	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	15	19	22	ns
$t_{PHL}$		17	21	26	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5 \text{ V}$	pF
		22	

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

## SWITCHING WAVEFORMS

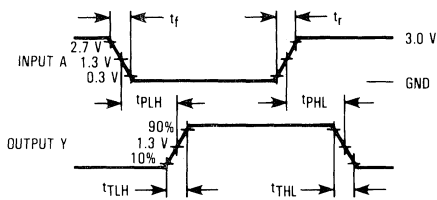
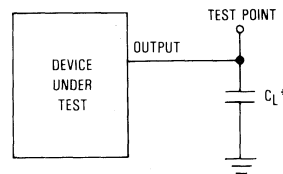


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

5

## EXPANDED LOGIC DIAGRAM

(1/6 of Device Shown)



## Hex Unbuffered Inverter

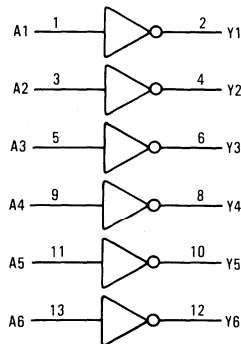
### High Performance Silicon-Gate CMOS

The MC54/74HCU04 is identical in pinout to the LSO4 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single-stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high-input impedance amplifier. For digital applications, the HC04 is recommended.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V; 2.5 to 6 V in Oscillator Configurations
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 12 FETs or 3 Equivalent Gates

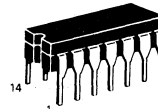
#### LOGIC DIAGRAM



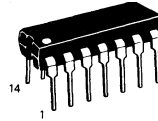
$$Y = \bar{A}$$

PIN 14 =  $V_{CC}$   
 PIN 7 = GND

## MC54/74HCU04



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



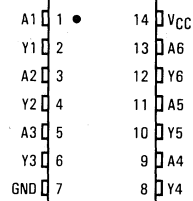
D SUFFIX  
 SOIC  
 CASE 751A-02

#### ORDERING INFORMATION

MC74HCUXN	Plastic
MC54HCUXJ	Ceramic
MC74HCUXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs A	Outputs Y
L	H
H	L

# MC54/74HCU04

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	—	No Limit	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.5 \text{ V}^*$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.7	1.7	1.7	V
			4.5	3.6	3.6	3.6	
			6.0	4.8	4.8	4.8	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.5 \text{ V}^*$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.8	0.8	0.8	
			6.0	1.1	1.1	1.1	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = \text{GND}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.8	1.8	1.8	V
			4.5	4.0	4.0	4.0	
		$V_{in} = \text{GND}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	6.0	5.5	5.5	5.5	
			6.0	3.86	3.76	3.70	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{CC}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.2	0.2	0.2	V
			4.5	0.5	0.5	0.5	
		$V_{in} = V_{CC}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	6.0	0.5	0.5	0.5	
			6.0	0.32	0.37	0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 4.

\*For  $V_{CC} = 2.0 \text{ V}$ ,  $V_{out} = 0.2 \text{ V}$  or  $V_{CC} - 0.2 \text{ V}$ .

5



# MC54/74HCU04

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		15	

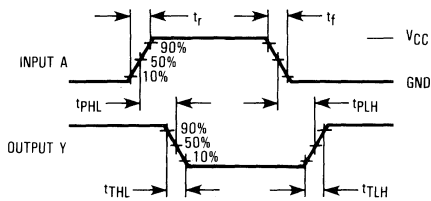
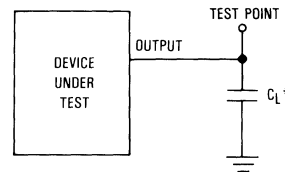


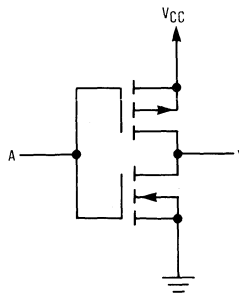
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

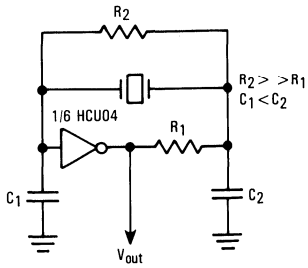
### LOGIC DETAIL (1/6 of Device Shown)



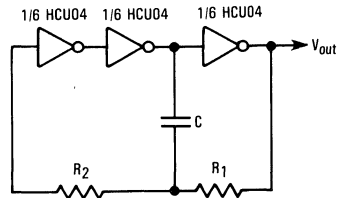
# MC54/74HCU04

## TYPICAL APPLICATIONS

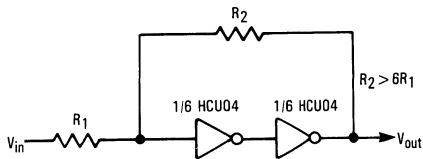
### Crystal Oscillator



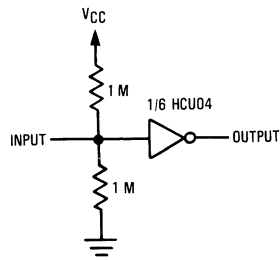
### Stable RC Oscillator



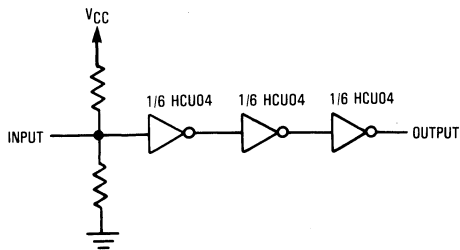
### Schmitt Trigger



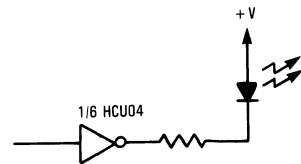
### High Input Impedance Single-Stage Amplifier with a 2 to 6 V Supply Range



### Multi-Stage Amplifier



### LED Driver



For reduced power supply current, use high-efficiency LEDs such as the Hewlett-Packard HLMP series or equivalent.

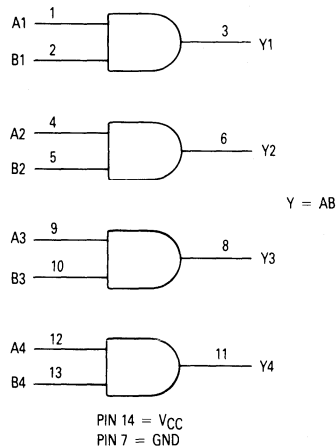
## Quad 2-Input AND Gate

### High-Performance Silicon-Gate CMOS

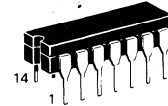
The MC54/74HC08A is identical in pinout to the LS08. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 24 FETs or 6 Equivalent Gates

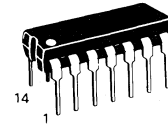
#### LOGIC DIAGRAM



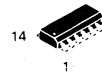
## MC54/74HC08A



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



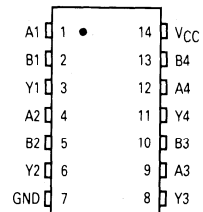
D SUFFIX  
 SOIC  
 CASE 751A-02

#### ORDERING INFORMATION

MC74HCXXAN Plastic  
 MC54HCXXAJ Ceramic  
 MC74HCXXAD SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

# MC54/74HC08A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	5.9	5.9	5.9	
			6.0	3.98	3.84	3.7	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC08A

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		20	

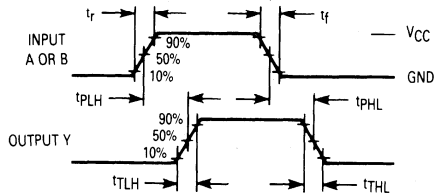
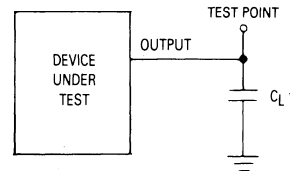


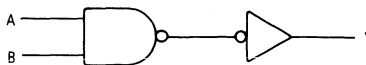
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

## EXPANDED LOGIC DIAGRAM (1/4 of the Device)



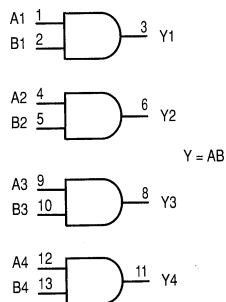
## Quad 2-Input AND Gate with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT08A may be used as a level converter for interfacing TTL or NMOS outputs to high-speed CMOS inputs.

The HCT08A is identical in pinout to the LS08.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 40 FETs or 10 Equivalent Gates

### LOGIC DIAGRAM

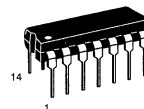


PIN 14 = V<sub>CC</sub>  
PIN 7 = GND

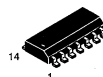
## MC54/74HCT08A



**J SUFFIX  
CERAMIC  
CASE 632-08**



**N SUFFIX  
PLASTIC  
CASE 646-06**

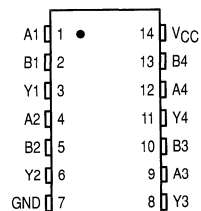


**D SUFFIX  
SOIC  
CASE 751A-02**

### ORDERING INFORMATION

MC74HCTXXAN	Plastic
MC54HCTXXAJ	Ceramic
MC74HCTXXAD	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

# MC54/74HCT08A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or Plastic DIP) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS				
Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

DC CHARACTERISTICS FOR THE MC54/74HCT08A (Voltages Referenced to GND)										
Symbol	Parameter	Test Conditions	V <sub>CC</sub> Volts	Guaranteed Limits						Unit
				25°C to -55°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	2.00 2.00		2.00 2.00		2.00 2.00	V	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5		0.80 0.80		0.80 0.80	0.80 0.80	V	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	4.40 5.40		4.40 5.40		4.40 5.40	V	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0 mA	4.5	3.98		3.84		3.70		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5		0.10 0.10		0.10 0.10	0.10 0.10	V	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0 mA	4.5		0.26		0.33	0.40		
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5		±0.10		±1.00	±1.00	μA	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>IN</sub> = V <sub>CC</sub> or GND  I <sub>OUT</sub>   ≤ 0 μA	5.5		1		10	40	μA	
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>IN</sub> = 2.4 V, Any One Input V <sub>IN</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C		25°C to 125°C				
					2.9		2.4		mA	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HCT08A

AC CHARACTERISTICS FOR THE MC54/74HCT08A ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6.0 \text{ ns}$ )									
Symbol	Parameter	Fig.	Guaranteed Limits						Unit
			25°C to -55°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y	1, 2		19		24		28	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output	1, 2		15		19		22	ns
$C_{in}$	Maximum Input Capacitance	—		10		10		10	pF
$C_{PD}$	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$						pF	
		20							

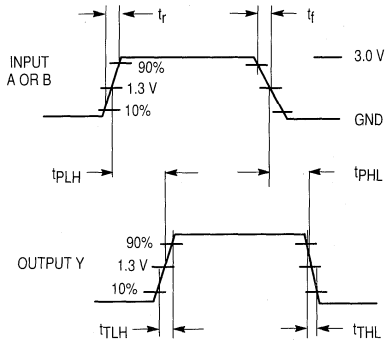
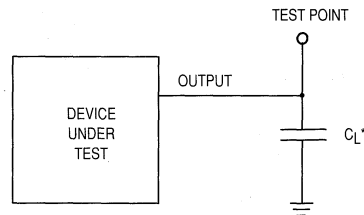


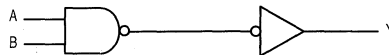
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

5



EXPANDED LOGIC DIAGRAM  
(1/4 OF THE DEVICE)

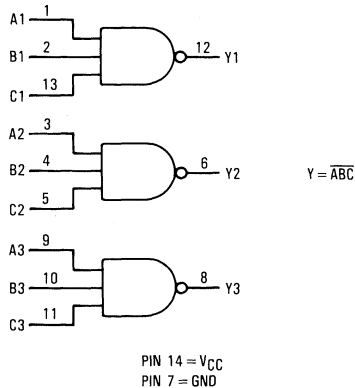


## Triple 3-Input NAND Gate High-Performance Silicon-Gate CMOS

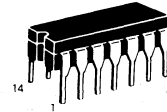
The MC54/74HC10 is identical in pinout to the LS10. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates

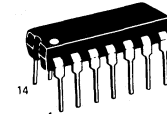
### LOGIC DIAGRAM



## MC54/74HC10



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



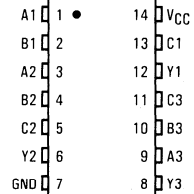
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

### ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs			Output
A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

# MC54/74HC10

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750	mW
		500	
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C
		300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	5.9	5.9	5.9	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC10

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

$C_{PD}$	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		25	

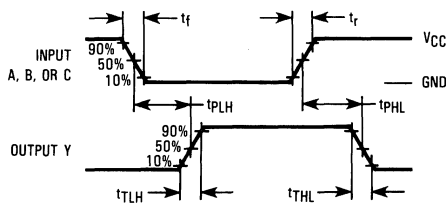
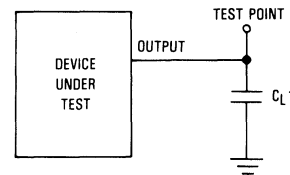


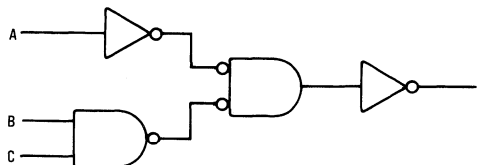
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM (1/3 of the Device)



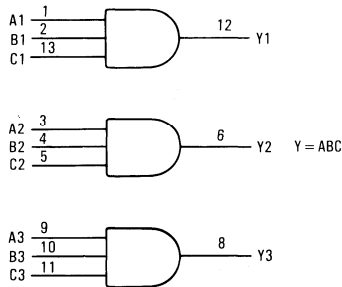
## Triple 3-Input AND Gate

### High-Performance Silicon-Gate CMOS

The MC54/74HC11 is identical in pinout to the LS11. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

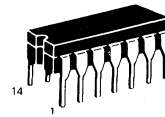
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates

#### LOGIC DIAGRAM

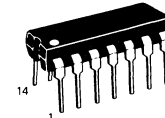


PIN 14 = V<sub>CC</sub>  
 PIN 7 = GND

## MC54/74HC11



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



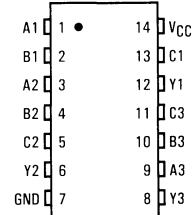
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

#### ORDERING INFORMATION

MC74HCXXN Plastic  
 MC54HCXXJ Ceramic  
 MC74HCXXD SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs			Output
A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

# MC54/74HC11

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μA
			6.0	±0.1	±1.0	±1.0	

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC11

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

$C_{PD}$	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		27	

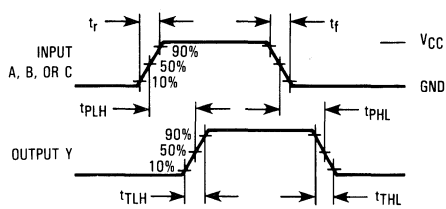
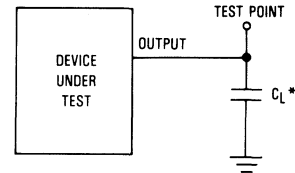


Figure 1. Switching Waveforms

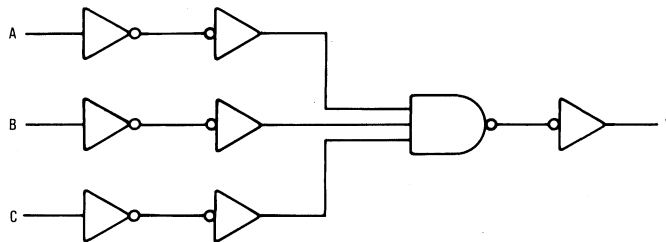


\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

5

### EXPANDED LOGIC DIAGRAM ( $\frac{1}{2}$ of the Device)



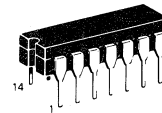
**MC54/74HC14A**

**Hex Schmitt-Trigger Inverter**  
**High-Performance Silicon-Gate CMOS**

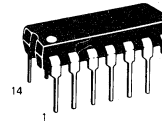
The MC54/74HC14A, is identical in pinout to the LS14, LS04, and HC04. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC14A is useful to "square up" slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HC14A finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



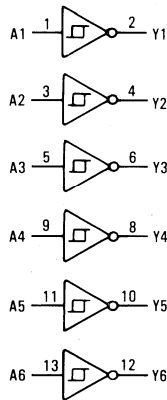
D SUFFIX  
 SOIC  
 CASE 751A-02

**ORDERING INFORMATION**

MC74HCXXAN	Plastic
MC54HCXXAJ	Ceramic
MC74HCXXAD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

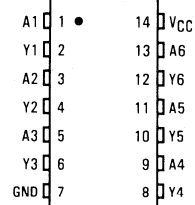
**LOGIC DIAGRAM**



$Y = \bar{A}$

PIN 14 =  $V_{CC}$   
 PIN 7 = GND

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Input	Output
A	Y
L	H
H	L

# MC54/74HC14A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\* This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2	6	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	-	No Limit*	ns

\*When V<sub>in</sub> ≈ 50% V<sub>CC</sub>, I<sub>CC</sub> > 1 mA.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6	4.2	4.2	4.2	
V <sub>T+</sub> min	Minimum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2	1	0.95	0.95	V
			4.5	2.3	2.25	2.25	
			6	3	2.95	2.95	
V <sub>T-</sub> max	Maximum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2	0.9	0.95	0.95	V
			4.5	2	2.05	2.05	
			6	2.6	2.65	2.65	
V <sub>T-</sub> min	Minimum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6	1.2	1.2	1.2	
V <sub>H</sub> max Note 2	Maximum Hysteresis Voltage (Figure 3)	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2	1.2	1.2	1.2	V
			4.5	2.25	2.25	2.25	
			6	3	3	3	
V <sub>H</sub> min Note 2	Minimum Hysteresis Voltage (Figure 3)	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2	0.2	0.2	0.2	V
			4.5	0.4	0.4	0.4	
			6	0.5	0.5	0.5	

### NOTES:

- Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 4.
- V<sub>H</sub> min = (V<sub>T+</sub> min) - (V<sub>T-</sub> max); V<sub>H</sub> max = (V<sub>T+</sub> max) - (V<sub>T-</sub> min).

5



# MC54/74HC14A

## DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> ≤ V <sub>T- min</sub>  I <sub>out</sub>   ≤ 20 μA	2 4.5 6	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V <sub>in</sub> ≤ V <sub>T- min</sub>  I <sub>out</sub>   ≤ 4 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5 6	3.98 5.48	3.84 5.34	3.7 5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> ≥ V <sub>T+ max</sub>  I <sub>out</sub>   ≤ 20 μA	2 4.5 6	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>in</sub> ≥ V <sub>T+ max</sub>  I <sub>out</sub>   ≤ 4 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5 6	0.26 0.26	0.33 0.33	0.4 0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6	±0.1	±1	±1	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6	1	10	40	μA

NOTE: 1. V<sub>Hmin</sub> > (V<sub>T+ min</sub>) - (V<sub>T- max</sub>); V<sub>Hmax</sub> = (V<sub>T+ max</sub>) - (V<sub>T- min</sub>).

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2	95	120	145	ns
		4.5	19	24	29	
		6	16	20	25	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2	75	95	110	ns
		4.5	15	19	22	
		6	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical @ 25°C, V <sub>CC</sub> = 5 V	pF
		22	

NOTE: 1. For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

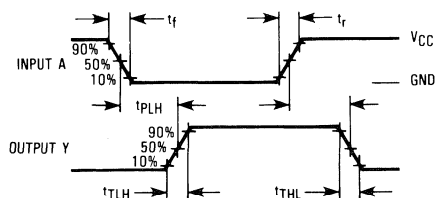
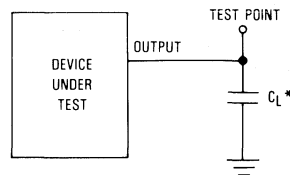


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

5

# MC54/74HC14A

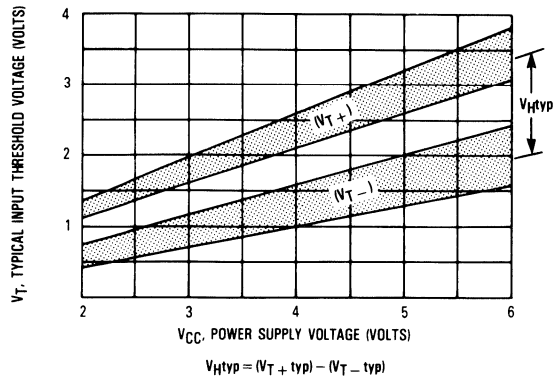


Figure 3. Typical Input Threshold,  $V_{T+}$ ,  $V_{T-}$  Versus Power Supply Voltage

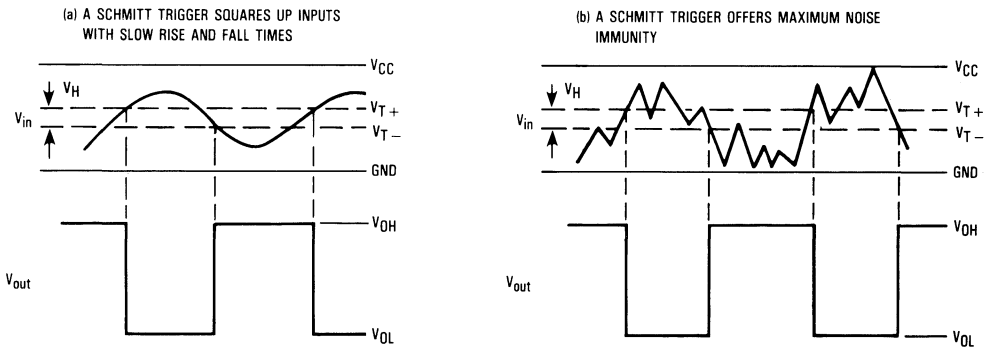


Figure 4. Typical Schmitt-Trigger Applications

5

## Hex Schmitt-Trigger Inverter with LSTTL Compatible Inputs

### High-Performance Silicon-Gate CMOS

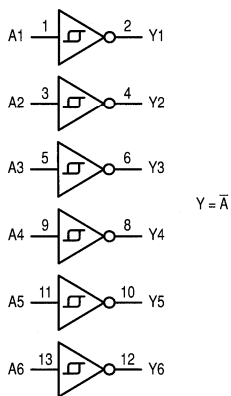
The MC54/74HCT14A may be used as a level converter for interfacing TTL or NMOS outputs to high-speed CMOS inputs.

The HCT14A is identical in pinout to the LS14.

The HCT14A is useful to "square up" slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HCT14A finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

#### LOGIC DIAGRAM

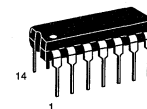


PIN 14 = VCC  
 PIN 7 = GND

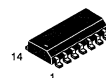
## MC54/74HCT14A



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**

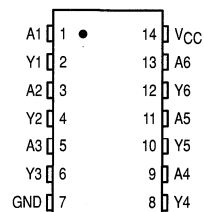


**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

#### ORDERING INFORMATION

MC74HCTXXAN	Plastic
MC54HCTXXAJ	Ceramic
MC74HCTXXAD	SOIC

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

**5**

# MC54/74HCT14A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C
		300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS				
Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	—	*	ns

\* No Limit when V<sub>in</sub> = 50% V<sub>CC</sub>, I<sub>CC</sub> > 1.0 mA.

## DC CHARACTERISTICS FOR THE MC74/54HCT14A

Symbol	Parameter	Test Conditions	V <sub>CC</sub> Volts	Temperature Limits						Unit
				25°C to -55°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
VT+max	Maximum Positive-Going Input Threshold Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5		1.9		1.9		1.9	V
			5.5		2.1		2.1		2.1	
VT+min	Minimum Positive-Going Input Threshold Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5	1.2		1.2		1.2		V
			5.5	1.4		1.4		1.4		
VT-max	Maximum Negative-Going Input Threshold Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   < 20 μA	4.5		1.2		1.2		1.2	
			5.5		1.4		1.4		1.4	
VT-min	Minimum Negative-Going Input Threshold Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   < 20 μA	4.5	0.5		0.5		0.5		
			5.5	0.6		0.6		0.6		
V <sub>H</sub> max	Maximum Hysteresis Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   < 20 μA	4.5		1.4		1.4		1.4	
			5.5		1.5		1.5		1.5	
V <sub>H</sub> min	Minimum Hysteresis Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   < 20 μA	4.5	0.4		0.4		0.4		
			5.5	0.4		0.4		0.4		
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> < VT-min  I <sub>OUT</sub>   ≤ 20 μA	4.5	4.4		4.4		4.4	V	
			5.5	5.4		5.4		5.4		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> < VT-min  I <sub>OUT</sub>   ≤ 20 μA	4.5		0.1		0.1		0.1	V
			5.5		0.1		0.1		0.1	
			4.5		0.26		0.33		0.4	

NOTE: Information on typical parametric values can be found in Chapter 4.

(continued)

# MC54/74HCT14A

DC CHARACTERISTICS FOR THE MC74/54HCT14A — continued											
Symbol	Parameter	Test Conditions	V <sub>CC</sub> Volts	Temperature Limits						Unit	
				25°C to -55°C		≤ 85°C		≤ 125°C			
				Min	Max	Min	Max	Min	Max		
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±1.0	μA	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	5.5		1.0		10		40	μA	
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5		≥ -55°C		25°C to 125°C				mA
					2.9	2.4					

AC CHARACTERISTICS FOR THE MC74/54HCT14A										
Symbol	Parameter	Test Conditions	Fig.	Temperature Limits						Unit
				25°C to -55°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (L to H)	V <sub>CC</sub> = 5.0 V ±10% C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns	Fig. 1 & 2		32		40		48	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output	V <sub>CC</sub> = 5.0 V ±10% C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns	Fig. 1 & 2		15		19		22	ns

C <sub>PD</sub>	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical @ 25°C, V <sub>CC</sub> = 5.0 V		pF
		32		

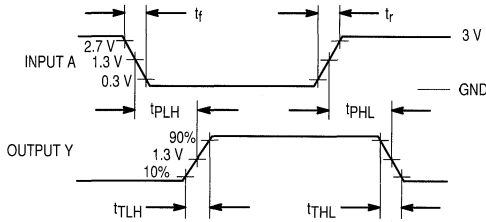
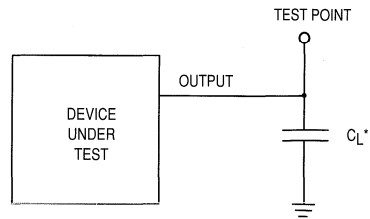


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

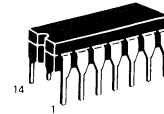
Figure 2. Test Circuit

## Dual 4-Input NAND Gate High-Performance Silicon-Gate CMOS

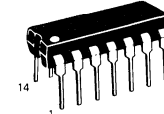
The MC54/74HC20 is identical in pinout to the LS20. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 28 FETs or 7 Equivalent Gates

### MC54/74HC20



**J SUFFIX  
 CERAMIC  
 CASE 632-08**



**N SUFFIX  
 PLASTIC  
 CASE 646-06**



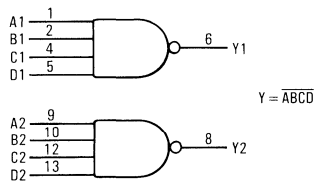
**D SUFFIX  
 SOIC  
 CASE 751A-02**

#### ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

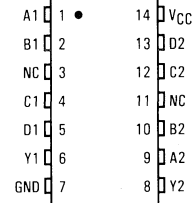
$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



PIN 14 =  $V_{CC}$   
 PIN 7 = GND  
 PINS 3, 11 = NO CONNECTION

#### PIN ASSIGNMENT



NC = NO CONNECTION

#### FUNCTION TABLE

Inputs				Output
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

**5**

# MC54/74HC20

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC20

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A, B, C, or D to Output Y (Figures 1 and 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0$ V	
			26

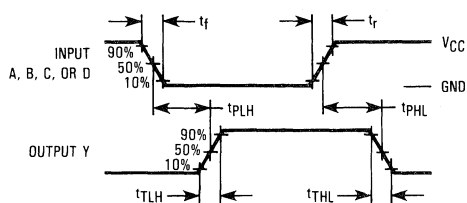
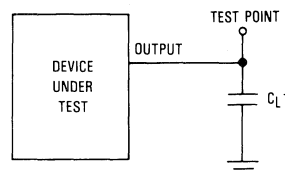


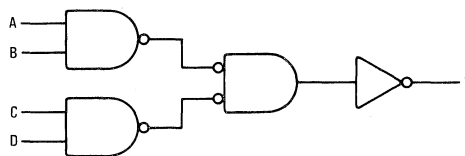
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM (1/2 of the Device)



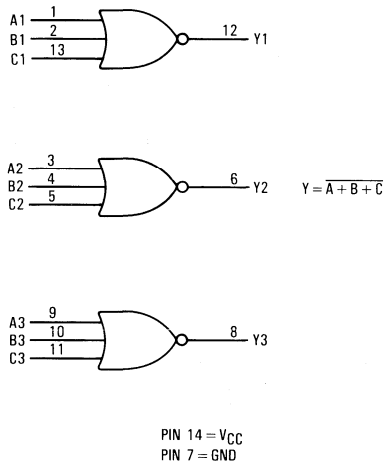


## Triple 3-Input NOR Gate High-Performance Silicon-Gate CMOS

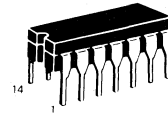
The MC54/74HC27 is identical in pinout to the LS27. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates

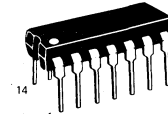
### LOGIC DIAGRAM



## MC54/74HC27



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



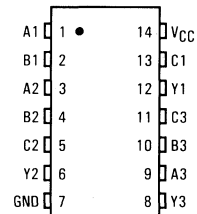
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

### ORDERING INFORMATION

MC74HCXXN Plastic  
 MC54HCXXJ Ceramic  
 MC74HCXXD SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs			Output
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

# MC54/74HC27

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC27

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		27	

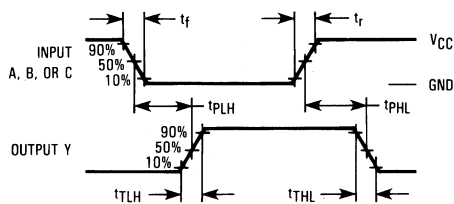
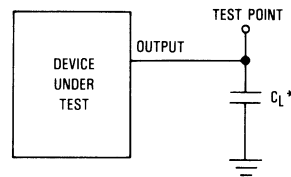


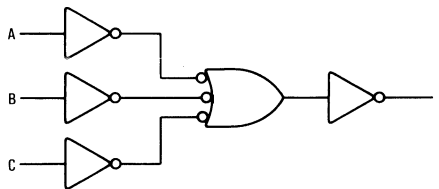
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM (1/2 of the Device)



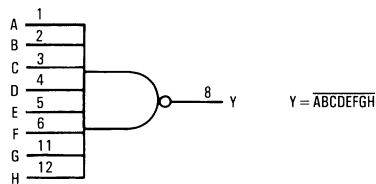
## 8-Input NAND Gate

### High-Performance Silicon-Gate CMOS

The MC54/74HC30 is identical in pinout to the LS30. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 32 FETs or 8 Equivalent Gates

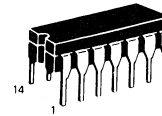
#### LOGIC DIAGRAM



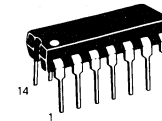
PINS 9, 10, 13 = NO CONNECTION

PIN 14 =  $V_{CC}$   
 PIN 7 = GND

## MC54/74HC30



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



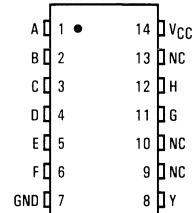
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

#### ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



NC = NO CONNECTION

#### FUNCTION TABLE

Inputs A through H	Output Y
All inputs H	L
One or more inputs L	H

# MC54/74HC30

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	0.1	0.1	0.1	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	± 0.1	± 1.0	± 1.0	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC30

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		27	

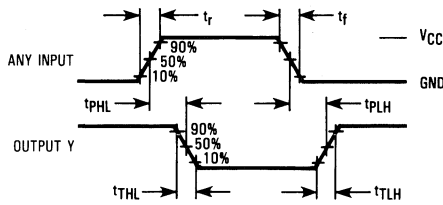
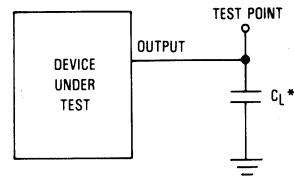


Figure 1. Switching Waveforms

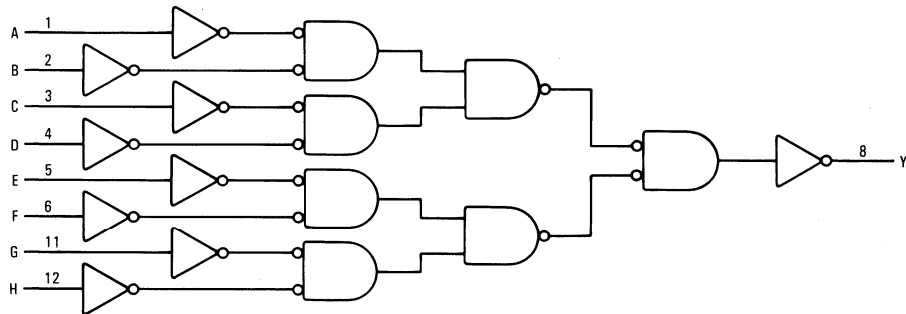


\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

5

### EXPANDED LOGIC DIAGRAM

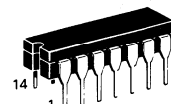


**MC54/74HC32A**

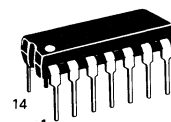
**Quad 2-Input OR Gate**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC32A is identical in pinout to the LS32. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

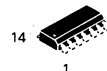
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



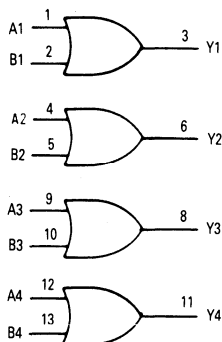
D SUFFIX  
 SOIC  
 CASE 751A-02

**ORDERING INFORMATION**

MC74HCXXAN Plastic  
 MC54HCXXAJ Ceramic  
 MC74HCXXAD SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

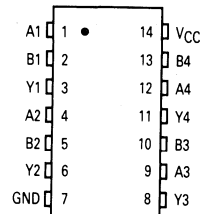
**LOGIC DIAGRAM**



$Y = A + B$

PIN 14 =  $V_{CC}$   
 PIN 7 = GND

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

# MC54/74HC32A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5



# MC54/74HC32A

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6.0$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		20	

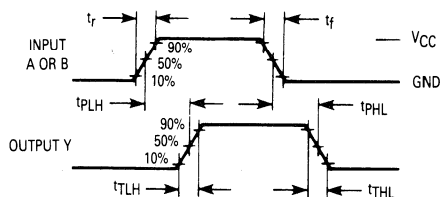


Figure 1. Switching Waveforms

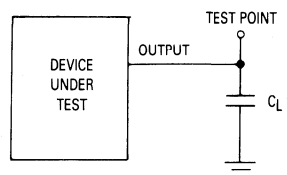
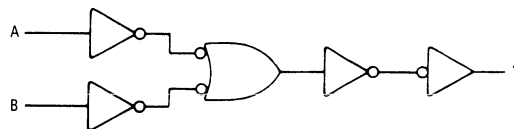


Figure 2. Test Circuit



EXPANDED LOGIC DIAGRAM  
(1/4 of the Device)

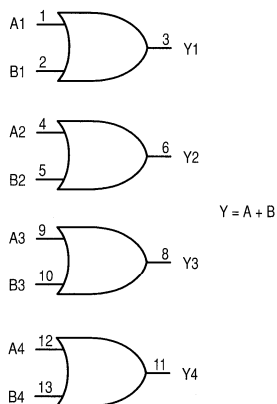
## Quad 2-Input OR Gate with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT32A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT32A is identical in pinout to the LS32.

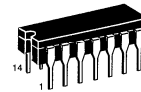
- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 64 FETs or 16 Equivalent Gates

### LOGIC DIAGRAM

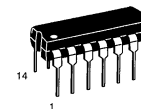


PIN 14 =  $V_{CC}$   
PIN 7 = GND

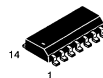
## MC54/74HCT32A



**J SUFFIX  
CERAMIC  
CASE 632-08**



**N SUFFIX  
PLASTIC  
CASE 646-06**

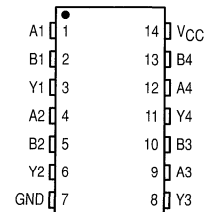


**D SUFFIX  
SOIC  
CASE 751A-02**

### ORDERING INFORMATION

MC74HCTXXAN	Plastic
MC54HCTXXAJ	Ceramic
MC74HCTXXAD	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

# MC54/74HCT32A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or Plastic DIP) (Ceramic DIP)	260	°C
		300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND < (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS				
Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

DC CHARACTERISTICS FOR THE MC54/74HCT32A (Voltages Referenced to GND)											
Symbol	Parameter	Test Conditions	V <sub>CC</sub> Volts	Guaranteed Limits						Unit	
				25°C to -55°C		≤ 85°C		≤ 125°C			
				Min	Max	Min	Max	Min	Max		
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	2.0 2.0		2.0 2.0		2.0 2.0		V	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5		0.8 0.8		0.8 0.8		0.8 0.8	V	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0 mA	5.5	3.98		3.84		3.7			
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1	V	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0 mA	4.5		0.26		0.33		0.4		
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±1.0	μA	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> ≤ 0 μA	5.5		1.0		10		40	μA	
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5		≥ -55°C		25°C to 125°C				
					2.9	2.4			mA		

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HCT32A

AC CHARACTERISTICS FOR THE MC54/74HCT32A ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )									
Symbol	Parameter	Fig.	Guaranteed Limits						Unit
			25°C to -55°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y	1, 2		20		25		30	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output	1, 2		15		19		22	ns
$C_{in}$	Maximum Input Capacitance			10		10		10	pF

$C_{PD}$	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$		pF
		15		

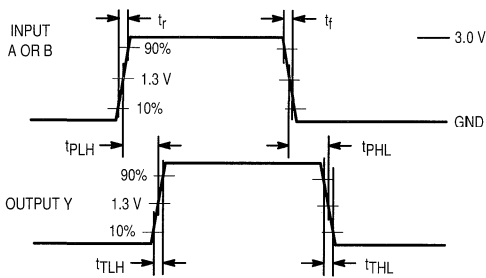
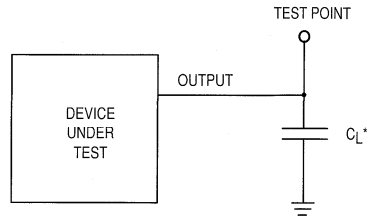


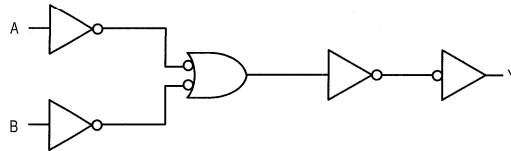
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

5



EXPANDED LOGIC DIAGRAM  
(1/4 OF THE DEVICE)

# 1-of-10 Decoder

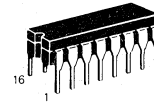
## High-Performance Silicon-Gate CMOS

The MC54/74HC42 is identical in pinout to the LS42. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

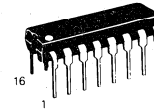
The HC42 decodes a BCD Address to one-of-ten active-low outputs. For Address inputs with a hexadecimal equivalent greater than 9, all outputs, Y0-Y9, remain high (inactive).

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 104 FETs or 26 Equivalent Gates

### MC54/74HC42



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



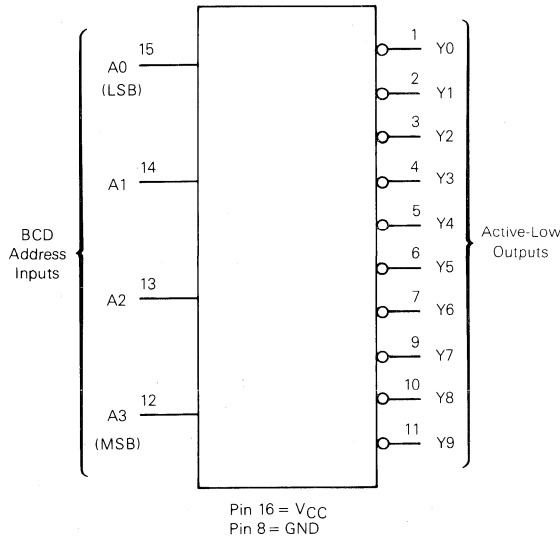
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

#### ORDERING INFORMATION

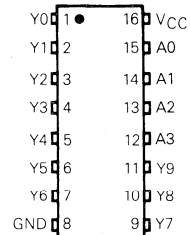
MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT



# MC54/74HC42

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC42

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		65	

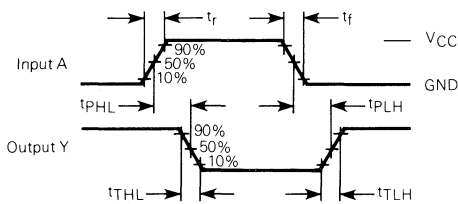
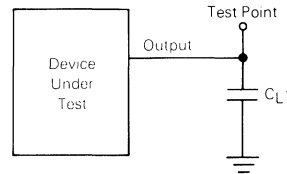


Figure 1. Switching Waveforms



\* Includes all probe and jig capacitance.

Figure 2. Test Circuit

## FUNCTION TABLE

Inputs				Outputs									
A3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	H	H	H	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	H	H	L
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

# MC54/74HC42

## PIN DESCRIPTIONS

### INPUTS

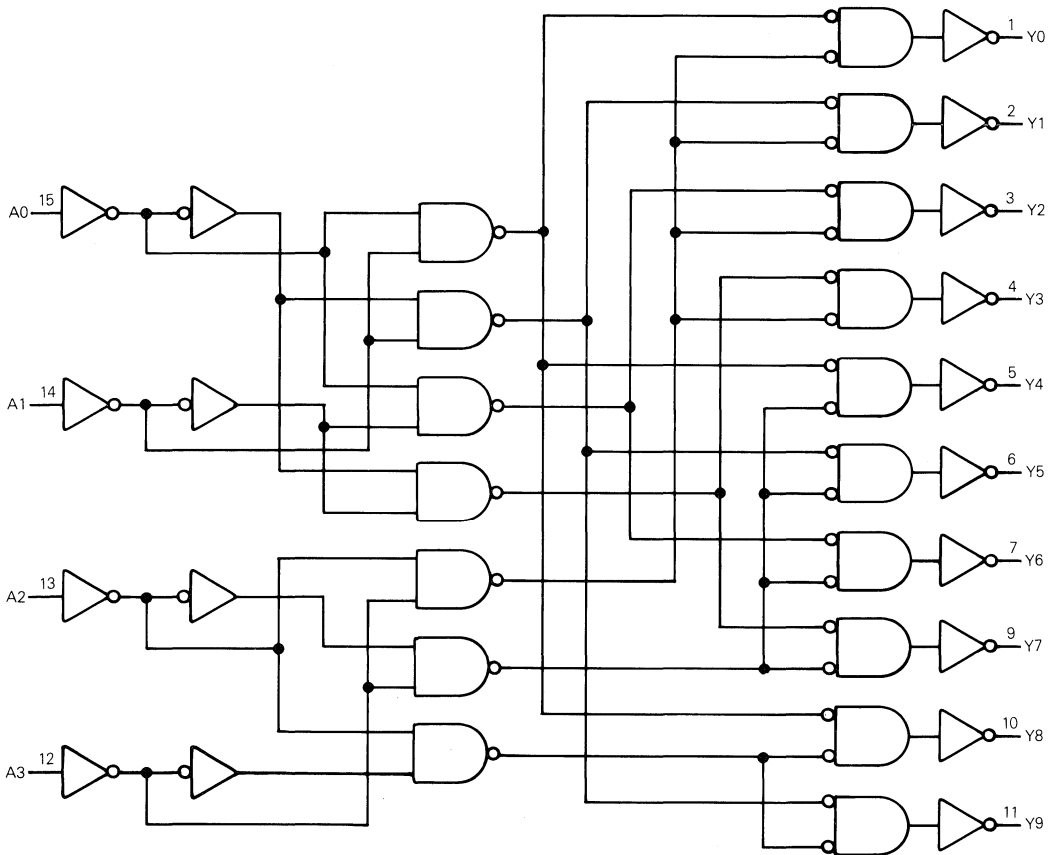
A0, A1, A2, A3, (PINS 15, 14, 13, 12) — BCD Address Inputs. The BCD address present at these inputs determines which output is active-low. These inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. Addresses with a hexadecimal equivalent

number greater than nine are not decoded.

### OUTPUTS

Y0-Y9 (PINS 1-7, 9-11) — Active-Low Decoded Outputs. These outputs assume a low level when addressed and remain high when not addressed.

## EXPANDED LOGIC DIAGRAM





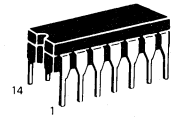
## 2-Wide, 2-Input/2-Wide, 3-Input AND-NOR Gates

### High-Performance Silicon-Gate CMOS

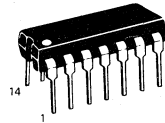
The MC54/74HC51 is identical in pinout to the LS51. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates

## MC54/74HC51



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



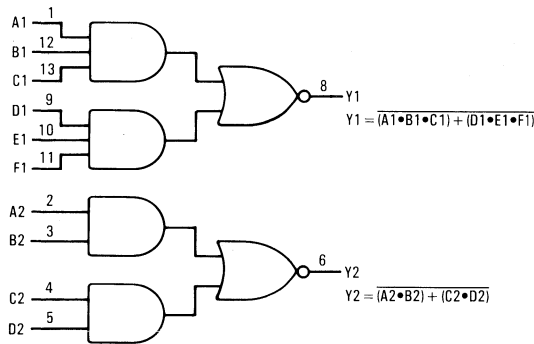
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

### ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

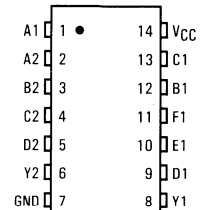
$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### LOGIC DIAGRAM



PIN 14 =  $V_{CC}$   
 PIN 7 = GND

### PIN ASSIGNMENT



### FUNCTION TABLES

Inputs						Output
A1	B1	C1	D1	E1	F1	Y1
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

Inputs				Output
A2	B2	C2	D2	Y2
H	H	X	X	L
X	X	H	H	L
All other combinations				H

# MC54/74HC51

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40		
		6.0	0.26	0.33	0.40		
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC51

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Section) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	

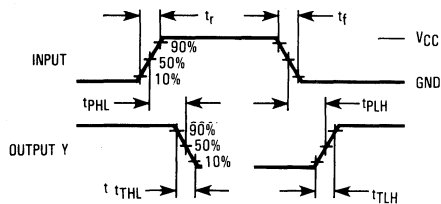
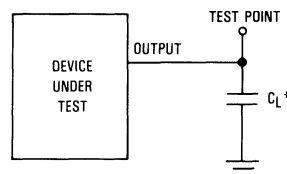


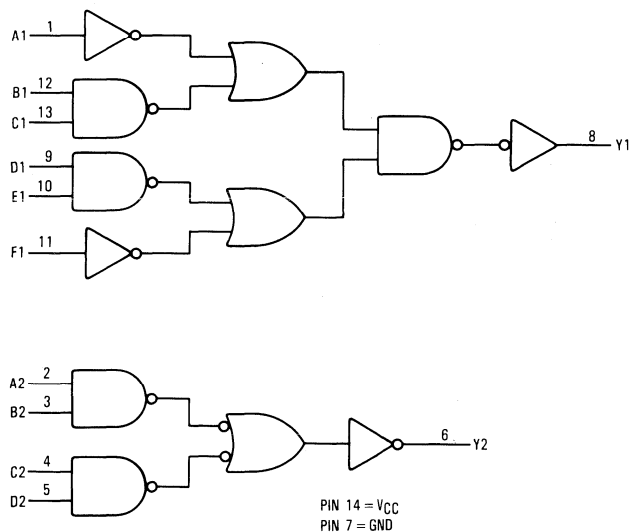
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM



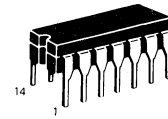
## 2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates

### High-Performance Silicon-Gate CMOS

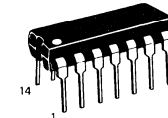
The MC54/74HC58 is identical to the MC54/74HC51 except that the outputs are inverted. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates

### MC54/74HC58



**J SUFFIX  
 CERAMIC  
 CASE 632-08**



**N SUFFIX  
 PLASTIC  
 CASE 646-06**



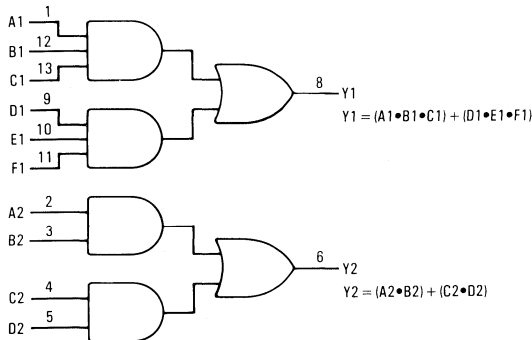
**D SUFFIX  
 SOIC  
 CASE 751A-02**

#### ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

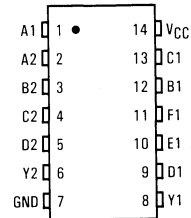
$T_A = -55^\circ$  to  $125^\circ$ C for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



PIN 14 =  $V_{CC}$   
 PIN 7 = GND

#### PIN ASSIGNMENT



#### FUNCTION TABLES

Inputs						Output
A1	B1	C1	D1	E1	F1	Y1
H	H	H	X	X	X	H
X	X	X	H	H	H	H
Any other combination						L

Inputs				Output
A2	B2	C2	D2	Y2
H	H	X	X	H
X	X	H	H	H
Any other combination				L

# MC54/74HC58

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
6.0	5.48	5.34	5.20				
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
6.0	0.26	0.33	0.40				
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC58

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Section) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		22	

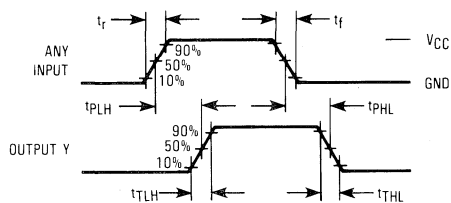
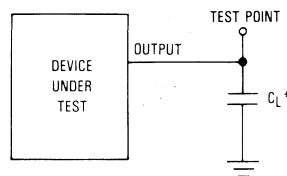


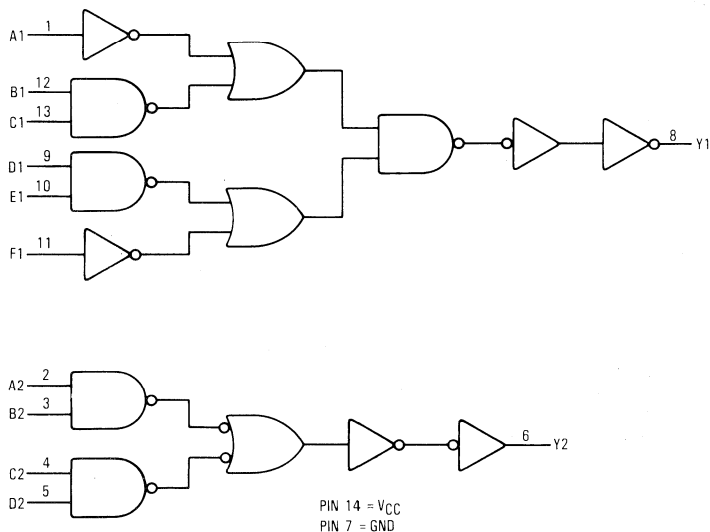
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM



PIN 14 = V<sub>CC</sub>  
PIN 7 = GND

## Dual J-K Flip-Flop with Reset

### High-Performance Silicon-Gate CMOS

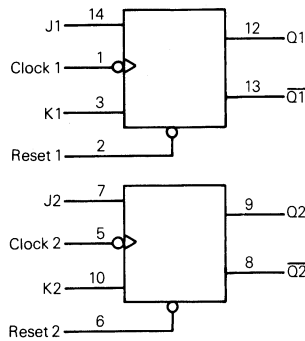
The MC54/74HC73 is identical in pinout to the LS73. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has an active-low asynchronous reset.

The MC54/74HC73 is identical in function to the HC107, but has a different pinout.

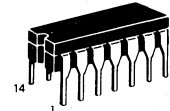
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates

#### LOGIC DIAGRAM

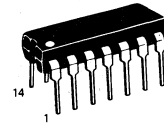


Pin 4 = V<sub>CC</sub>  
 Pin 11 = GND

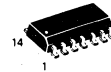
## MC54/74HC73



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



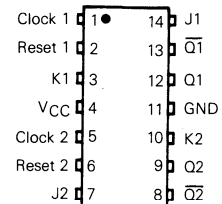
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

#### ORDERING INFORMATION

MC74HCXXD SOIC  
 MC74HCXXN Plastic  
 MC54HCXXJ Ceramic

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs				Outputs	
Reset	Clock	J	K	Q	Q̄
L	X	X	X	L	H
H		L	L	No Change	
H		L	H	L	H
H		H	L	H	L
H		H	H	Toggle	
H	L	X	X	No Change	
H	H	X	X	No Change	
H		X	X	No Change	

# MC54/74HC73

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C
		300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	5.9	5.9	5.9	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HC73

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figures 1 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q or $\bar{Q}$ (Figures 2 and 4)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC73

## SWITCHING WAVEFORMS

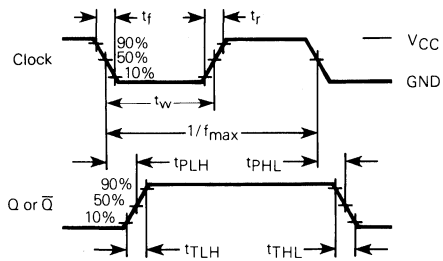


Figure 1.

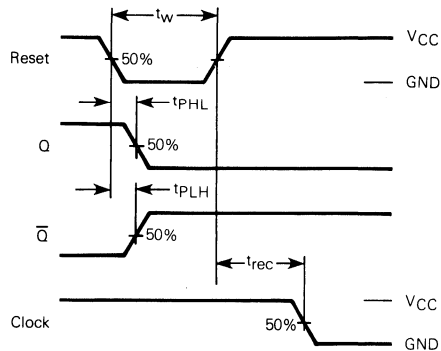


Figure 2.

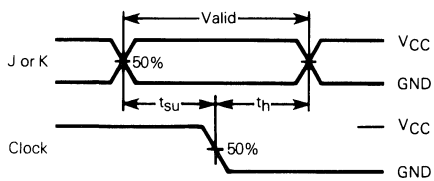
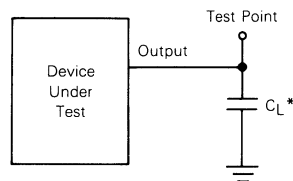


Figure 3.

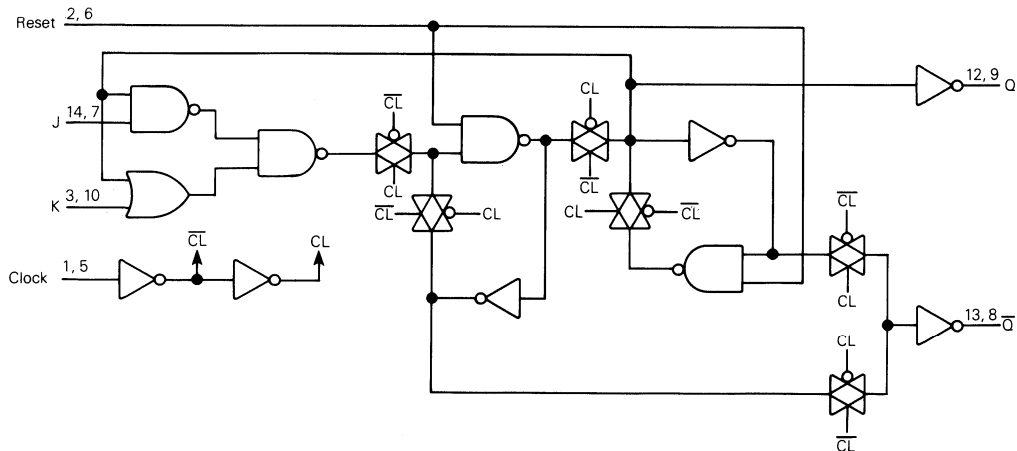


\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

5

## EXPANDED LOGIC DIAGRAM



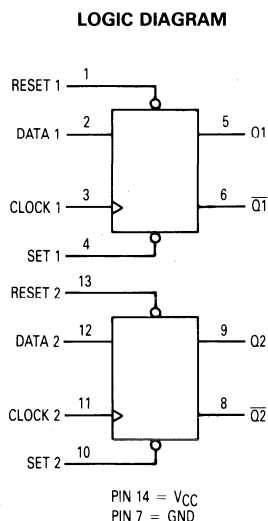
## Dual D Flip-Flop with Set and Reset

### High-Performance Silicon-Gate CMOS

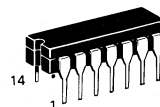
The MC54/74HC74A is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and  $\bar{Q}$  outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

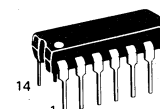
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 128 FETs or 32 Equivalent Gates



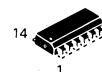
## MC54/74HC74A



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



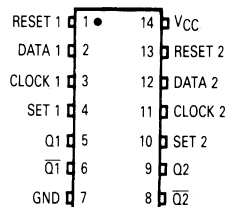
D SUFFIX  
 SOIC  
 CASE 751A-02

### ORDERING INFORMATION

MC74HCXXAN	Plastic
MC54HCXXAJ	Ceramic
MC74HCXXAD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H		H	H	L
H	H		L	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H		X	No Change	No Change

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

**5**

# MC54/74HC74A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package‡	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	2.0	0.26	0.33	0.4	μA
			4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> = GND I <sub>out</sub> = 0 μA	6.0	2.0	20	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC74A

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figures 1 and 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Set or Reset to Q or $\bar{Q}$ (Figures 2 and 4)	2.0	105	130	160	ns
		4.5	21	26	32	
		6.0	18	22	27	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
		39			

## TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>h</sub>	Minimum Hold Time, Clock to Data (Figure 3)	2.0	3.0	3.0	3.0	ns
		4.5	3.0	3.0	3.0	
		6.0	3.0	3.0	3.0	
t <sub>rec</sub>	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	8.0	8.0	8.0	ns
		4.5	8.0	8.0	8.0	
		6.0	8.0	8.0	8.0	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t <sub>w</sub>	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

# MC54/74HC74A

## SWITCHING WAVEFORMS

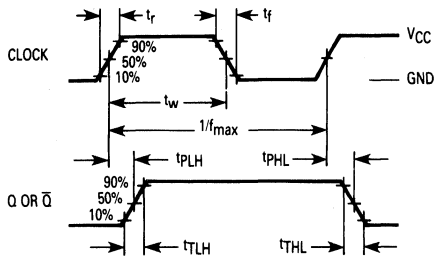


Figure 1.

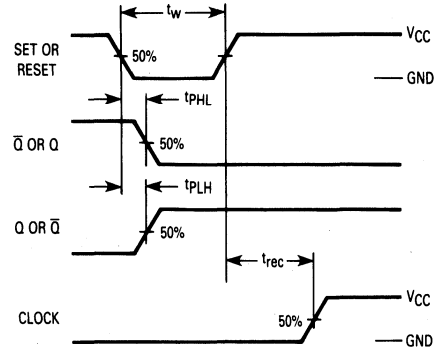


Figure 2.

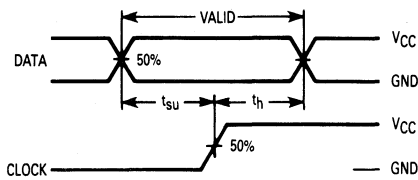
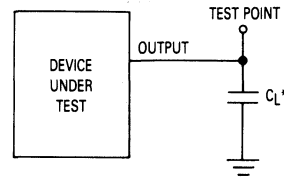


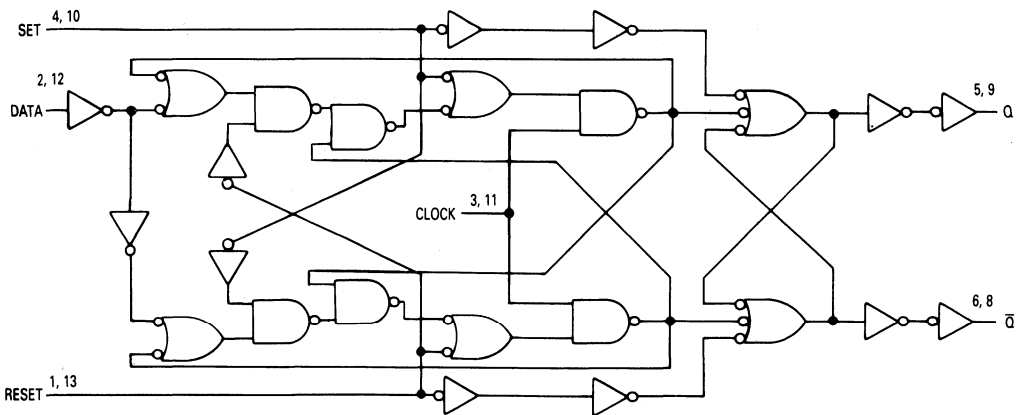
Figure 3.



\*Includes all probe and jig capacitance

Figure 4.

## EXPANDED LOGIC DIAGRAM



## Dual D Flip-Flop with Set and Reset with LSTTL Compatible Inputs

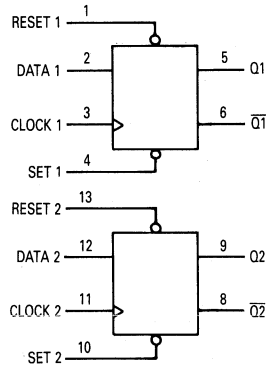
### High-Performance Silicon-Gate CMOS

The MC54/74HCT74A is identical in pinout to the LS74. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and  $\bar{Q}$  outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates

#### LOGIC DIAGRAM

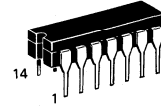


PIN 14 = V<sub>CC</sub>  
 PIN 7 = GND

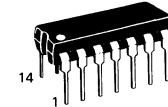
Design Criteria	Value	Units
Internal Gate Count*	34	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	.0075	pJ

\*Equivalent to a two-input NAND gate.

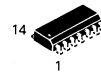
## MC54/74HCT74A



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06

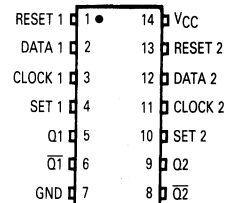


D SUFFIX  
 SOIC  
 CASE 751A-02

#### ORDERING INFORMATION

MC74HCTXXAN	Plastic
MC54HCTXXAJ	Ceramic
MC74HCTXXAD	SOIC

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H		L	H	L
H	H		H	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H		X	No Change	No Change

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

# MC54/74HCT74A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1.0 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V I <sub>out</sub> ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V I <sub>out</sub> ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>out</sub> ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>out</sub> ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>out</sub> ≤ 4.0 mA	4.5	3.98	3.84	3.7	μA
			5.5	0.26	0.33	0.4	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	1.0	10	40	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HCT74A

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$f_{\max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figures 1 and 4)	24	30	36	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Set or Reset to Q or $\bar{Q}$ (Figures 2 and 4)	24	30	36	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF
$C_{PD}$	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$			pF
		130			

## TIMING REQUIREMENTS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )

Symbol	Parameter	Fig.	Guaranteed Limit						Units
			25°C to -55°C		≤85°C		≤125°C		
			Min	Max	Min	Max	Min	Max	
$t_{su}$	Minimum Setup Time, Data to Clock	3	15		19		22		ns
$t_h$	Minimum Hold Time, Clock to Data	3	3		3		3		ns
$t_{rec}$	Minimum Recovery Time, Set or Reset Inactive to Clock	2	6		8		9		ns
$t_w$	Minimum Pulse Width, Clock	1	15		19		22		ns
$t_w$	Minimum Pulse Width, Set or Reset	2	15		19		22		ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Times	1		500		500		500	ns

# MC54/74HCT74A

## SWITCHING WAVEFORMS

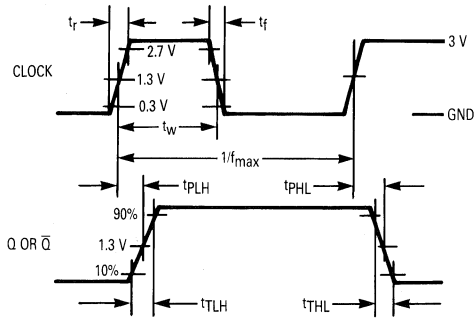


Figure 1.

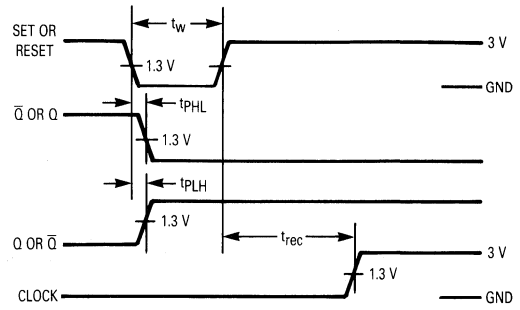


Figure 2.

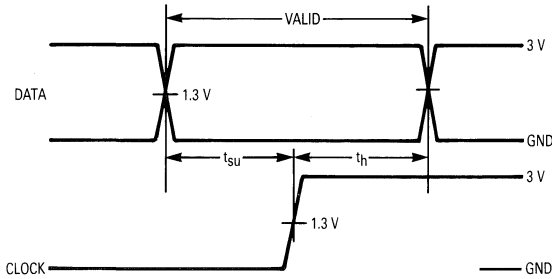
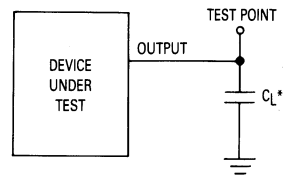


Figure 3.

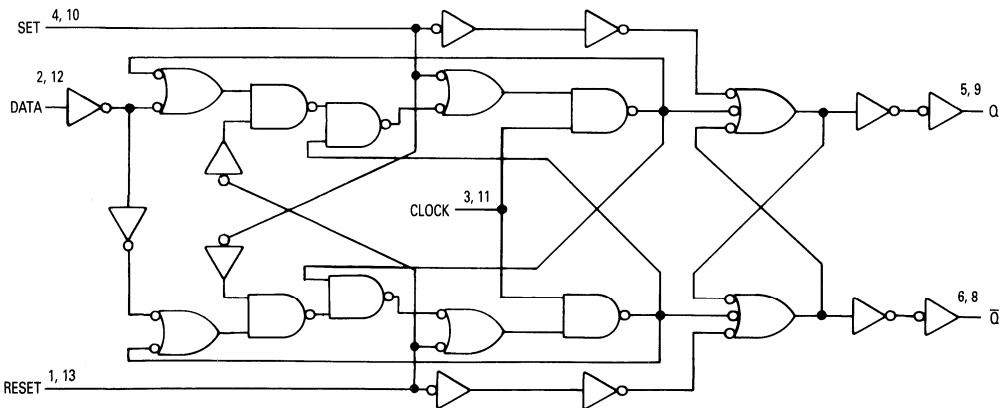


\*Includes all probe and jig capacitance

Figure 4. Test Circuit

5

### EXPANDED LOGIC DIAGRAM

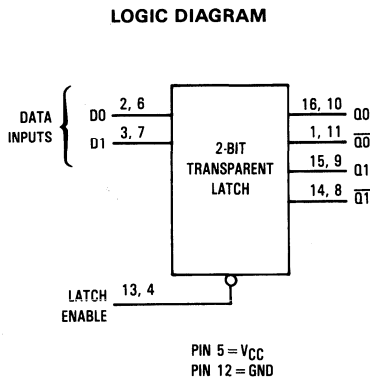


## Dual 2-Bit Transparent Latch High-Performance Silicon-Gate CMOS

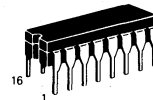
The MC54/74HC75 is identical in pinout to the LS75. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 2-bit transparent latches. Each latch stores the input data while Latch Enable is at a logic low. The outputs follow the data inputs when Latch Enable is at a logic high.

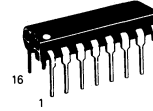
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 80 FETs or 20 Equivalent Gates



### MC54/74HC75



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



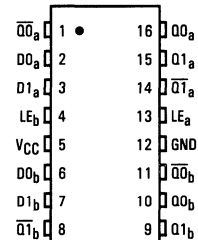
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

#### ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs		Outputs	
D	Latch Enable	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q0	$\bar{Q}0$

X = don't care  
 Q0 = latched data

**5**

# MC54/74HC75

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC75

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, D to Q (Figures 1 and 5)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, D to $\bar{Q}$ (Figures 1 and 5)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to $\bar{Q}$ (Figures 2 and 5)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, D to Latch Enable (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Latch Enable to D (Figure 4)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable Input (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC75

## SWITCHING WAVEFORMS

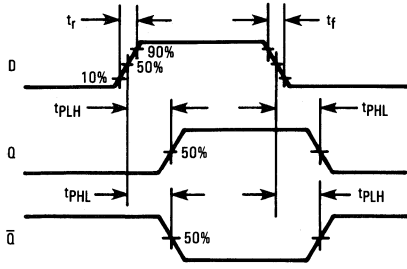


Figure 1

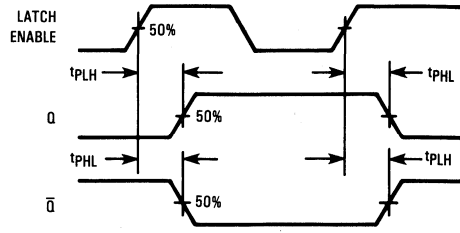


Figure 2

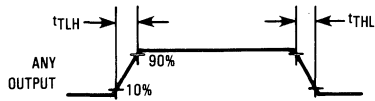


Figure 3

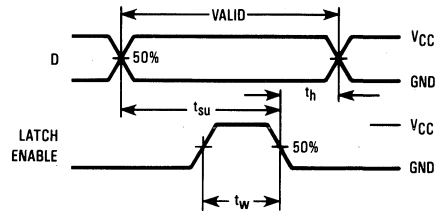
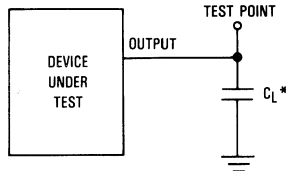


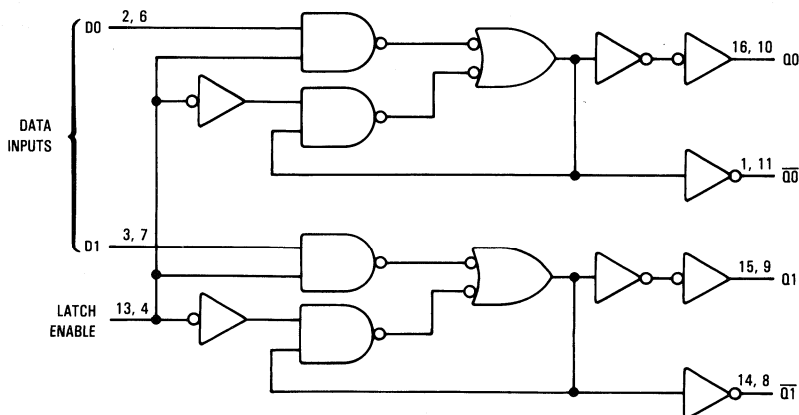
Figure 4



\*Includes all probe and jig capacitance.

Figure 5. Test Circuit

## EXPANDED LOGIC DIAGRAM



## 4-Bit Magnitude Comparator

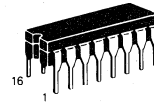
### High-Performance Silicon-Gate CMOS

The MC54/74HC85 is identical in pinout and function to the LS85. This device is similar in function to the MM74C85 and L85, but has a different pinout. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

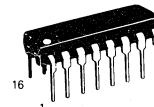
This 4-Bit Magnitude Comparator compares two 4-bit nibbles and gives a high voltage level on either the  $A > B_{out}$ ,  $A = B_{out}$ , or  $A < B_{out}$  output, leaving the other two at a low voltage level. This device also has  $A > B_{in}$ ,  $A = B_{in}$ , and  $A < B_{in}$  inputs, eliminating the need for external gates when cascading.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current:  $1 \mu A$
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 248 FETs or 62 Equivalent Gates

## MC54/74HC85



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



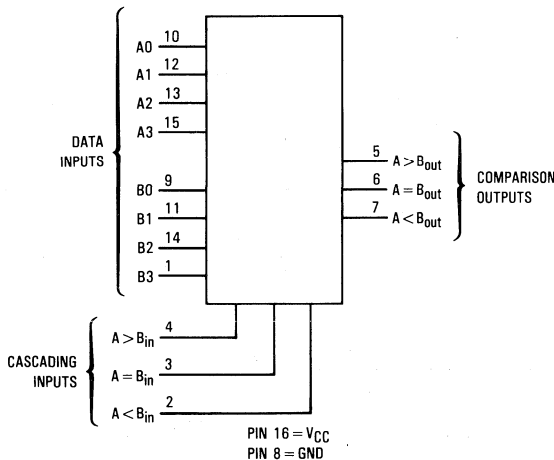
**N SUFFIX  
 PLASTIC  
 CASE 648-06**

### ORDERING INFORMATION

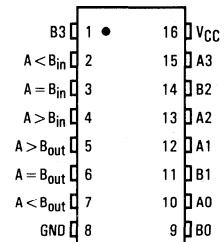
MC74HCXXN	Plastic
MC54HCXXJ	Ceramic

$T_A = -55^\circ$  to  $125^\circ C$  for all packages.  
 Dimensions in Chapter 6.

### LOGIC DIAGRAM



### PIN ASSIGNMENT



# MC54/74HC85

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	0.26	0.33	0.40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	4.5	0.26	0.33	0.40	μA
			6.0	8	80	160	
			6.0	±0.1	±1.0	±1.0	

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HC85

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Inputs A or B to Outputs A > B or A < B (Figures 1 and 2)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Inputs A or B to Output A = B (Figures 1 and 2)	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Inputs A < B or A = B to Output A > B (Figures 1 and 2)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Inputs A > B or A = B to Output A < B (Figures 1 and 2)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A = B to Output A = B (Figures 1 and 2)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		50	

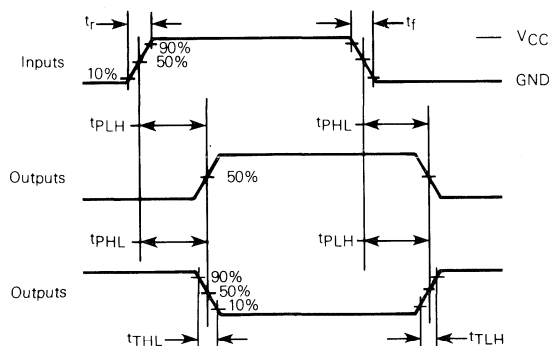
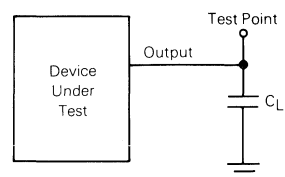


Figure 1. Switching Waveforms



\* Includes all probe and jig capacitance.

Figure 2. Test Circuit

# MC54/74HC85

## PIN DESCRIPTIONS

### INPUTS

**A0, A1, A2, A3 (Pins 10, 12, 13, 15)** — Data Nibble A Inputs. The data nibble present at these inputs is compared to Data Nibble B. A3 is the most significant bit and A0 is the least significant bit.

**B0, B1, B2, B3 (Pins 9, 11, 14, 1)** — Data Nibble B Inputs. The data nibble present at these inputs is compared to Data Nibble A. B3 is the most significant bit and B0 is the least significant bit.

### CONTROLS

**A > B<sub>in</sub>, A = B<sub>in</sub>, A < B<sub>in</sub> (Pins 4, 3, 2)** — Cascading Inputs. These inputs determine the states of the outputs only when Data Nibble A equals Data Nibble B. The A = B<sub>in</sub> input overrides both the A > B<sub>in</sub> and A < B<sub>in</sub> inputs.

For single stage operation or for the least significant stage in cascaded operation, the A < B<sub>in</sub> and A > B<sub>in</sub> inputs should be tied to ground and the A = B<sub>in</sub> input tied to V<sub>CC</sub>. Between cascaded comparators, the A < B<sub>out</sub>, A = B<sub>out</sub>, and A > B<sub>out</sub>

outputs should be tied to A < B<sub>in</sub>, A = B<sub>in</sub>, and A > B<sub>in</sub>, respectively, of the succeeding stage.

### OUTPUTS

**A > B<sub>out</sub> (Pin 5)** — A-Greater-Than-B Output. This output is at a high voltage level when Nibble A is greater than Nibble B, regardless of the data present at the cascading inputs. This output is also high when Nibble A equals Nibble B and the A > B<sub>in</sub> input is high (A < B<sub>in</sub> and A = B<sub>in</sub> are at a low voltage level).

**A = B<sub>out</sub> (Pin 6)** — A-Equals-B Output. This output is high when Nibble A equals Nibble B and the A = B<sub>in</sub> input is high. A < B<sub>in</sub> and A > B<sub>in</sub> have no effect when the comparator is in this condition and A = B<sub>in</sub> is at a high voltage level.

**A < B<sub>out</sub> (Pin 7)** — A-Less-Than-B Output. This output is at a high voltage level when Nibble A is less than Nibble B, regardless of data present at the cascading inputs. This output is also high when Nibble A equals Nibble B and the A < B<sub>in</sub> input is high (A > B<sub>in</sub> and A = B<sub>in</sub> are at a low voltage level).

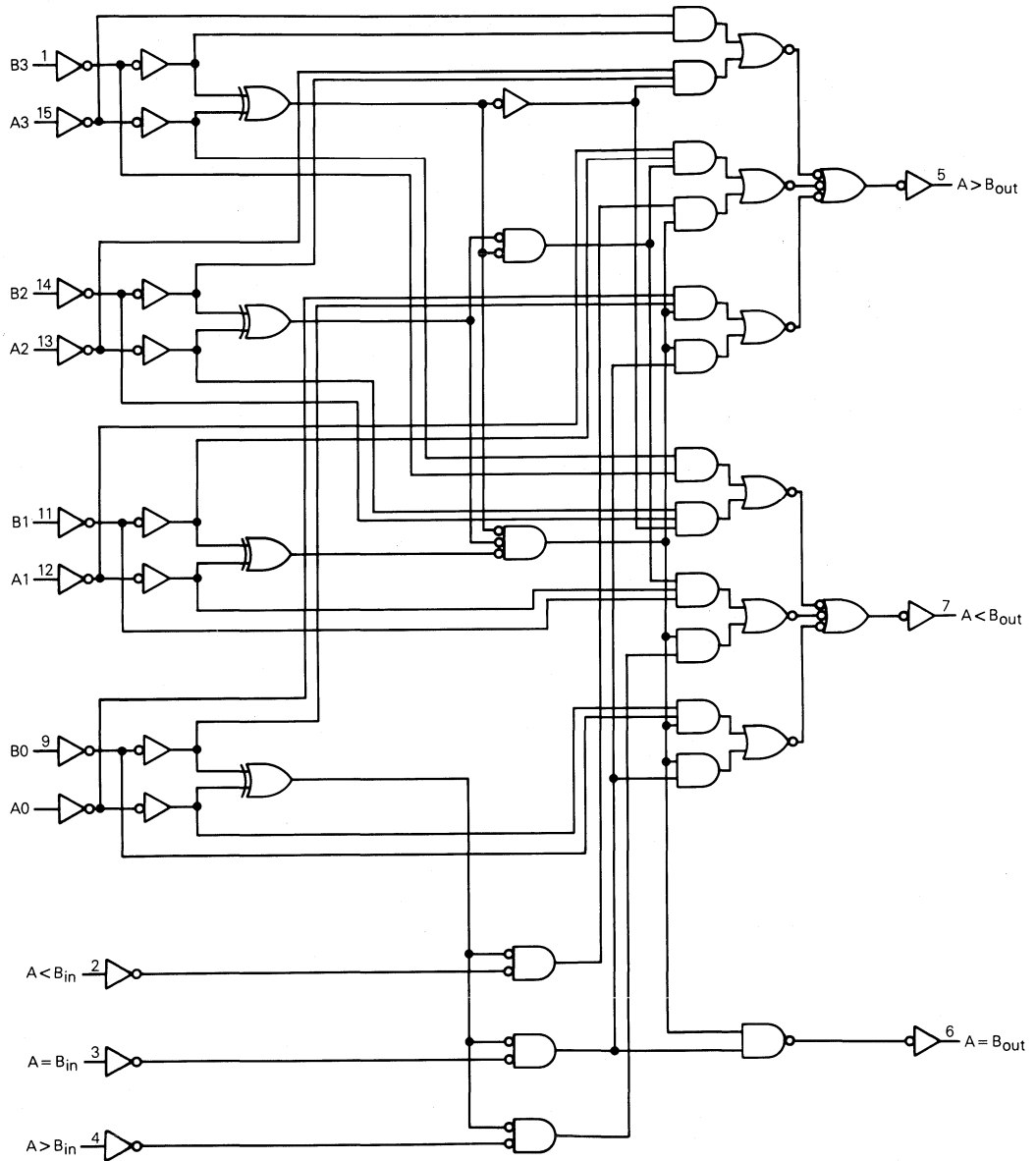
FUNCTION TABLE

Data Inputs				Cascading Inputs			Output		
A3, B3	A2, B2	A1, B1	A0, B0	A > B <sub>in</sub>	A = B <sub>in</sub>	A < B <sub>in</sub>	A > B <sub>out</sub>	A = B <sub>out</sub>	A < B <sub>out</sub>
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	L	H
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	H	X	L	H	L

X = Don't Care

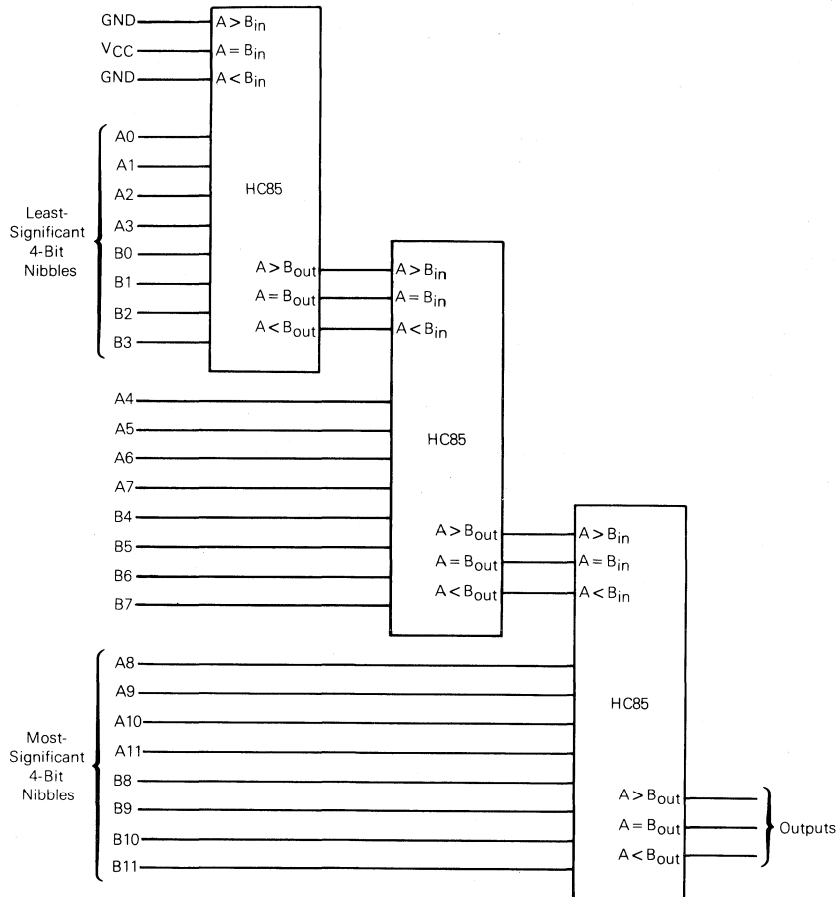
# MC54/74HC85

## EXPANDED LOGIC DIAGRAM



# MC54/74HC85

## TYPICAL APPLICATION CASCADING COMPARATORS



5

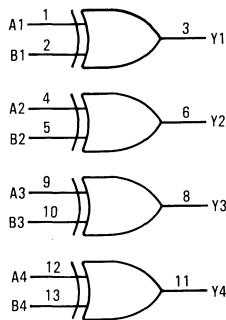
## Quad 2-Input Exclusive OR Gate

### High-Performance Silicon-Gate CMOS

The MC54/74HC86 is identical in pinout to the LS86; this device is similar in function to the MM74C86 and L86, but has a different pinout. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates

#### LOGIC DIAGRAM

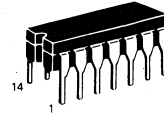


$$Y = A \oplus B$$

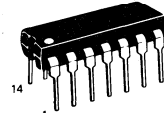
$$= \bar{A}B + A\bar{B}$$

PIN 14 =  $V_{CC}$   
 PIN 7 = GND

## MC54/74HC86



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



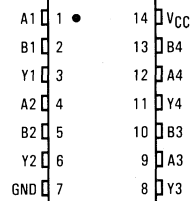
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

#### ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

# MC54/74HC86

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	5.9	5.9	5.9	
			4.5	3.98	3.84	3.70	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
			6.0	2	20	40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC86

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		33	

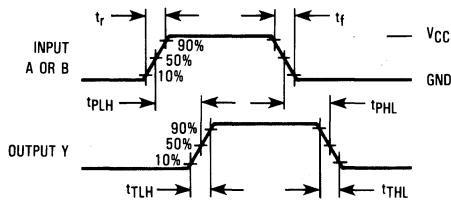
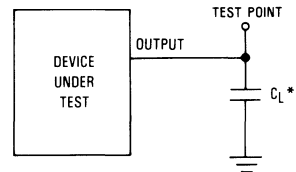


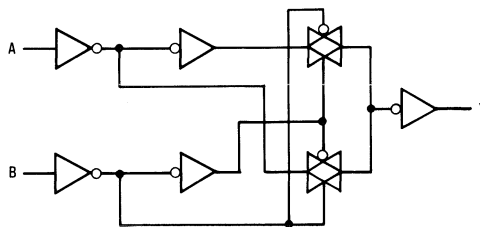
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM (% of Device)



## Dual J-K Flip-Flop with Reset

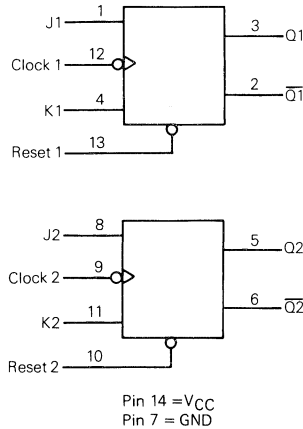
### High-Performance Silicon-Gate CMOS

The MC54/74HC107 is identical in pinout to the LS107. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

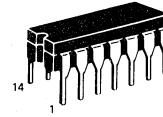
Each flip-flop is negative-edge clocked and has an active-low asynchronous reset. The HC107 is identical in function to the HC73, but has a different pinout.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates

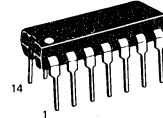
#### LOGIC DIAGRAM



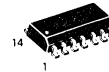
## MC54/74HC107



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



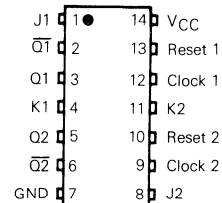
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

#### ORDERING INFORMATION

MC74HCXXD	SOIC
MC74HCXXN	Plastic
MC54HCXXJ	Ceramic

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs				Outputs	
Reset	Clock	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H		L	L	No Change	
H		L	H	L	H
H		H	L	H	L
H		H	H	Toggle	
H	L	X	X	No Change	
H	H	X	X	No Change	
H		X	X	No Change	



# MC54/74HC107

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260	°C
		300	

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	V	
			4.5	3.15	3.15		
			6.0	4.2	4.2		
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	V	
			4.5	0.9	0.9		
			6.0	1.2	1.2		
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	V	
			4.5	4.4	4.4		
			6.0	5.9	5.9		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	V	
			4.5	0.1	0.1		
			6.0	0.1	0.1		
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33		
			6.0	0.26	0.33		
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	±0.1	±1.0	μA	
			6.0	4	40		80

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC107

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figures 1 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q or $\bar{Q}$ (Figures 2 and 4)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC107

## SWITCHING WAVEFORMS

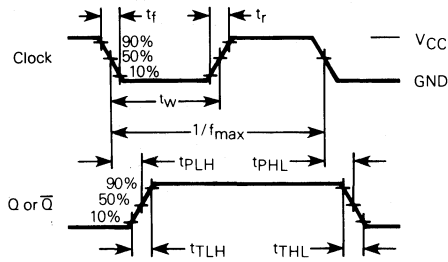


Figure 1.

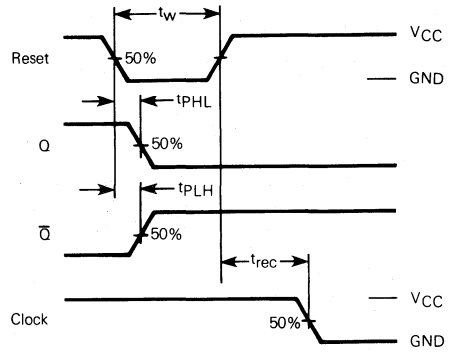


Figure 2.

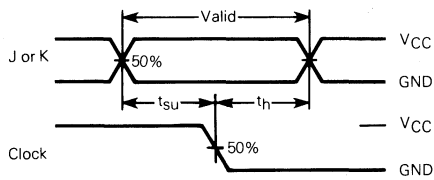
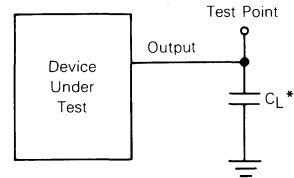


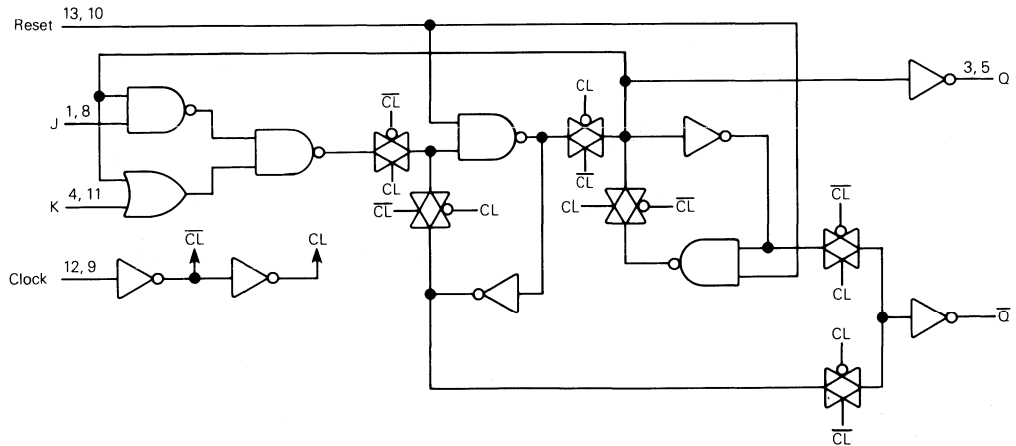
Figure 3.



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM



# Dual J-K Flip-Flop with Set and Reset

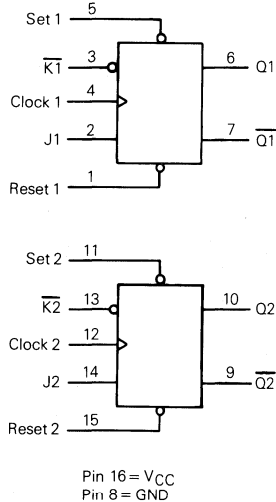
## High-Performance Silicon-Gate CMOS

The MC54/74HC109 is identical in pinout to the LS109. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

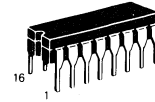
This device consists of two J-K flip-flops with individual set, reset, and clock inputs. Changes at the inputs are reflected at the outputs with the next low-to-high transition of the clock. Both Q and  $\bar{Q}$  outputs are available from each flip-flop.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 148 FETs or 37 Equivalent Gates

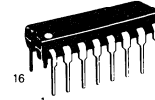
### LOGIC DIAGRAM



## MC54/74HC109



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



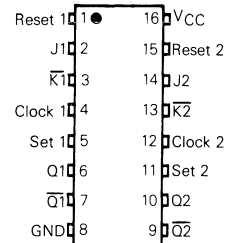
**D SUFFIX**  
**SOIC**  
**CASE 751B-03**

### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H		L	L	L	H
H	H		H	L	Toggle	
H	H		L	H	No Change	
H	H		H	H	H	L
H	H	L	X	X	No Change	

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

5

# MC54/74HC109

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	$\mu\text{A}$
			6.0	5.48	5.34	5.20	
			6.0	0.26	0.33	0.40	
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
			6.0	4	40	80	
			6.0	0.26	0.33	0.40	

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC109

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figures 1 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Set or Reset to Q or $\bar{Q}$ (Figures 2 and 4)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		40	

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, J or $\bar{K}$ to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Clock to J or $\bar{K}$ (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>rec</sub>	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC109

## SWITCHING WAVEFORMS

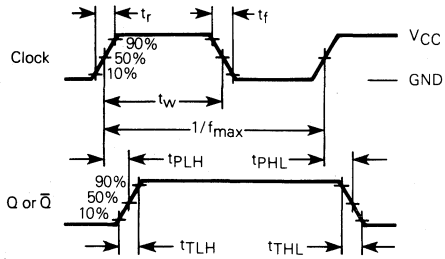


Figure 1.

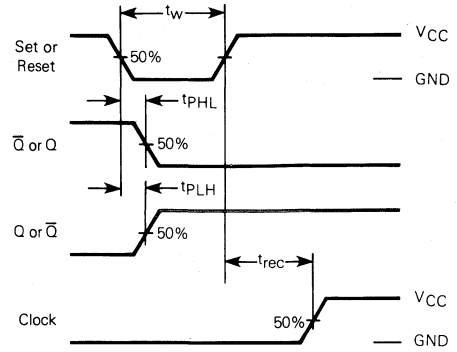


Figure 2.

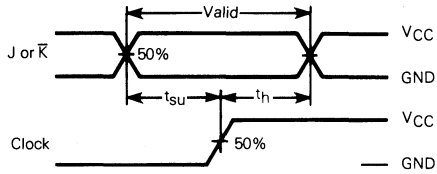
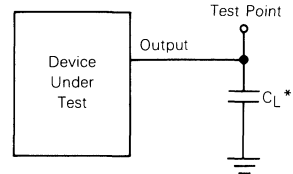


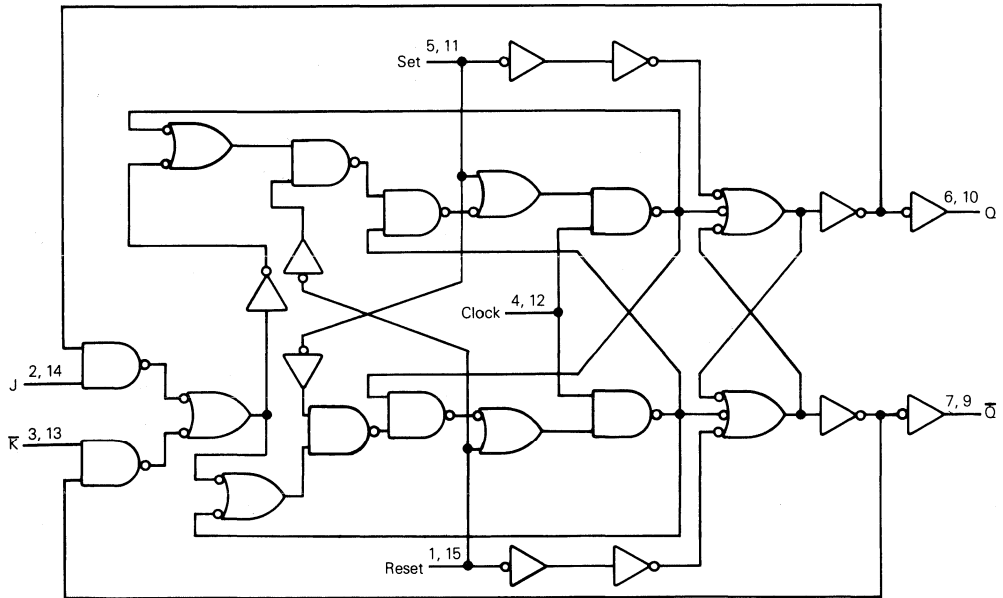
Figure 3.



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM



# Dual J-K Flip-Flop with Set and Reset

## High-Performance Silicon-Gate CMOS

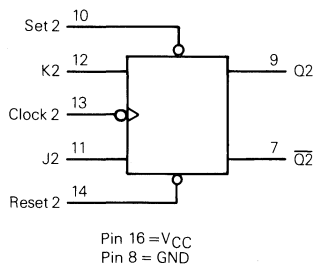
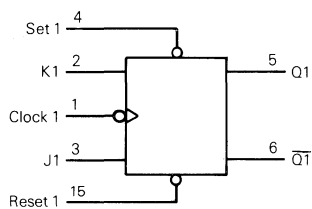
The MC54/74HC112 is identical in pinout to the LS112. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

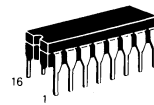
The HC112 is identical in function to the HC76, but has a different pinout.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Similar in Function to the LS112 Except When Set and Reset are Low Simultaneously
- Chip Complexity: 100 FETs or 25 Equivalent Gates

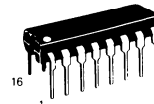
### LOGIC DIAGRAM



## MC54/74HC112



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



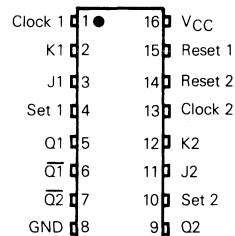
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXD	SOIC
MC74HCXXN	Plastic
MC54HCXXJ	Ceramic

T<sub>A</sub> = -55° to 125°C for all packages.  
Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↘	L	L	No Change	
H	H	↘	L	H	L	H
H	H	↘	H	L	H	L
H	H	↘	H	H	Toggle	
H	H	L	X	X	No Change	
H	H	H	X	X	No Change	
H	H	↘	X	X	No Change	

\* Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

5



# MC54/74HC112

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltage to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC112

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figures 1 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q or $\bar{Q}$ (Figures 2 and 4)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Set to Q or $\bar{Q}$ (Figures 2 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC112

## SWITCHING WAVEFORMS

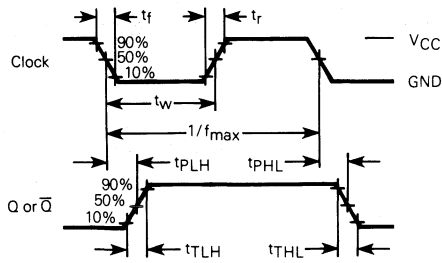


Figure 1.

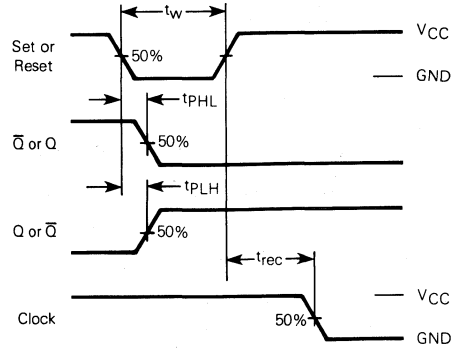


Figure 2.

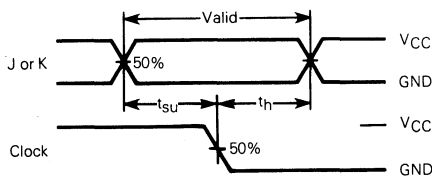
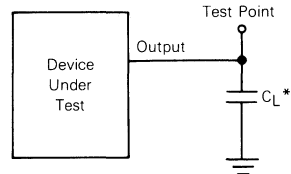


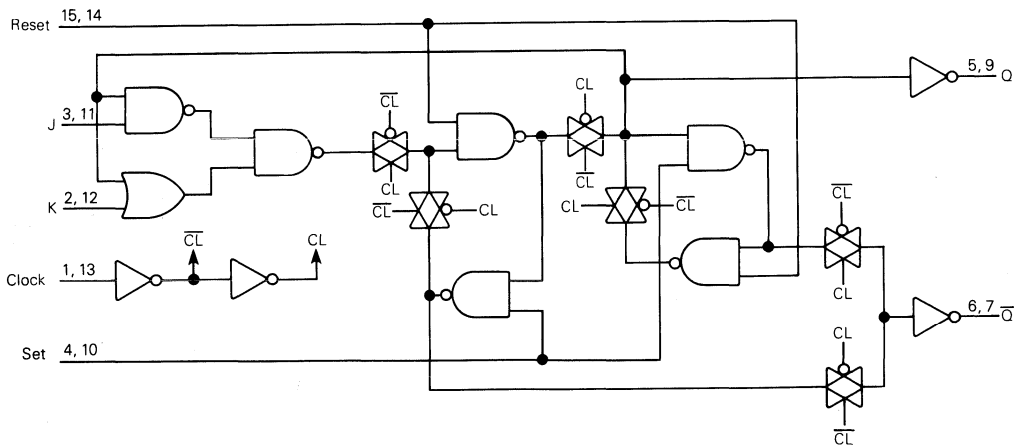
Figure 3.



\*includes all probe and jig capacitance.

Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM



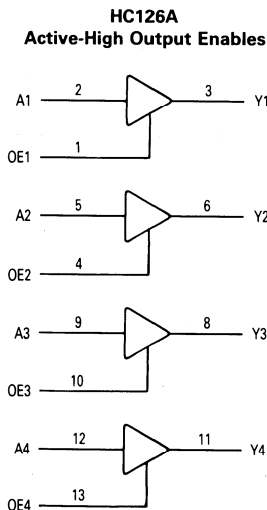
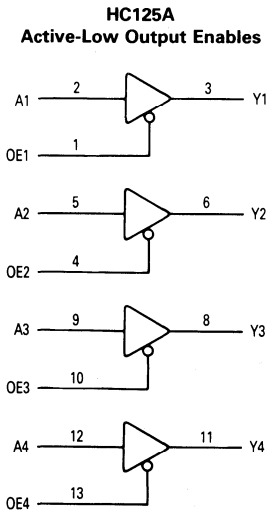
## Quad 3-State Noninverting Buffers High-Performance Silicon-Gate CMOS

The MC54/74HC125A and MC54/74HC126A are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC125A and HC126A noninverting buffers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low (HC125A) or active-high (HC126A).

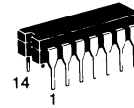
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

### LOGIC DIAGRAM

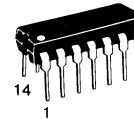


PIN 14 =  $V_{CC}$   
 PIN 7 = GND

## MC54/74HC125A MC54/74HC126A



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



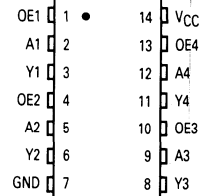
D SUFFIX  
 SOIC  
 CASE 751A-02

### ORDERING INFORMATION

MC74HCXXXAN Plastic  
 MC54HCXXXAJ Ceramic  
 MC74HCXXXAD SOIC

$T_A$  = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

HC125A			HC126A		
Inputs	Output		Inputs	Output	
A	OE	Y	A	OE	Y
H	L	H	H	H	H
L	L	L	L	H	L
X	H	Z	X	L	Z

X = don't care  
 Z = high impedance

# MC54/74HC125A • MC54/74HC126A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit				
				25°C to -55°C	≤85°C	≤125°C					
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V				
			4.5	3.15	3.15	3.15					
			6.0	4.2	4.2	4.2					
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V				
			4.5	1.35	1.35	1.35					
			6.0	1.8	1.8	1.8					
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V				
			4.5	4.4	4.4	4.4					
			6.0	5.9	5.9	5.9					
			V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34		3.7 5.2			
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V				
			4.5	0.1	0.1	0.1					
			6.0	0.1	0.1	0.1					
			V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33		0.4 0.4			
			I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0		±0.1	±1.0	±1.0	μA
			I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0		±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4.0	40	160	μA				

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC125A • MC54/74HC126A

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6.0$  ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0	90	115	135	ns
		4.5	18	23	27	
		6.0	15	20	23	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0	90	115	135	ns
		4.5	18	23	27	
		6.0	15	20	23	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, VCC = 5.0 V	pF
		45	

## SWITCHING WAVEFORMS

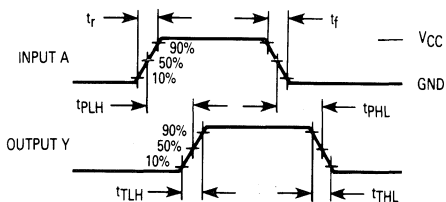


Figure 1

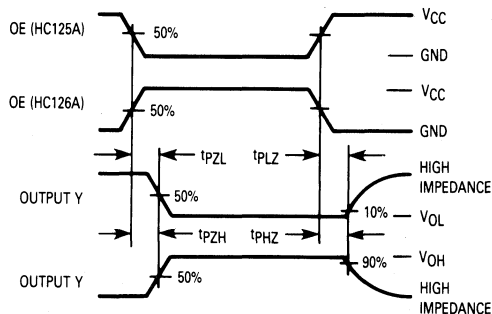
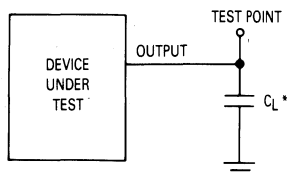
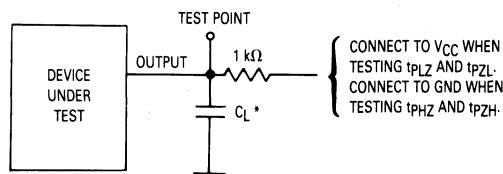


Figure 2



\*Includes all probe and jig capacitance.

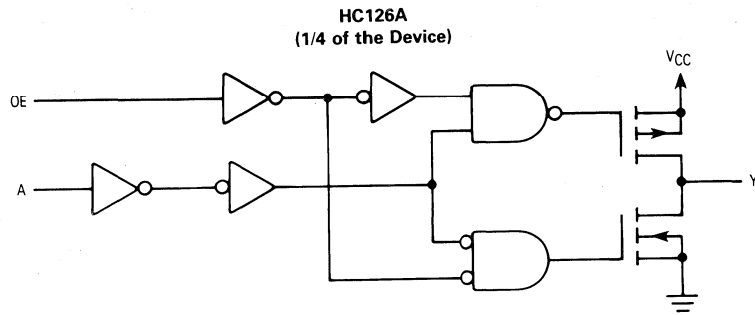
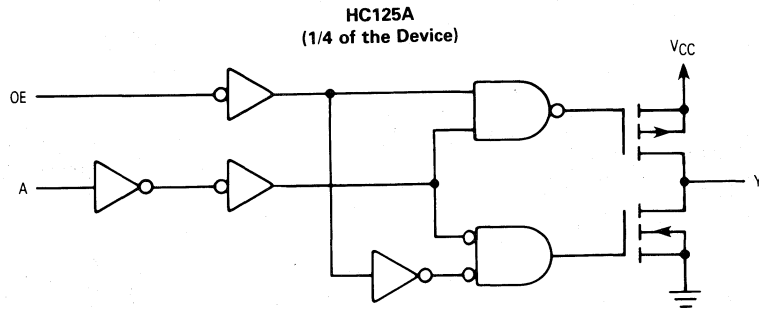
Figure 3. Test Circuit



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

# MC54/74HC125A • MC54/74HC126A



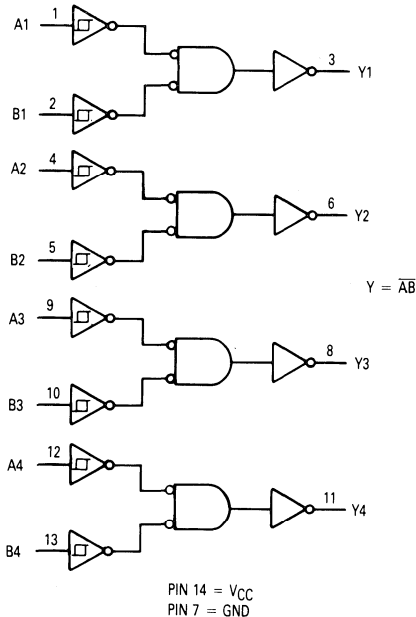
## Quad 2-Input NAND Gate with Schmitt-Trigger Inputs High-Performance Silicon-Gate CMOS

The MC54/74HC132A is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

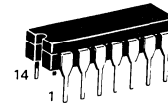
The HC132A can be used to enhance noise immunity or to square up slowly changing waveforms.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

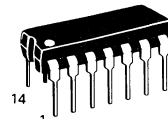
### LOGIC DIAGRAM



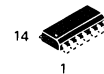
## MC54/74HC132A



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



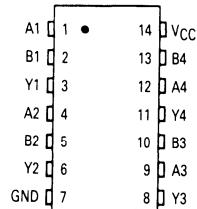
D SUFFIX  
 SOIC  
 CASE 751A-02

### ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXAD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L



# MC54/74HC132A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	—	no limit*	ns

\*When V<sub>in</sub> ~ 0.5 V<sub>CC</sub>, I<sub>CC</sub> > > quiescent current.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C	-40°C to +85°C	-55°C to +125°C	
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>T+</sub> min	Minimum Positive-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.0	0.95	0.95	V
			4.5	2.3	2.25	2.25	
			6.0	3.0	2.95	2.95	
V <sub>T-</sub> max	Maximum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.9	0.95	0.95	V
			4.5	2.0	2.05	2.05	
			6.0	2.6	2.65	2.65	
V <sub>T-</sub> min	Minimum Negative-Going Input Threshold Voltage (Figure 3)	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>H</sub> max Note 2	Maximum Hysteresis Voltage (Figure 3)	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.2	1.2	1.2	V
			4.5	2.25	2.25	2.25	
			6.0	3.0	3.0	3.0	
V <sub>H</sub> min Note 2	Minimum Hysteresis Voltage (Figure 3)	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.2	0.2	0.2	V
			4.5	0.4	0.4	0.4	
			6.0	0.5	0.5	0.5	

NOTE 1. V<sub>H</sub> min > (V<sub>T+</sub> min) - (V<sub>T-</sub> max); V<sub>H</sub> max = (V<sub>T+</sub> max) + (V<sub>T-</sub> min).

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC132A

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> ≤ V <sub>T- min</sub> or V <sub>T+ max</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> ≤ V <sub>T- min</sub> or V <sub>T+ max</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> ≥ V <sub>T+ max</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> ≥ V <sub>T+ max</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	1.0	10	40	μA

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		24	

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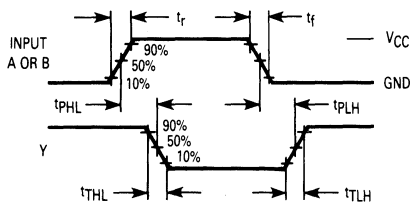
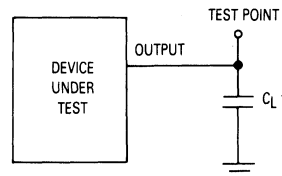


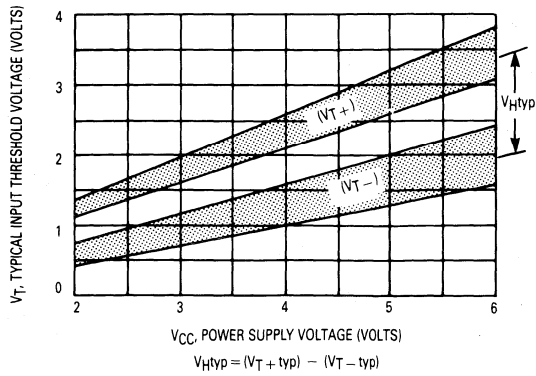
Figure 1. Switching Waveforms



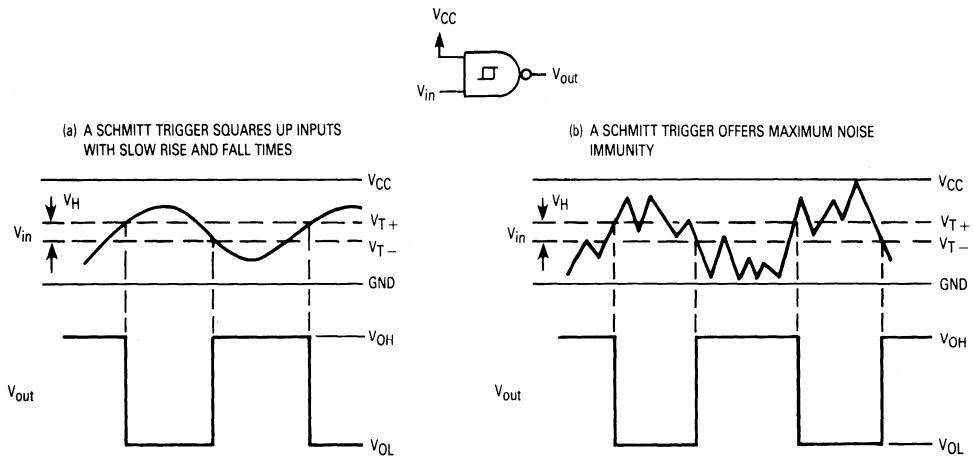
\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

# MC54/74HC132A



**Figure 3. Typical Input Threshold,  $V_{T+}$ ,  $V_{T-}$ , versus Power Supply Voltage**



**Figure 4. Typical Schmitt-Trigger Applications**

# 13-Input NAND Gate

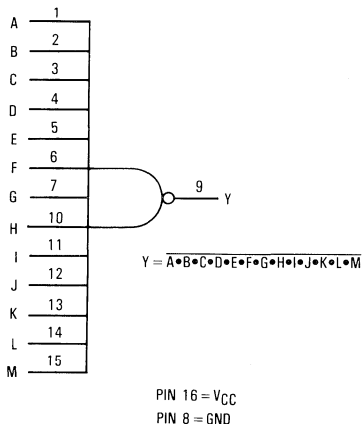
## High-Performance Silicon-Gate CMOS

The MC54/74HC133 is identical in pinout to the LS133. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This NAND gate features 13 inputs which surpasses most random logic requirements.

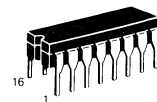
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 68 FETs or 17 Equivalent Gates

### LOGIC DIAGRAM

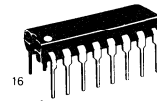


**5**

## MC54/74HC133



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



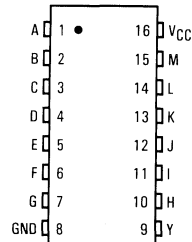
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs A through M	Output Y
All inputs H	L
All other combinations	H

# MC54/74HC133

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>		I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
			6.0	2	20	40	
			6.0	2	20	40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μA
			6.0	2	20	40	
			6.0	2	20	40	

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC133

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		27	

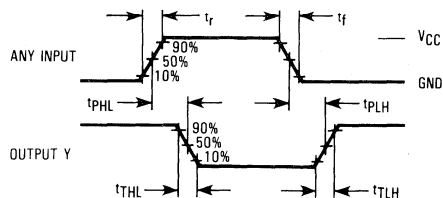
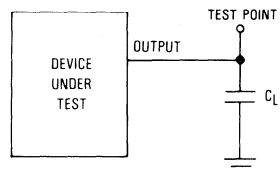


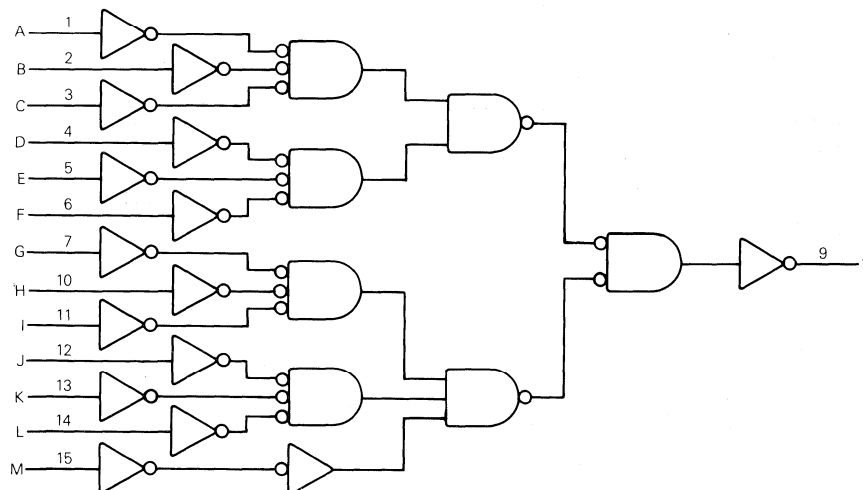
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM



# 1-of-8 Decoder/Demultiplexer with Address Latch

## High-Performance Silicon-Gate CMOS

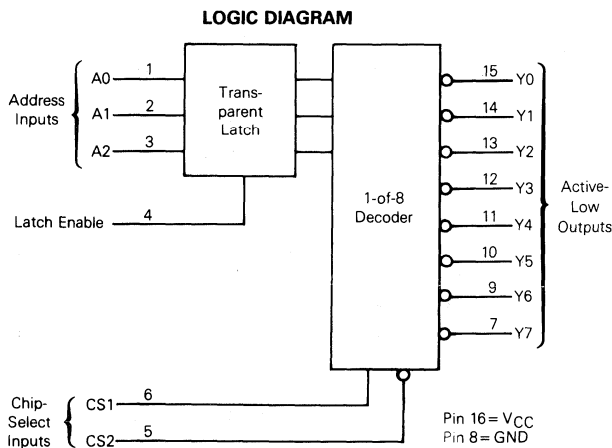
The MC54/74HC137 is identical in pinout to the LS137. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC137 decodes a three-bit Address to one-of-eight active-low outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

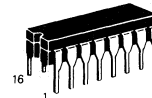
The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC137 is the inverting version of the HC237.

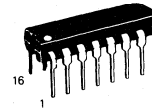
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 152 FETs or 38 Equivalent Gates



### MC54/74HC137



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



**N SUFFIX  
 PLASTIC  
 CASE 648-06**



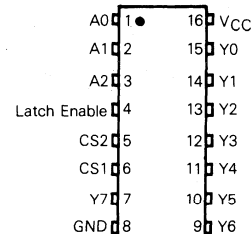
**D SUFFIX  
 SOIC  
 CASE 751B-04**

#### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs						Outputs							
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	*							

\* = Depends upon the Address previously applied while LE was at a low level.

# MC54/74HC137

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	2.0	0.1	0.1	0.1	μA
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	2.0	0.26	0.33	0.40	μA
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	2.0	± 0.1	± 1.0	± 1.0	μA
			4.5	± 0.1	± 1.0	± 1.0	
			6.0	± 0.1	± 1.0	± 1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	2.0	8	80	160	μA
			4.5	8	80	160	
			6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.

5



# MC54/74HC137

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 6)	2.0	170	215	255	ns
		4.5	34	43	51	
		6.0	29	37	43	
t <sub>PHL</sub>		2.0	240	300	360	
		4.5	48	60	72	
		6.0	41	51	61	
t <sub>PLH</sub>	Maximum Propagation Delay, CS1 or CS2 to Output Y (Figures 2, 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PHL</sub>		2.0	195	245	295	
		4.5	39	49	59	
		6.0	33	42	50	
t <sub>PLH</sub>	Maximum Propagation Delay, Latch Enable to Output Y (Figures 4 and 6)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PHL</sub>		2.0	250	315	375	
		4.5	50	63	75	
		6.0	43	54	64	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		100	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Input A to Latch Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input A (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 2)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC137

## PIN DESCRIPTIONS

### ADDRESS INPUTS

**A0, A1, A2 (PINS 1, 2, 3)** — Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

### CONTROL INPUTS

**CS1, CS2 (PINS 6, 5)** — Chip-Select inputs. For CS1 at a high level and CS2 at a low level, the chip is enabled and the outputs follow the address inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs are at a high level.

**LATCH ENABLE (PIN 4)** — Latch-Enable input. A high level at this input latches the Address. A low level at this input allows the outputs to follow the data at the Address pins (CS1 = H and CS2 = L).

### OUTPUTS

**Y0-Y7** — Active-low outputs. One of these eight outputs is selected when the chip is enabled (CS1 = H and CS2 = L) and the data on the A0, A1, and A2 inputs correspond to that particular output. The selected output is at a low level while all others remain at a high level.

## SWITCHING WAVEFORMS

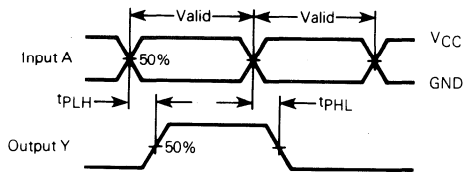


Figure 1.

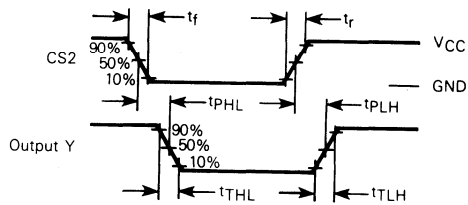


Figure 2.

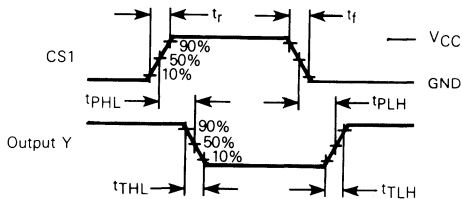


Figure 3.

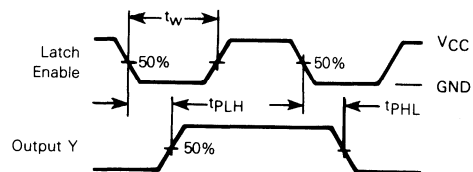


Figure 4.

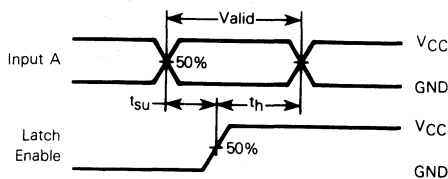
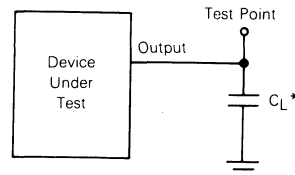


Figure 5.

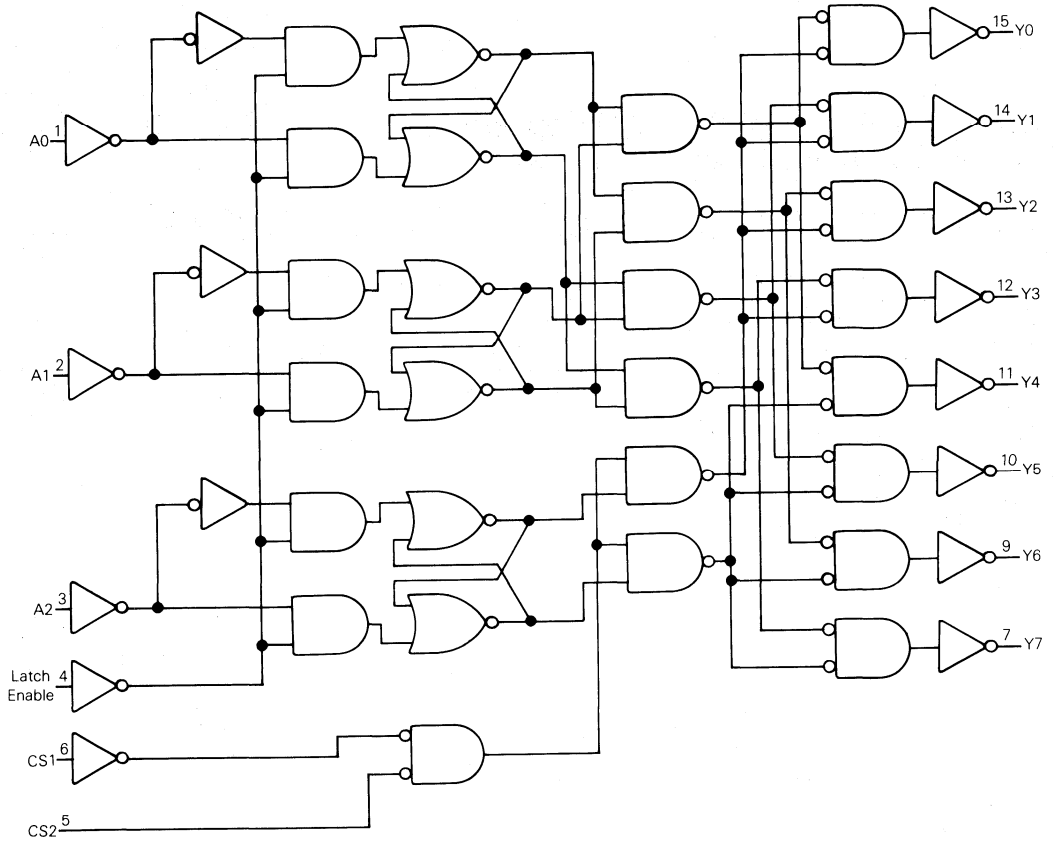


\* Includes all probe and jig capacitance.

Figure 6. Test Circuit

# MC54/74HC137

## EXPANDED LOGIC DIAGRAM



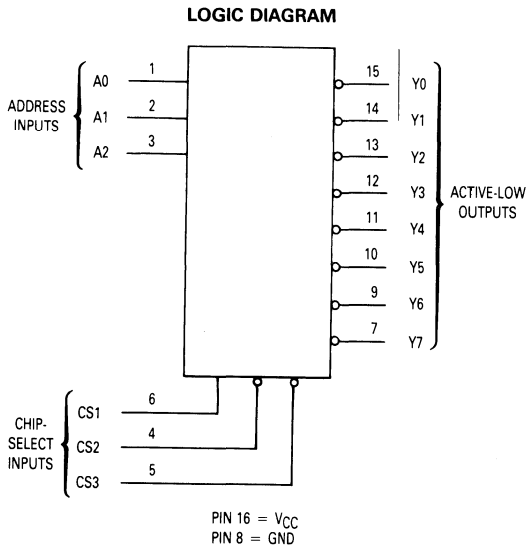
# 1-of-8 Decoder/Demultiplexer

## High-Performance Silicon-Gate CMOS

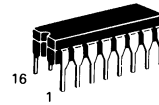
The MC54/74HC138A is identical in pinout to the LS138. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC138A decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

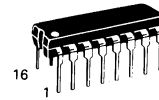
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 29 Equivalent Gates



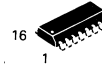
### MC54/74HC138A



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



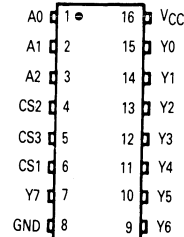
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

#### ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXAD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs					Outputs								
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	L	H	H	H	L
H	L	L	H	L	H	H	H	H	L	H	H	H	L
H	L	L	H	H	L	H	H	H	L	H	H	H	L

H = high level (steady state)  
 L = low level (steady state)  
 X = don't care

# MC54/74HC138A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation Plastic or Ceramic DIP† in Still Air, SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C  
For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 2)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
6.0	5.48		5.34	5.20			
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
6.0	0.26		0.33	0.40			
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	4	40	160	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC138A

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6.0$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	2.0 4.5 6.0	135 27 23	170 34 29	205 41 35	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, CS1 to Output Y (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, CS2 or CS3 to Output Y (Figures 3 and 4)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical (α 25°C, V <sub>CC</sub> = 5.0 V)	pF
		55	

## SWITCHING WAVEFORMS

Figure 1.

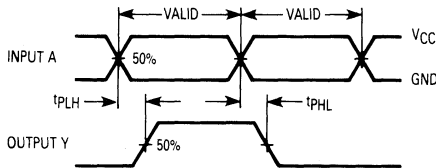


Figure 2.

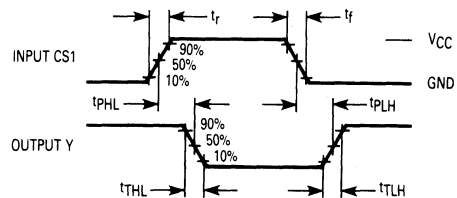


Figure 3.

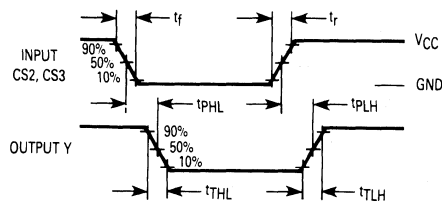
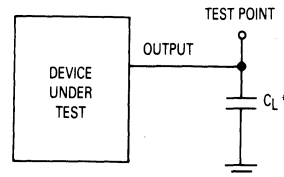


Figure 4. Test Circuit



\*Includes all probe and jig capacitance.

# MC54/74HC138A

## PIN DESCRIPTIONS

### ADDRESS INPUTS

**A0, A1, A2 (PINS 1, 2, 3)** — Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active-low.

### CONTROL INPUTS

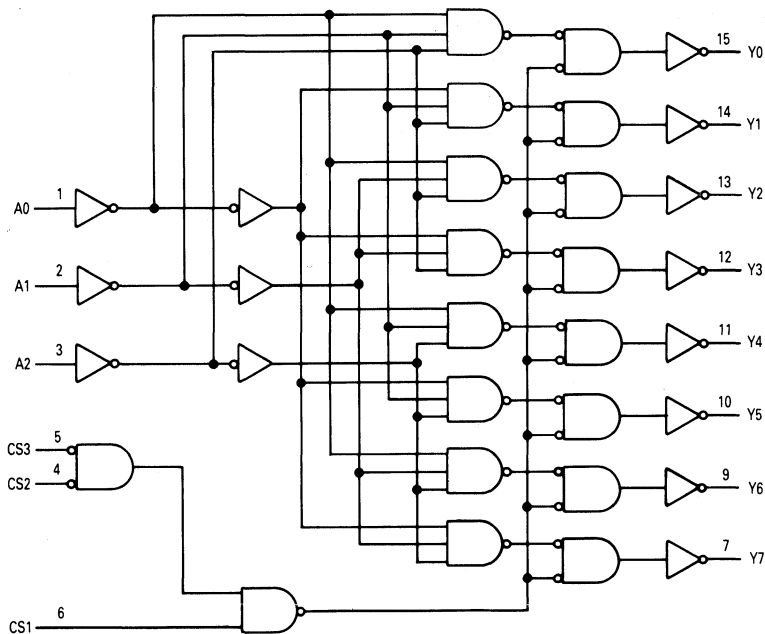
**CS1, CS2, CS3 (PINS 6, 4, 5)** — Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the outputs follow the Address inputs.

For any other combination of CS1, CS2, and CS3, the outputs are at a logic high.

### OUTPUTS

**Y0–Y7 (PINS 15, 14, 13, 12, 11, 10, 9, 7)** — Active-low Decoded outputs. These outputs assume a low level when addressed and the chip is selected. These outputs remain high when not addressed or the chip is not selected.

## EXPANDED LOGIC DIAGRAM



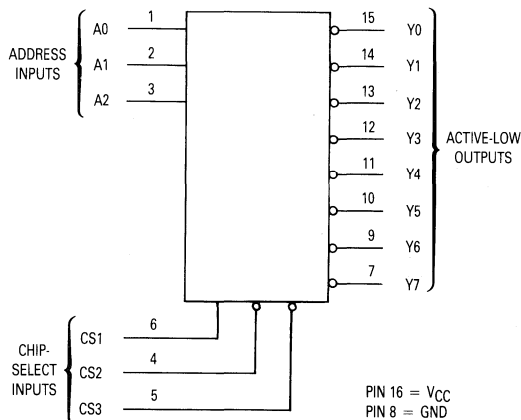
# 1-of-8 Decoder/Demultiplexer with LSTTL Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT138A is identical in pinout to the LS138. The HCT138A may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The HCT138A decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates

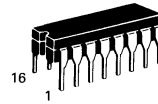
**LOGIC DIAGRAM**



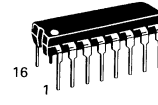
Design Criteria	Value	Units
Internal Gate Count*	30.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	.0075	pJ

\*Equivalent to a two-input NAND gate.

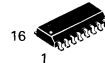
## MC54/74HCT138A



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**

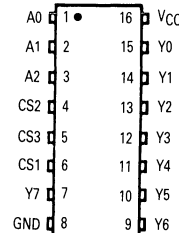


**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

**ORDERING INFORMATION**

MC74HCTXXXAN Plastic  
MC54HCTXXXAJ Ceramic  
MC74HCTXXXAD SOIC

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs			Outputs										
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	L	H	H	H	H	H	H
H	L	L	L	H	H	L	L	H	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	H	H	H	L
H	L	L	H	L	H	H	H	H	H	H	H	H	L
H	L	L	H	H	L	H	H	H	H	H	H	H	L

H = high level (steady state)

L = low level (steady state)

X = don't care



# MC54/74HCT138A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1.0 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 μA	4.5	3.98	3.84	3.7	μA
			5.5	0.26	0.33	0.4	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4.0	40	160	μA

ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTE: Information on typical parametric values can be found in Chapter 4.

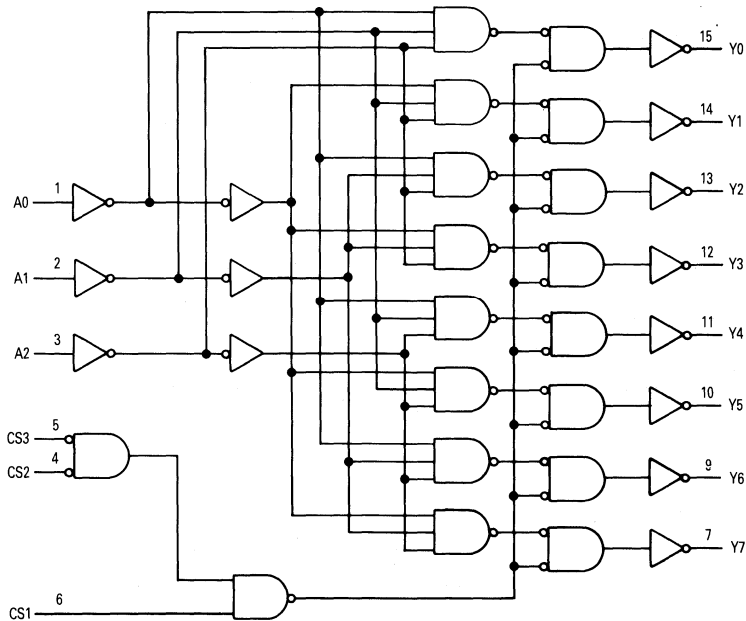
5

# MC54/74HCT138A

AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	30	38	45	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, CS1 to Output Y (Figures 2 and 4)	27	34	41	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Output Transition Time, CS2 or CS3 to Output Y (Figures 3 and 4)	30	38	45	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 2 and 4)	15	19	22	ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Time	500	500	500	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF
$C_{PD}$	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$			pF
		51			

EXPANDED LOGIC DIAGRAM



5

# MC54/74HCT138A

## SWITCHING WAVEFORMS

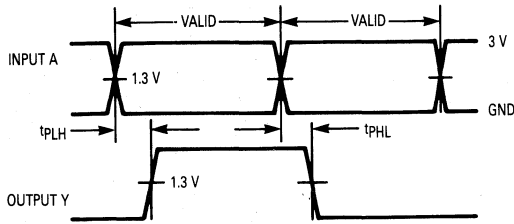


Figure 1.

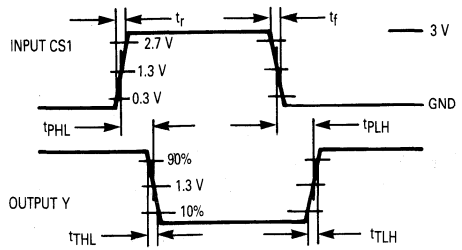


Figure 2.

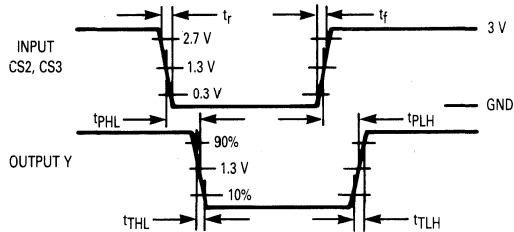
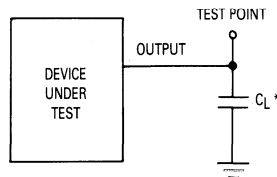


Figure 3.

## TEST CIRCUIT



\*Includes all probe and jig capacitance.

Figure 4.

## Dual 1-of-4 Decoder/ Demultiplexer

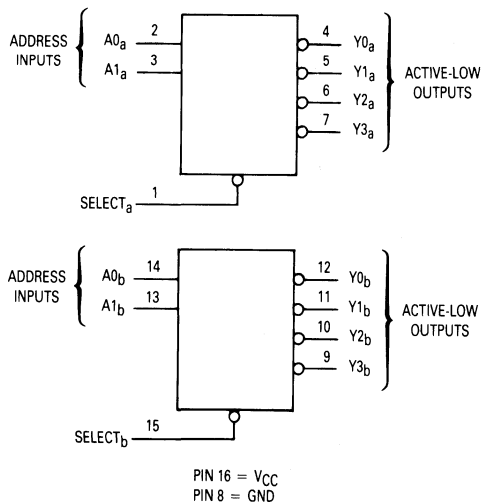
### High-Performance Silicon-Gate CMOS

The MC54/74HC139A is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

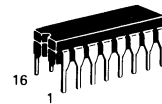
This device consists of two independent 1-of-4 decoders, each of which decodes a two-bit Address to one-of-four active-low outputs. Active-low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 25 Equivalent Gates

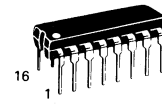
**LOGIC DIAGRAM**



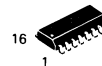
## MC54/74HC139A



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



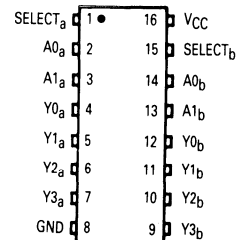
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXAD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Select	Inputs		Outputs			
	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don't care

# MC54/74HC139A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
6.0	5.48	5.34	5.20				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
6.0	0.26	0.33	0.40				
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC139A

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Select to Output Y (Figures 1 and 3)	2.0	115	145	175	ns
		4.5	23	29	35	
		6.0	20	25	30	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 3)	2.0	115	145	175	ns
		4.5	23	29	35	
		6.0	20	25	30	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Decoder) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		55	

## SWITCHING WAVEFORMS

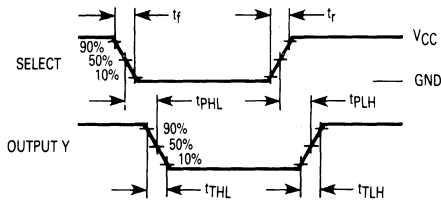


Figure 1.

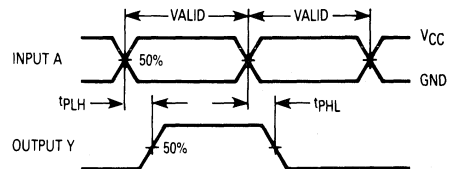
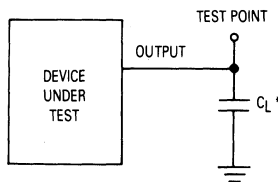


Figure 2.



\*Includes all probe and jig capacitance.

Figure 3. Test Circuit

# MC54/74HC139A

## PIN DESCRIPTIONS

### ADDRESS INPUTS

**A0<sub>a</sub>, A1<sub>a</sub>, A0<sub>b</sub>, A1<sub>b</sub> (PINS 2, 3, 14, 13)** — Address inputs. These inputs, when the respective 1-of-4 decoder is enabled, determine which of its four active-low outputs is selected.

### CONTROL INPUTS

**Select<sub>a</sub>, Select<sub>b</sub> (PINS 1, 15)** — Active-low select inputs. For a low level on this input, the outputs for that

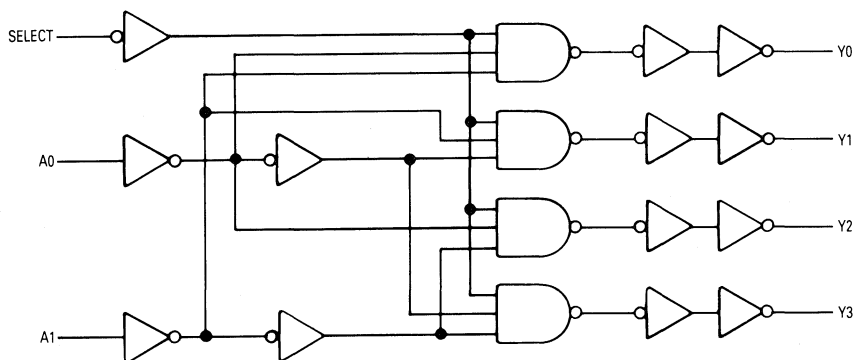
particular decoder follow the Address inputs. A high level on this input forces all outputs to a high level.

### OUTPUTS

**Y0<sub>a</sub>-Y3<sub>a</sub>, Y0<sub>b</sub>-Y3<sub>b</sub> (PINS 4-7, 12, 11, 10, 9)** — Active-low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

## EXPANDED LOGIC DIAGRAM

(1/2 of Device)



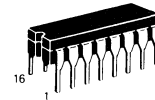
**MC54/74HC147**

**Decimal-to-BCD Encoder**  
**High-Performance Silicon-Gate CMOS**

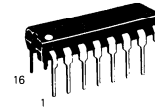
The MC54/74HC147 is identical in pinout to the LS147. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device encodes nine active-low data inputs to four active-low BCD Address Outputs, ensuring that only the highest order active data line is encoded. The implied decimal zero condition is encoded when all nine data inputs are at a high level (inactive).

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu A$
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



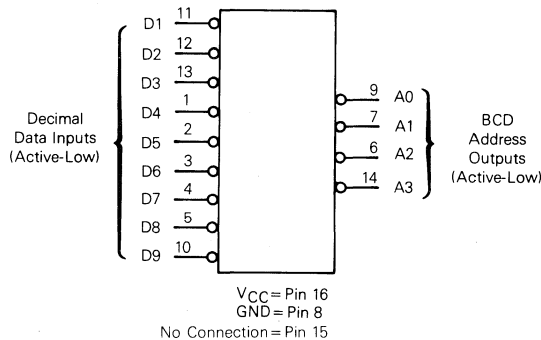
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

**ORDERING INFORMATION**

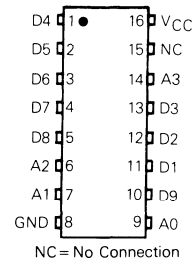
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ C$  for all packages.  
 Dimensions in Chapter 6.

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs									Outputs			
D9	D8	D7	D6	D5	D4	D3	D2	D1	A3	A2	A1	A0
H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	L
H	H	H	H	H	H	H	L	X	H	H	L	H
H	H	H	H	H	H	L	X	X	H	H	L	L
H	H	H	H	H	L	X	X	X	H	L	H	H
H	H	H	H	L	X	X	X	X	H	L	H	L
H	H	H	L	X	X	X	X	X	H	L	L	H
H	H	L	X	X	X	X	X	X	H	L	L	L
H	L	X	X	X	X	X	X	X	L	H	H	H
L	X	X	X	X	X	X	X	X	L	H	H	L

5



# MC54/74HC147

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	6.0	5.9	5.9	5.9	
			4.5	3.98	3.84	3.70	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	6.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.40	
6.0	0.26	0.33	0.40				
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC147

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input D to Output A (Figures 1 and 2)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

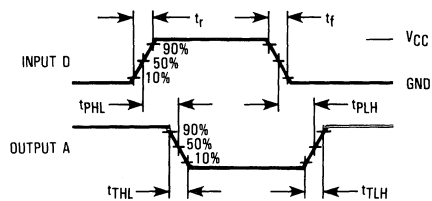
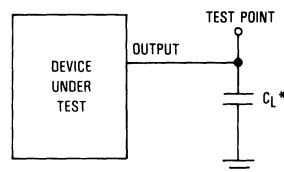


Figure 1. Switching Waveforms

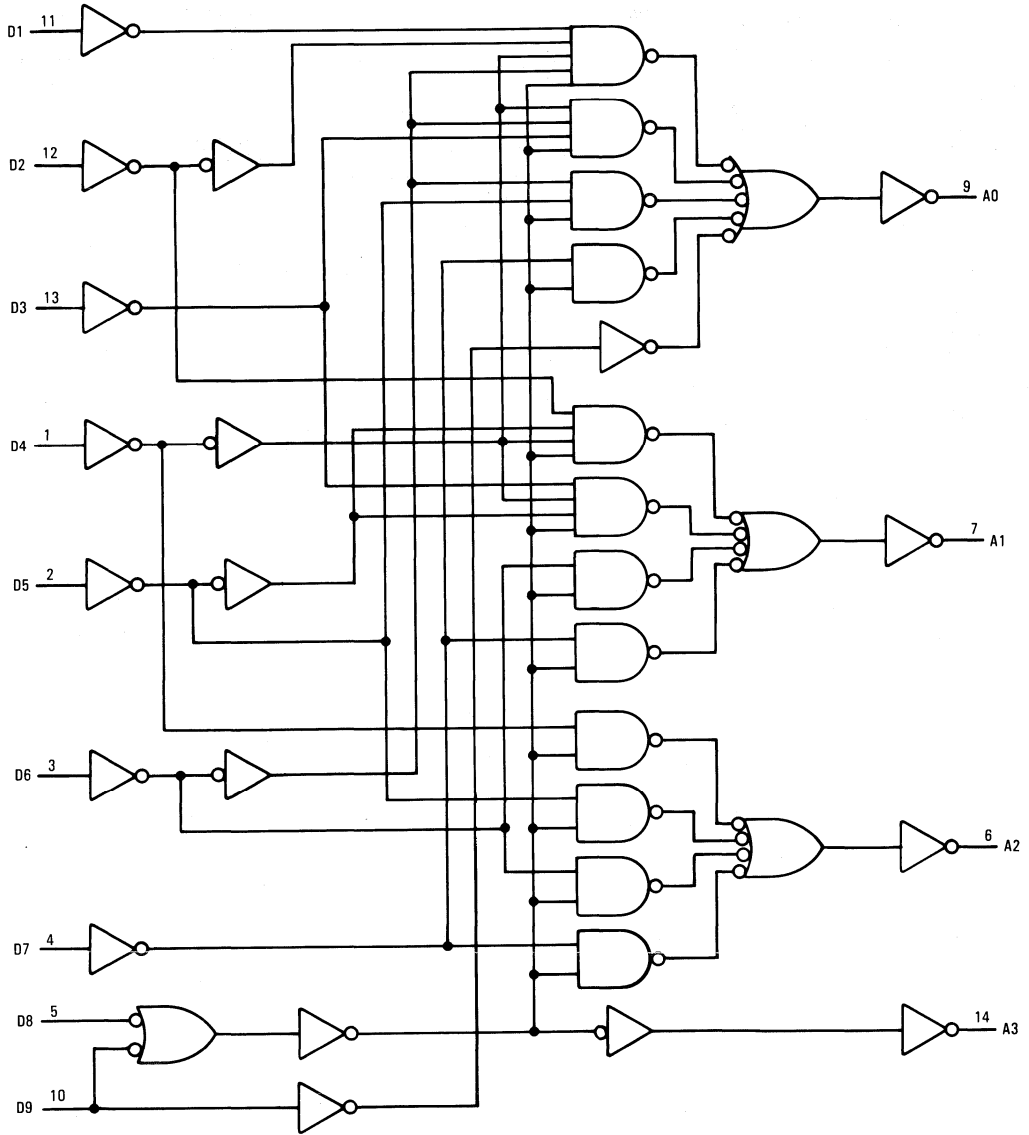


\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

# MC54/74HC147

## EXPANDED LOGIC DIAGRAM



5

# 8-Input Data Selector/Multiplexer

## High-Performance Silicon-Gate CMOS

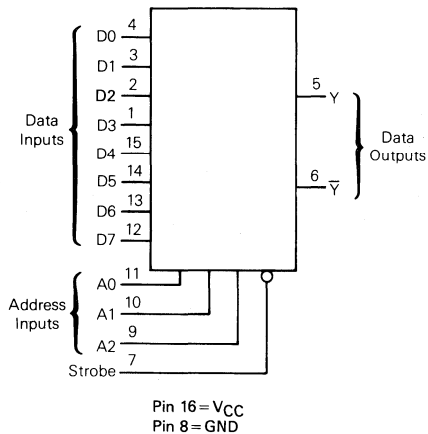
The MC54/74HC151 is identical in pinout to the LS151. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Strobe pin must be at a low level for the selected data to appear at the outputs. If Strobe is high, the Y output is forced to a low level and the  $\bar{Y}$  output is forced to a high level.

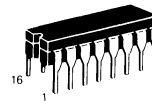
The HC151 is similar in function to the HC251 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 132 FETs or 33 Equivalent Gates

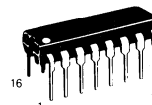
**LOGIC DIAGRAM**



## MC54/74HC151



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



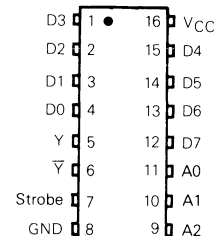
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs				Outputs	
A2	A1	A0	Strobe	Y	$\bar{Y}$
X	X	X	H	L	H
L	L	L	L	D0	$\bar{D}0$
L	L	H	L	D1	$\bar{D}1$
L	H	L	L	D2	$\bar{D}2$
L	H	H	L	D3	$\bar{D}3$
H	L	L	L	D4	$\bar{D}4$
H	L	H	L	D5	$\bar{D}5$
H	H	L	L	D6	$\bar{D}6$
H	H	H	L	D7	$\bar{D}7$

D0, D1, . . . D7 = the level of the respective D input

# MC54/74HC151

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package‡	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	0.26	0.33	0.40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC151

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input D to Output Y or $\bar{Y}$ (Figures 1, 3 and 6)	2.0	185	230	280	ns
		4.5	37	46	56	
		6.0	31	39	48	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y or $\bar{Y}$ (Figures 2 and 6)	2.0	205	255	310	ns
		4.5	41	51	62	
		6.0	35	43	53	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Strobe to Output Y or $\bar{Y}$ (Figures 4, 5 and 6)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		36	

## PIN DESCRIPTIONS

### INPUTS

D0, D1, . . . , D7 (PINS 4, 3, 2, 1, 15, 14, 13, 12) — Data inputs. Data on any one of these eight binary inputs may be selected to appear on the output.

### CONTROL INPUTS

A0, A1, A2 (PINS 11, 10, 9) — Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

STROBE (PIN 7) — Strobe. This input pin must be at a low level for the selected data to appear at the outputs. If the Strobe pin is high, the Y output is forced to a low level and the  $\bar{Y}$  output is forced to a high level.

### OUTPUTS

Y,  $\bar{Y}$  (PINS 5, 6) — Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ( $\bar{Y}$  output) forms.

# MC54/74HC151

## SWITCHING WAVEFORMS

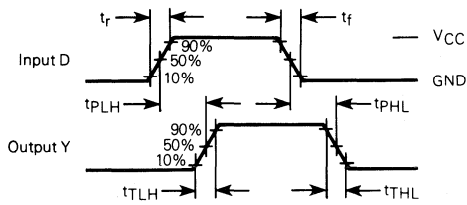


Figure 1.

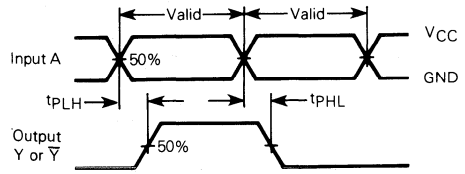


Figure 2.

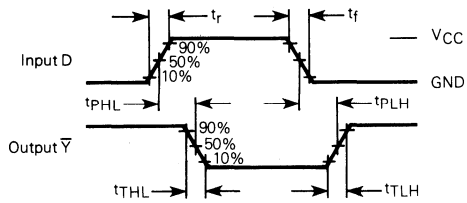


Figure 3.

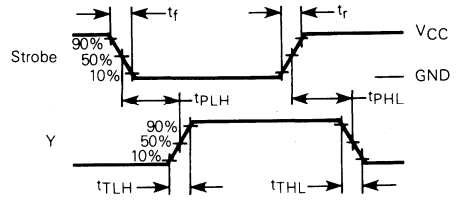


Figure 4.

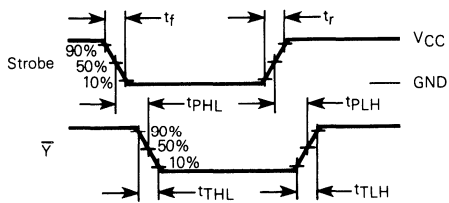
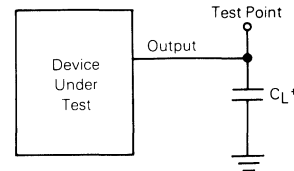


Figure 5.

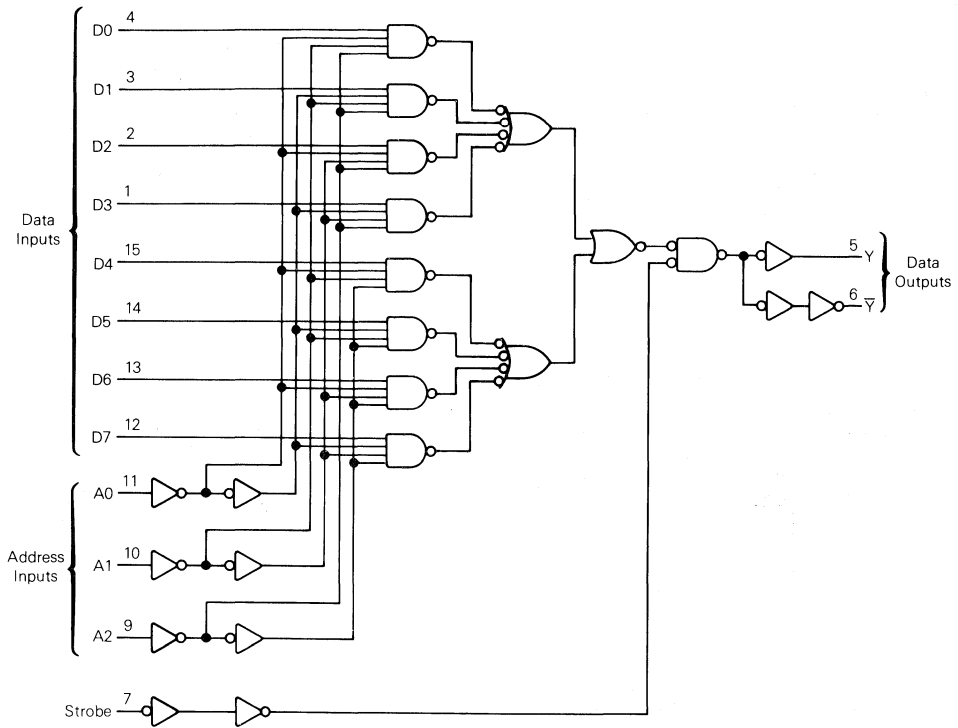


\* Includes all probe and jig capacitance.

Figure 6. Test Circuit

# MC54/74HC151

## EXPANDED LOGIC DIAGRAM



5



## Dual 4-Input Data Selector/Multiplexer

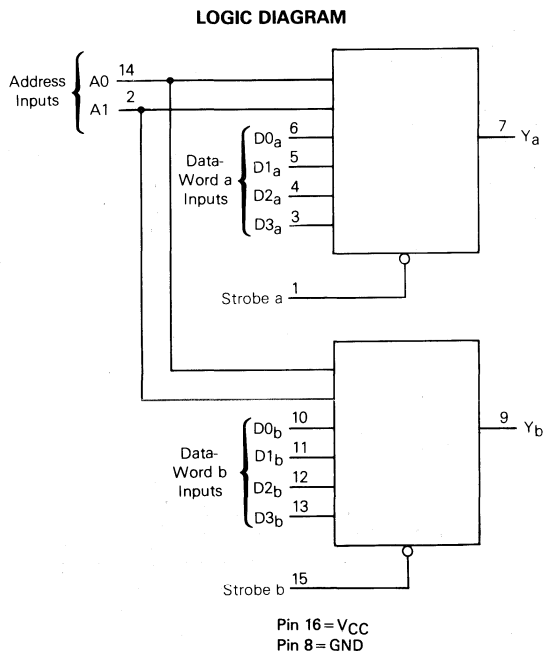
### High-Performance Silicon-Gate CMOS

The MC54/74HC153 is identical in pinout to the LS153. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

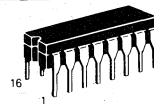
The Address Inputs select one of four Data Inputs from each multiplexer. Each multiplexer has an active-low Strobe control and a noninverting output.

The HC153 is similar in function to the HC253, which has 3-state outputs.

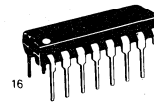
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates



## MC54/74HC153



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT

Strobe a	1	16	VCC
A1	2	15	Strobe b
D3a	3	14	A0
D2a	4	13	D3b
D1a	5	12	D2b
D0a	6	11	D1b
Ya	7	10	D0b
GND	8	9	Yb

### FUNCTION TABLE

Inputs			Output
A1	A0	Strobe	Y
X	X	H	L
L	L	L	D0
L	H	L	D1
H	L	L	D2
H	H	L	D3

D0, D1, D2, and D3 = the level of the respective Data Input

# MC54/74HC153

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit			
				25°C to -55°C	≤85°C	≤125°C				
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V			
			4.5	3.15	3.15	3.15				
			6.0	4.2	4.2	4.2				
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V			
			4.5	0.9	0.9	0.9				
			6.0	1.2	1.2	1.2				
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V			
			4.5	4.4	4.4	4.4				
			6.0	5.9	5.9	5.9				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V			
			4.5	0.1	0.1	0.1				
			6.0	0.1	0.1	0.1				
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA			
			I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0		8	80	160

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC153

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input D to Output Y (Figures 1 and 4)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Strobe to Output Y (Figures 3 and 4)	2.0	95	120	145	ns
		4.5	19	24	29	
		6.0	16	20	25	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Multiplexer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		31	

## SWITCHING WAVEFORMS

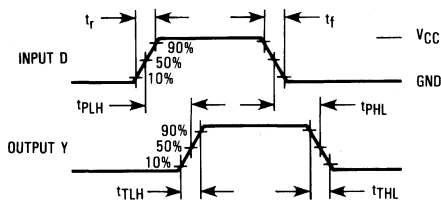


Figure 1

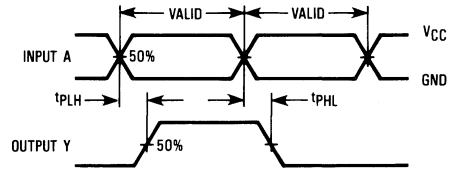


Figure 2

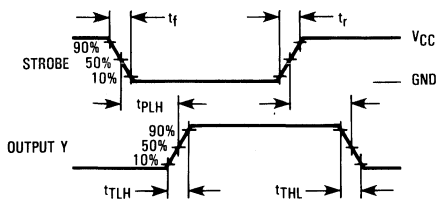
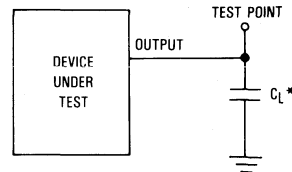


Figure 3



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

# MC54/74HC153

## PIN DESCRIPTIONS

### DATA INPUTS

**D0<sub>a</sub>-D3<sub>a</sub>, D0<sub>b</sub>-D3<sub>b</sub> (PINS 3, 4, 5, 6, 10, 11, 12, 13)** — Data Inputs. With the outputs enabled, the addressed Data Inputs appear at the Y outputs.

### CONTROL INPUTS

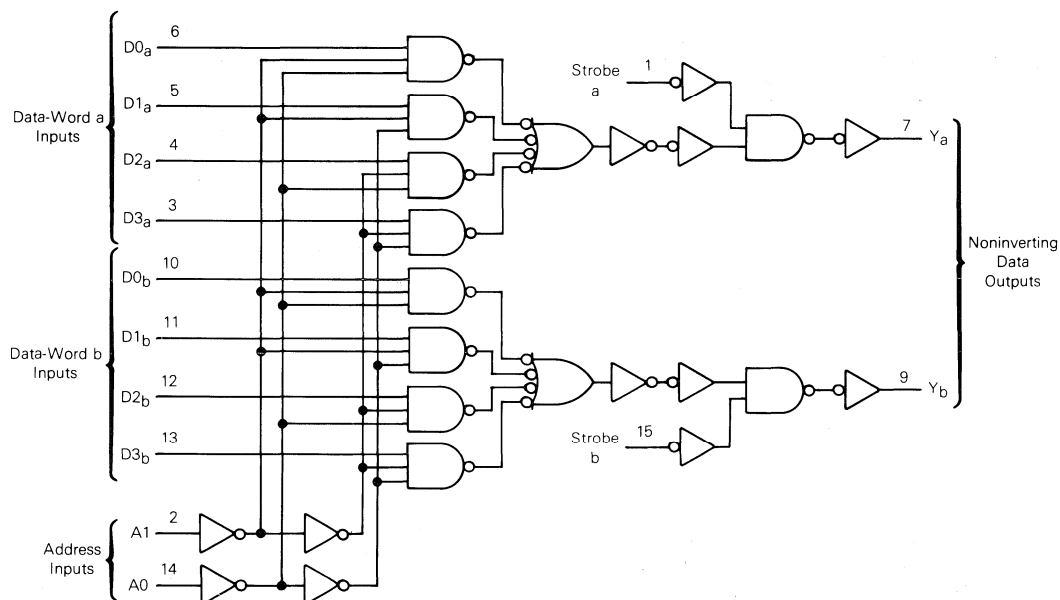
**A0, A1 (PINS 2, 14)** — Address Inputs. These inputs address the pair of Data Inputs which appear at the corresponding outputs.

**STROBE (PINS 1, 15)** — Active-low Strobe. A low level applied to these pins enables the corresponding outputs.

### OUTPUTS

**Y<sub>a</sub>, Y<sub>b</sub> (PINS 7, 9)** — Noninverting data outputs.

## EXPANDED LOGIC DIAGRAM



# 1-of-16 Decoder/Demultiplexer

## High-Performance Silicon-Gate CMOS

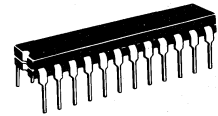
The MC54/74HC154 is identical in pinout to the LS154. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device, when enabled, selects one of 16 active-low outputs. Two active-low Chip Selects are provided to facilitate the chip-select, demultiplexing, and cascading functions. When either Chip Select is high, all outputs are high. The demultiplexing function is accomplished by using the Address inputs to select the desired device output. Then, while holding one chip select input low, data can be applied to the other chip select input (see Application Note).

The HC154 is primarily used for memory address decoding and data routing applications.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 192 FETs or 48 Equivalent Gates

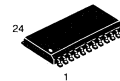
### MC54/74HC154



**J SUFFIX**  
**CERAMIC**  
 CASE 758-01



**N SUFFIX**  
**PLASTIC**  
 CASE 724-03



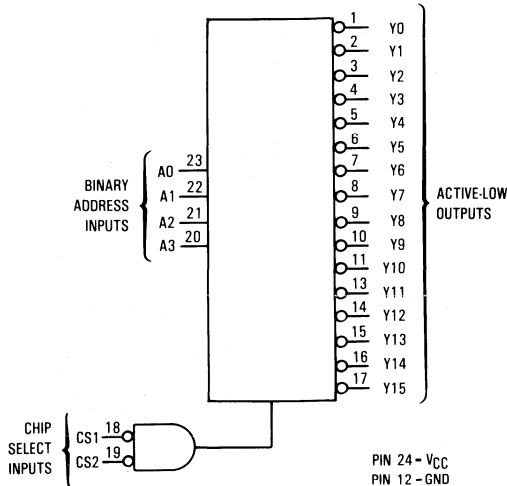
**DW SUFFIX**  
**PLASTIC**  
 CASE 751E-03

#### ORDERING INFORMATION

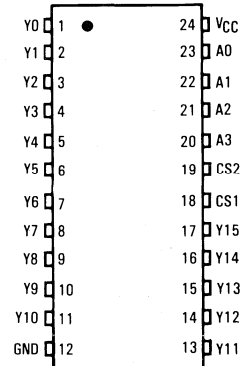
MC74HCXXDW SOIC  
 MC74HCXXN Plastic  
 MC54HCXXJ Ceramic

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT



# MC54/74HC154

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP or SOIC Package)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.  
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	0.26	0.33	0.40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA
			6.0	8	80	160	
			6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HC154

## SWITCHING WAVEFORMS

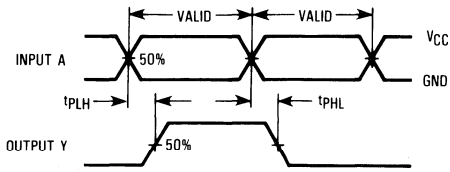


Figure 1.

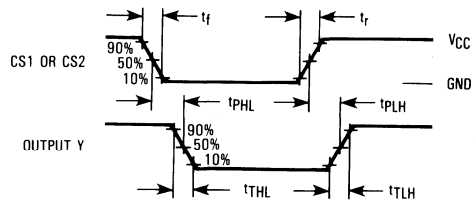
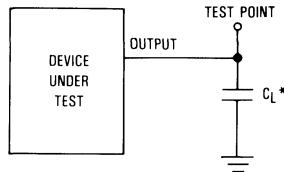


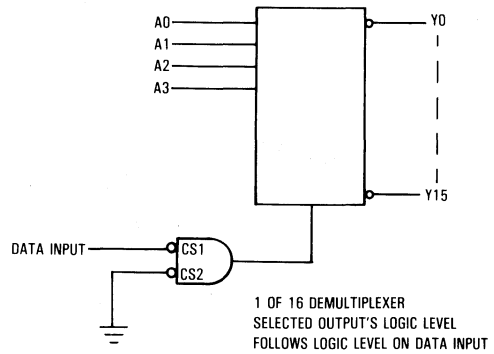
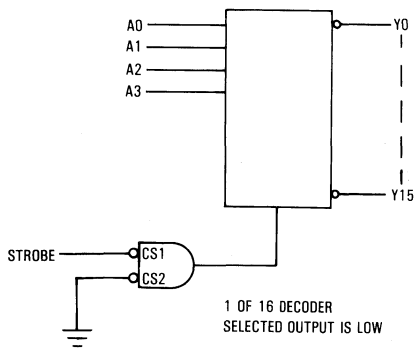
Figure 2.



\*Includes all probe and jig capacitance.

Figure 3. Test Circuit

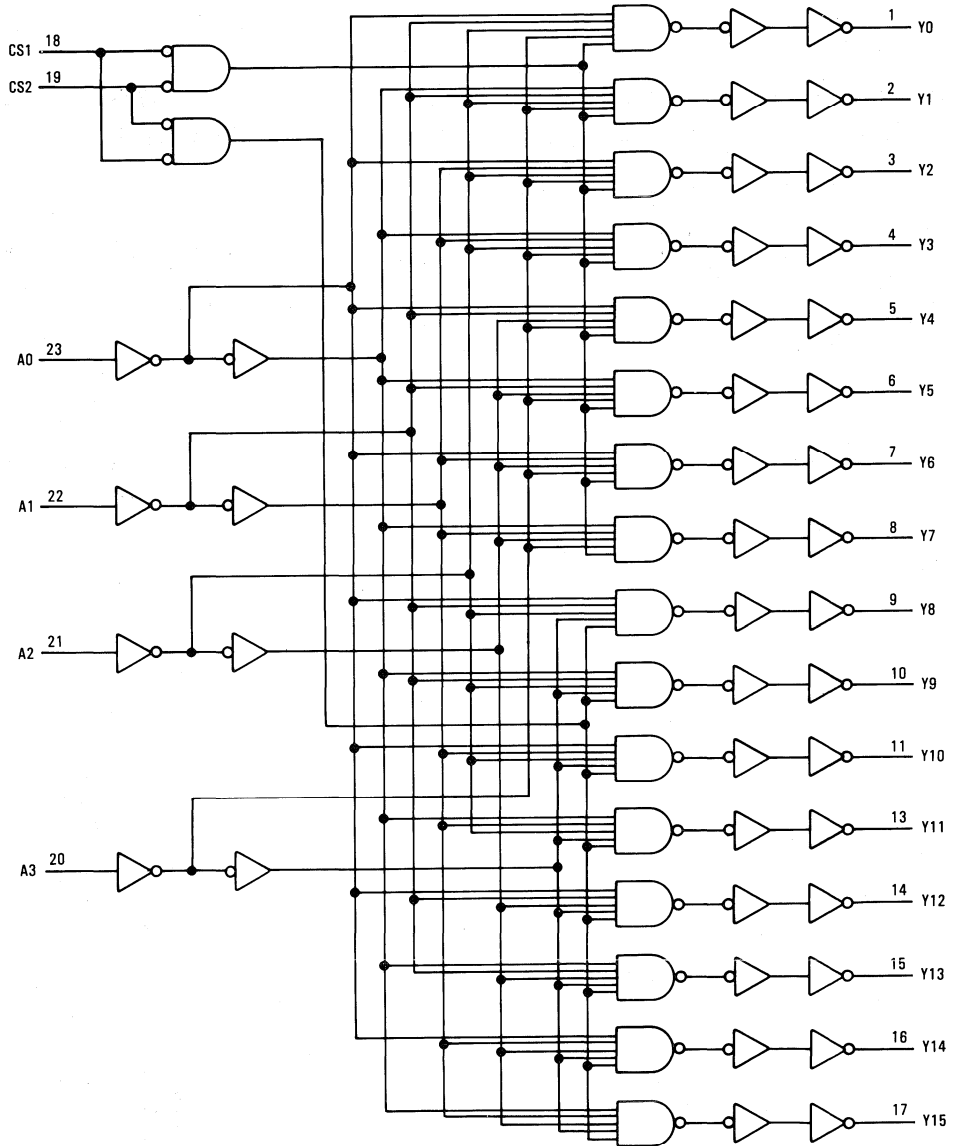
## TYPICAL APPLICATIONS





# MC54/74HC154

## EXPANDED LOGIC DIAGRAM



## Quad 2-Input Data Selectors/Multiplexers

### High-Performance Silicon-Gate CMOS

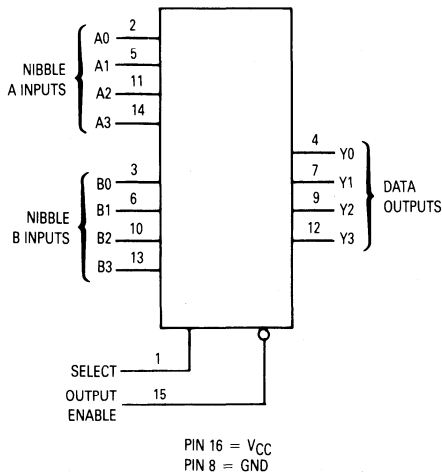
The MC54/74HC157A is identical in pinout to the LS157. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device routes 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form. A high level on the Output Enable input sets all four Y outputs to a low level.

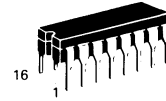
The HC157A is similar in function to the HC257 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 82 FETs or 20.5 Equivalent Gates

**LOGIC DIAGRAM**



## MC54/74HC157A



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



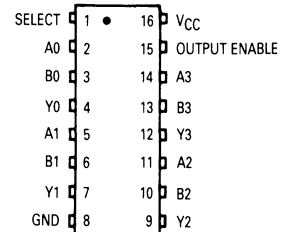
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXXAN Plastic  
 MC54HCXXXAJ Ceramic  
 MC74HCXXXAD SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Outputs Y0-Y3
Output Enable	Select	
H	X	L
L	L	A0-A3
L	H	B0-B3

X = don't care  
 A0-A3, B0-B3 = the levels of  
 the respective Data-Word  
 Inputs.

# MC54/74HC157A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC157A

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6.0$  ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
tPLH, tPHL	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 4)	2.0	105	130	160	ns
		4.5	21	26	32	
		6.0	18	22	27	
tPLH, tPHL	Maximum Propagation Delay, Select to Output Y (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
tPLH, tPHL	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		33	

## PIN DESCRIPTIONS

### INPUTS

**A0, A1, A2, A3 (PINS 2, 5, 11, 14)** — Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

**B0, B1, B2, B3 (PINS 3, 6, 10, 13)** — Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

### OUTPUTS

**Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12)** — Data outputs. The selected input Nibble is presented at these outputs when

the Output Enable input is at a low level. The data present on these pins is in its noninverted form. For the Output Enable input at a high level, the outputs are at a low level.

### CONTROL INPUTS

**SELECT (PIN 1)** — Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

**OUTPUT ENABLE (PIN 15)** — Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level.

# MC54/74HC157A

## SWITCHING WAVEFORMS

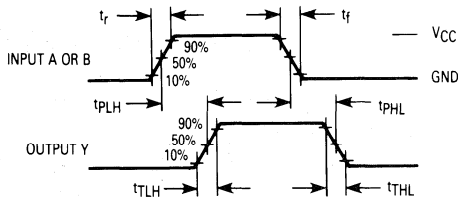


Figure 1. HC157A

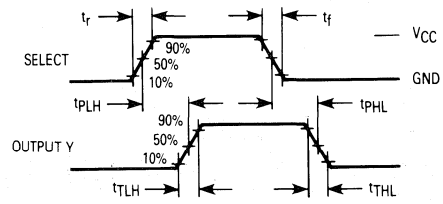


Figure 2. Y versus Select, Noninverted

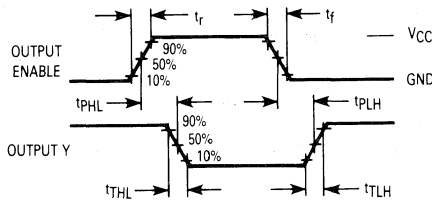
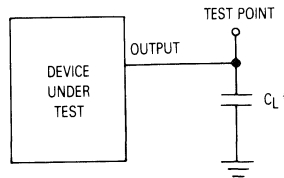


Figure 3. HC157A

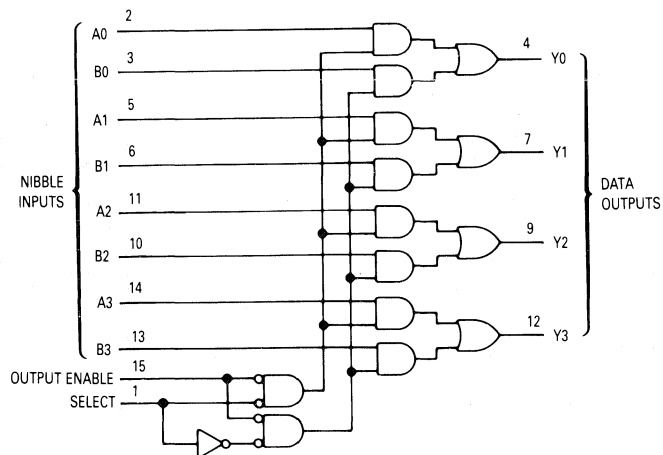


\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

5

## EXPANDED LOGIC DIAGRAM



## Quad 2-Input Data Selector/Multiplexer with LSTTL Compatible Inputs High-Performance Silicon-Gate CMOS

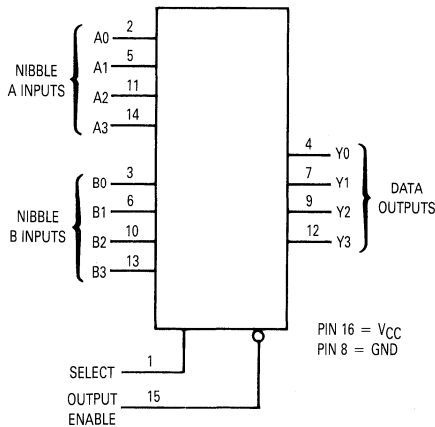
The MC54/74HCT157A is identical in pinout to the LS157. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device routes 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form. A high level on the Output Enable input sets all four Y outputs to a low level.

The HCT157A is similar in function to the HC257 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 102 FETs or 25.5 Equivalent Gates

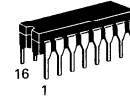
### LOGIC DIAGRAM



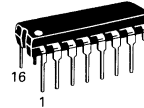
Design Criteria	Value	Unit
Internal Gate Count*	25.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	0.005	$\mu$ W
Speed Power Product	0.0075	pJ

\*Equivalent to a two-input NAND gate.

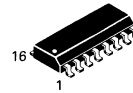
## MC54/74HCT157A



J SUFFIX  
 CERAMIC  
 CASE 620-09



N SUFFIX  
 PLASTIC  
 CASE 648-08

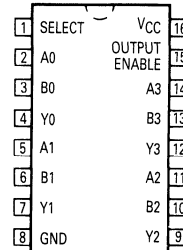


D SUFFIX  
 SOIC  
 CASE 751B-04

### ORDERING INFORMATION

MC74HCTXXAN	Plastic
MC54HCTXXAJ	Ceramic
MC74HCTXXAD	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Outputs Y0-Y3
Output Enable	Select	
H	X	L
L	L	A0-A3
L	H	B0-B3

X = Don't Care  
 A0-A3, B0-B3 = the levels of the respective Data-Word inputs.

# MC54/74HCT157A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	0.26	0.33	0.4	V
			5.5	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4.0	40	160	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HCT157A

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 4)	27	34	41	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Select to Output Y (Figures 2 and 4)	37	46	56	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	30	38	45	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Time	500	500	500	ns
$C_{PD}$	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical ( $\alpha$ 25°C, $V_{CC} = 5.0\text{ V}$ )			pF
		64			

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see the Motorola High-Speed CMOS Logic Data Book — DL129/D.

## PIN DESCRIPTIONS

### INPUTS

**A0, A1, A2, A3 (Pins 2, 5, 11, 14)** — Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

**B0, B1, B2, B3 (Pins 3, 6, 10, 13)** — Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

### OUTPUTS

**Y0, Y1, Y2, Y3 (Pins 4, 7, 9, 12)** — Data outputs. The selected input Nibble is presented at these outputs

when the Output Enable input is at a low level. The data is presented to the outputs in noninverted form. For the Output Enable input at a high level, the outputs are at a low level.

### CONTROL INPUTS

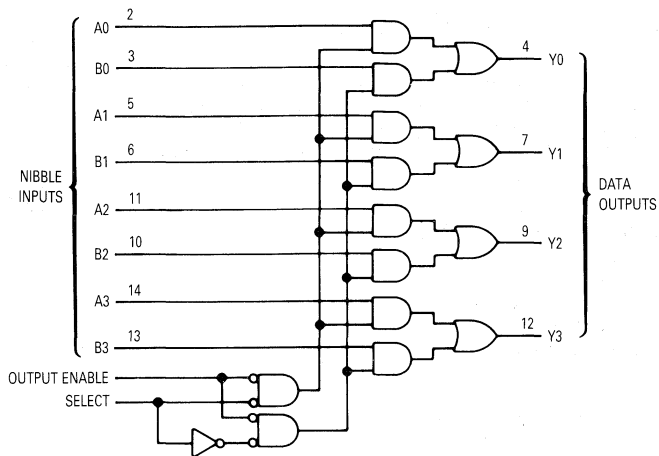
**Select (Pin 1)** — Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

**Output Enable (Pin 15)** — Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level.



# MC54/74HCT157A

## EXPANDED LOGIC DIAGRAM



## SWITCHING WAVEFORMS

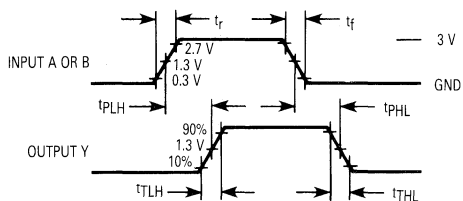


Figure 1.

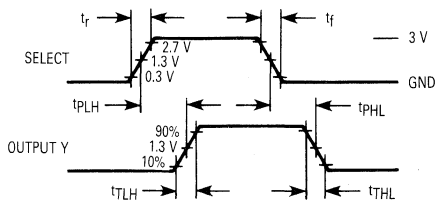


Figure 2.

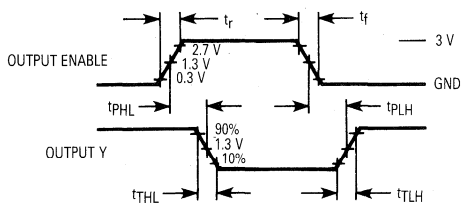
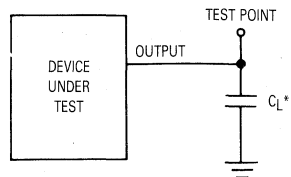


Figure 3.



\*Includes all probe and jig capacitance

Figure 4. Test Circuit

## Pre-settable Counters

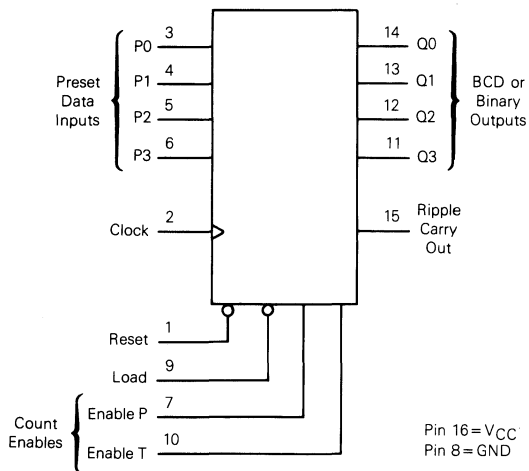
### High-Performance Silicon-Gate CMOS

The MC54/74HC160 and HC162 are identical in pinout to the LS160 and LS162, respectively. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC160 and HC162 are programmable BCD counters with asynchronous and synchronous Reset inputs, respectively.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates

#### LOGIC DIAGRAM



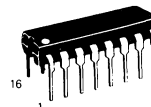
Device	Count Mode	Reset Mode
HC160	BCD	Asynchronous
HC162	BCD	Synchronous

## MC54/74HC160

## MC54/74HC162



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



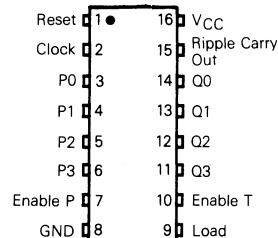
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

#### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Clock	Inputs				Output Q
	Reset*	Load	Enable P	Enable T	
	L	X	X	X	Reset
	H	L	X	X	Load Preset Data
	H	H	H	H	Count
	H	H	L	X	No Count
	H	H	X	L	No Count

\* HC162 only. HC160 is an Asynchronous-Reset Device

H = high level  
 L = low level  
 X = don't care

# MC54/74HC160 • MC54/74HC162

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC160 • MC54/74HC162

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)* (Figures 1 and 7)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 7)	2.0	170	215	255	ns
		4.5	34	43	51	
		6.0	29	37	43	
t <sub>PHL</sub>		2.0	205	255	310	
		4.5	41	51	62	
		6.0	35	43	53	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (HC160 Only) (Figures 2 and 7)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t <sub>PLH</sub>	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 3 and 7)	2.0	160	200	240	ns
		4.5	32	40	48	
		6.0	27	34	41	
t <sub>PHL</sub>		2.0	195	245	295	
		4.5	39	49	59	
		6.0	33	42	50	
t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Ripple Carry Out (Figures 1 and 7)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PHL</sub>		2.0	215	270	325	
		4.5	43	54	65	
		6.0	37	46	55	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Ripple Carry Out (HC160 Only) (Figures 2 and 7)	2.0	220	275	330	ns
		4.5	44	55	66	
		6.0	37	47	56	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 7)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

\*Applies to noncascaded/nonsynchronously clocked configurations only. With synchronously cascaded counters, (1) Clock to Ripple Carry Out propagation delays, (2) Enable T or Enable P to Clock setup times, and (3) Clock to Enable T or Enable P hold times determine f<sub>max</sub>. However, if Ripple Carry Out of each stage is tied to the Clock of the next stage (nonsynchronously clocked), the f<sub>max</sub> in the table above is applicable. See Applications Information in this data sheet.

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		60	

5

## MC54/74HC160 • MC54/74HC162

### TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Preset Data Inputs to Clock (Figure 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>su</sub>	Minimum Setup Time, Load to Clock (Figure 5)	2.0	135	170	205	ns
		4.5	27	34	41	
		6.0	23	29	35	
t <sub>su</sub>	Minimum Setup Time, Reset to Clock (HC162 only) (Figure 4)	2.0	160	200	240	ns
		4.5	32	40	48	
		6.0	27	34	41	
t <sub>su</sub>	Minimum Setup Time, Enable T or Enable P to Clock (Figure 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t <sub>h</sub>	Minimum Hold Time, Clock to Preset Data Inputs (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t <sub>h</sub>	Minimum Hold Time, Clock to Load (Figure 5)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>h</sub>	Minimum Hold Time, Clock to Reset (HC162 only) (Figure 4)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>h</sub>	Minimum Hold Time, Clock to Enable T or Enable P (Figure 6)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (HC160 only) (Figure 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>rec</sub>	Minimum Recovery Time, Load Inactive to Clock (Figure 5)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (HC160 only) (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

**FUNCTION DESCRIPTION**

The HC160/162 are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count-enable controls.

The HC160 and HC162 are BCD counters with asynchronous Reset, and synchronous Reset, respectively.

**INPUTS**

**Clock (Pin 2)** — The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting (HC162) and loading occur with the rising edge of the Clock input.

**Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)** — These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (pin 3) is the least-significant bit and P3 (pin 6) is the most-significant bit.

**OUTPUTS**

**Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)** — These are the counter outputs (BCD or binary). Q0 (pin 14) is the least-significant bit and Q3 (pin 11) is the most-significant bit.

**Ripple Carry Out (Pin 15)** — When the counter is in its maximum state (1001 for the BCD counters or 1111 for the binary counters), this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

$$\text{Ripple Carry Out} = \text{Enable T} \bullet \text{Q0} \bullet \overline{\text{Q1}} \bullet \overline{\text{Q2}} \bullet \text{Q3}$$

for BCD counters HC160 and HC162

**CONTROL FUNCTIONS**

**Resetting** — A low level on the Reset pin (pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to a low level. The HC160 resets asynchronously and the HC162 resets with the rising edge of the Clock input (synchronous reset).

**Loading** — With the rising edge of the Clock, a low level on Load (pin 9) loads the data from the Preset Data Input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Although the HC160 and HC162 are BCD counters, they may be programmed to any state. If they are loaded with a state disallowed in BCD code, they will return to their normal count sequence within two clock pulses (see the Output State Diagram).

**Count Enable/Disable** — These devices have two count-enable control pins: Enable P (pin 7) and Enable T (pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \bullet \text{Enable T} \bullet \text{Load}$$

The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control; Enable T is both a count-enable and a Ripple-Carry Output control.

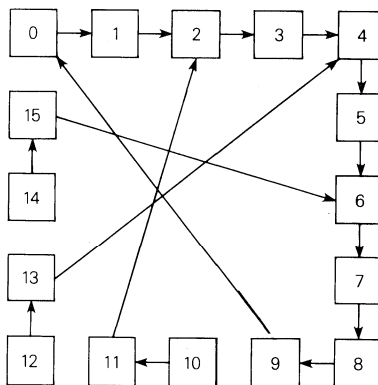
**TABLE 1. COUNT ENABLE/DISABLE**

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0-Q3	Ripple Carry Out
H	H	H	Count	High when Q0-Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0-Q3 are maximum*
X	X	L	No Count	L

\*Q0 through Q3 are maximum for the HC160 and HC162 when Q3 Q2 Q1 Q0 = 1001.

**OUTPUT STATE DIAGRAMS**

**HC160 and HC162  
BCD Counters**



# MC54/74HC160 • MC54/74HC162

## SWITCHING WAVEFORMS

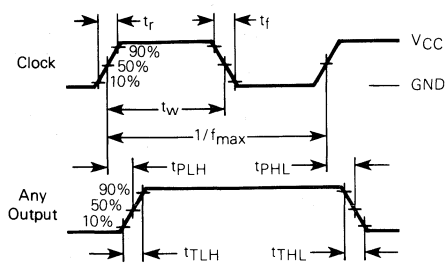


Figure 1.

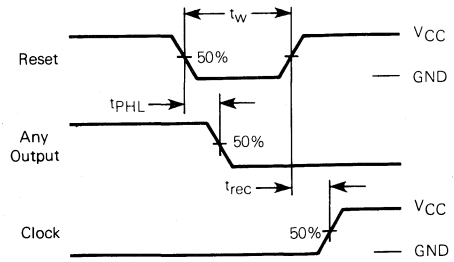


Figure 2.

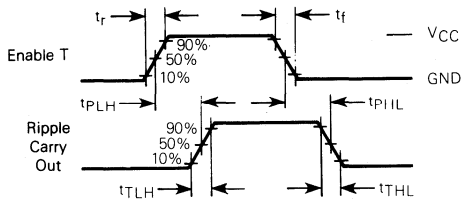


Figure 3.

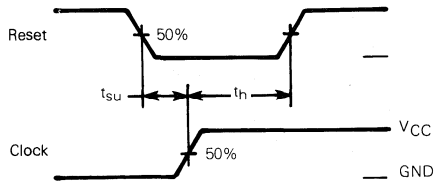


Figure 4. HC162 and HC163 Only.

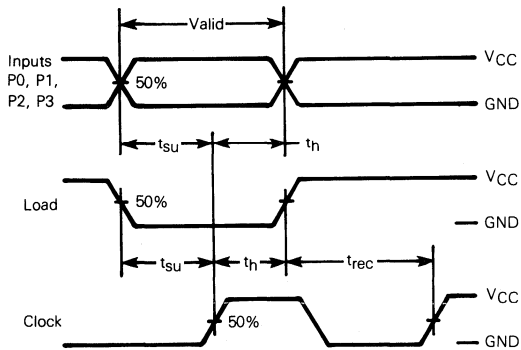


Figure 5.

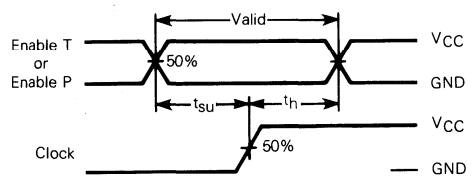
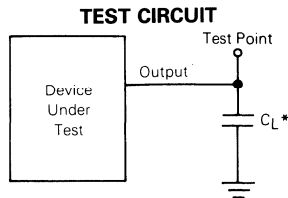


Figure 6.

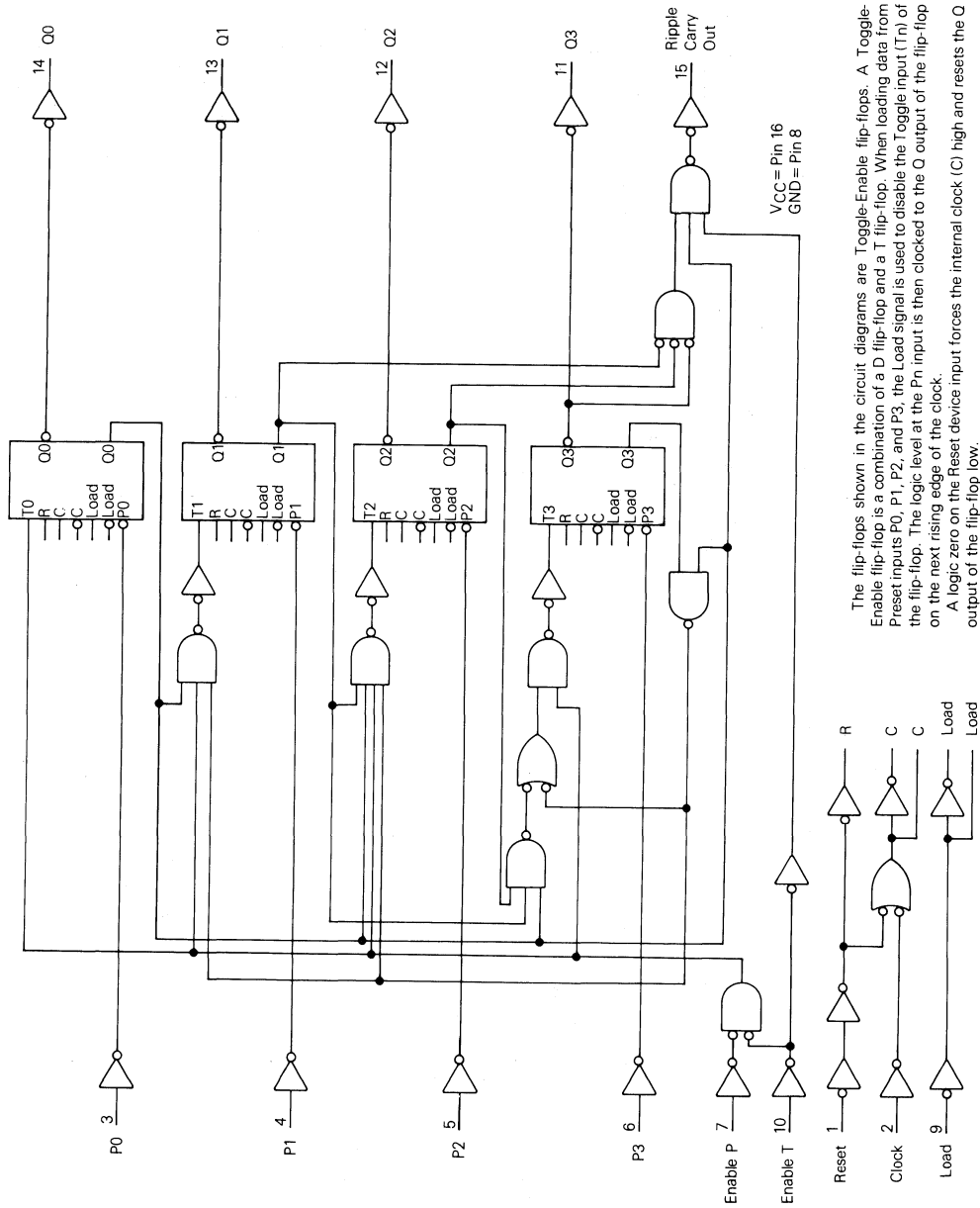


\* Includes all probe and jig capacitance.

Figure 7.

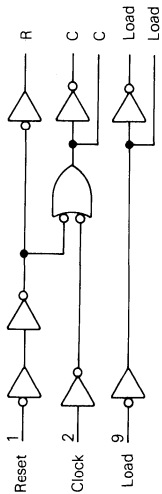
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MC54HC160 • MC74HC160  
BCD Counter with Asynchronous Reset



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.



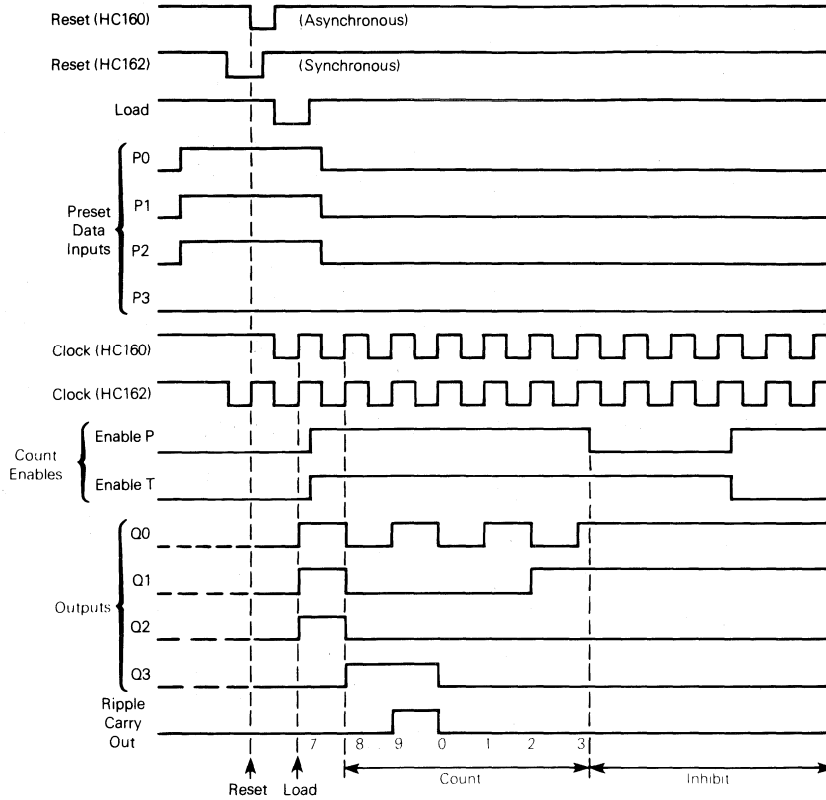


# MC54/74HC160 • MC54/74HC162

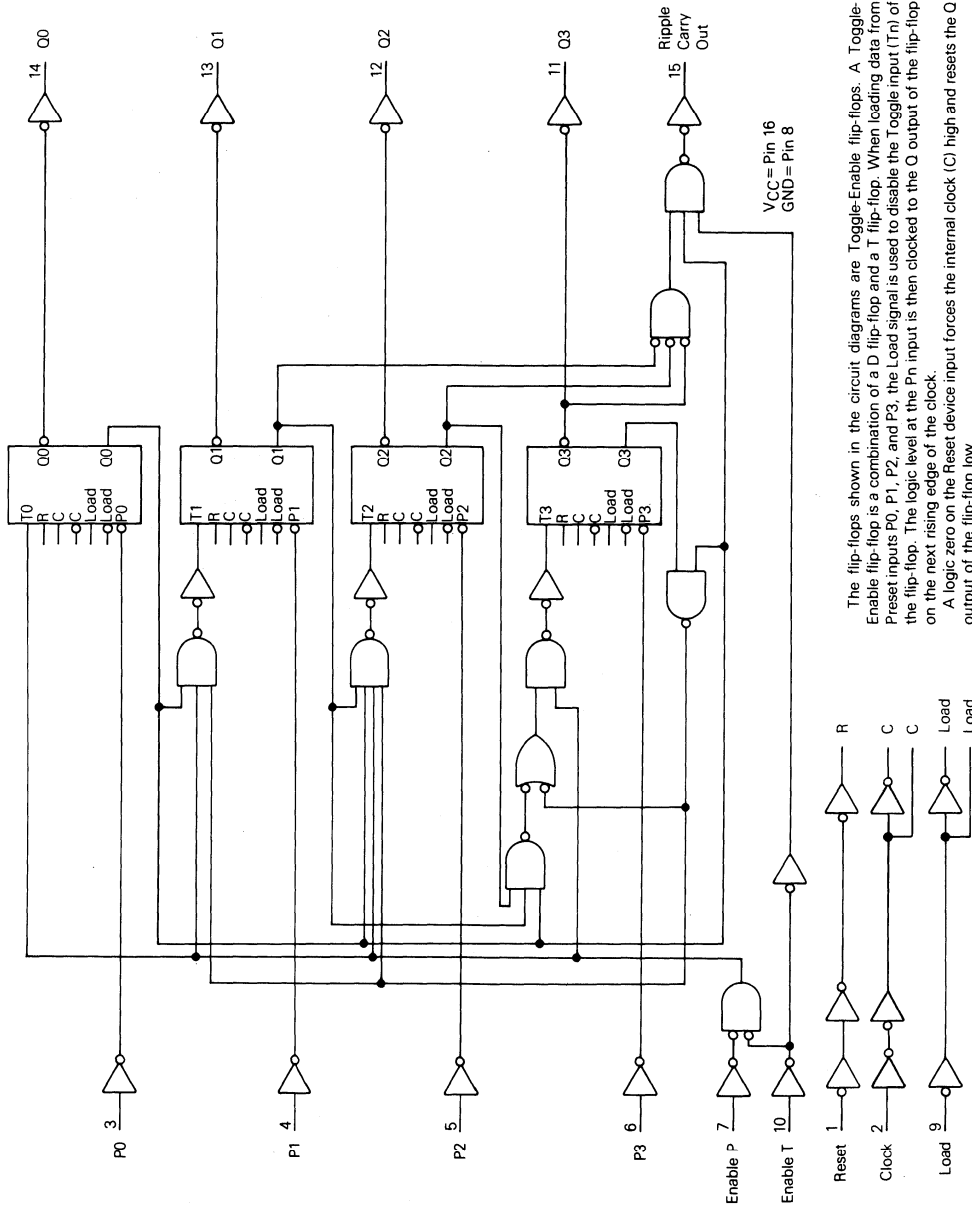
## HC160, HC162 TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.



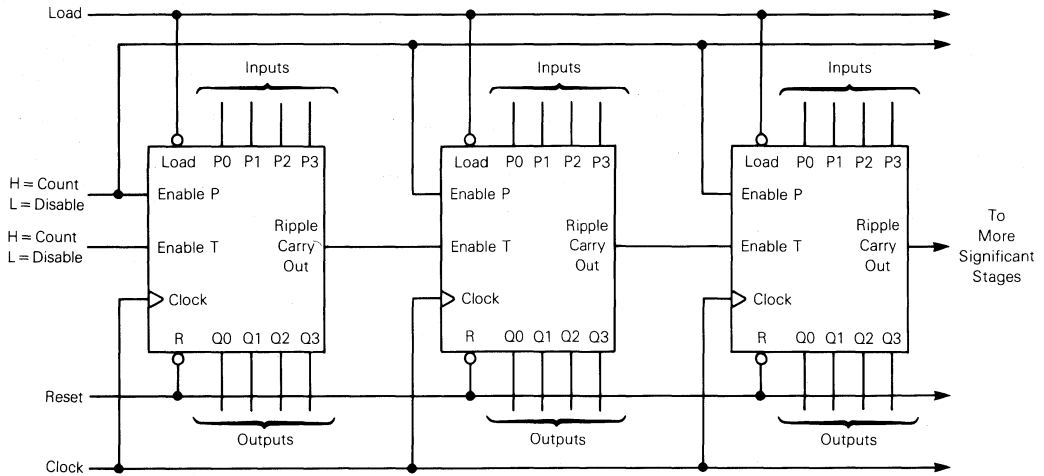
MC54HC162 • MC74HC162  
BCD Counter with Synchronous Reset



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When leading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tr) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.  
A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

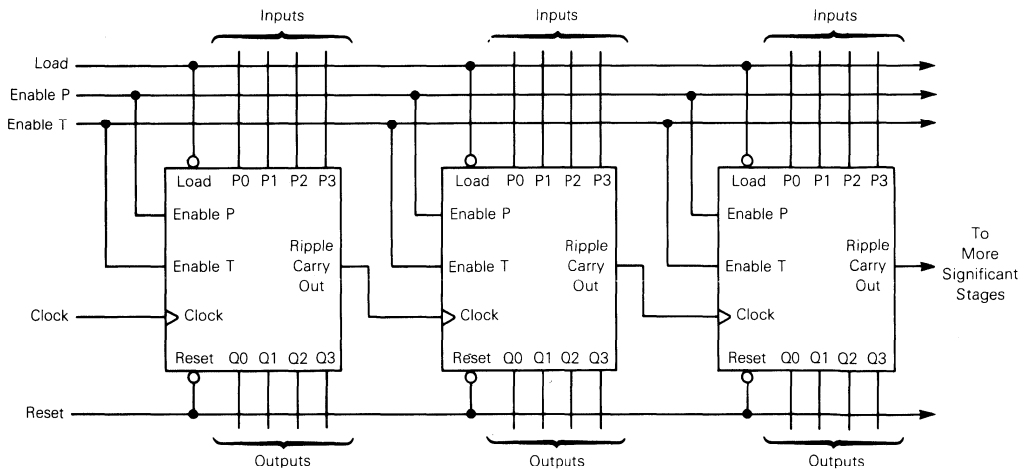
TYPICAL APPLICATIONS  
CASCADING

N-Bit Synchronous Counters

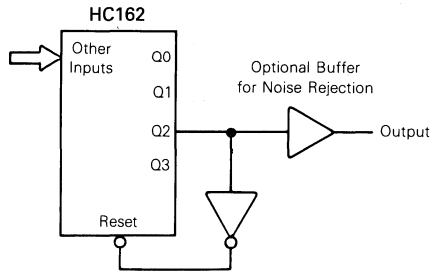


NOTE: When used in these cascaded configurations the clock  $f_{max}$  guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.

Nibble Ripple Counter



TYPICAL APPLICATION



Modulo-5 Counter

The HC162 facilitates designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous Reset.

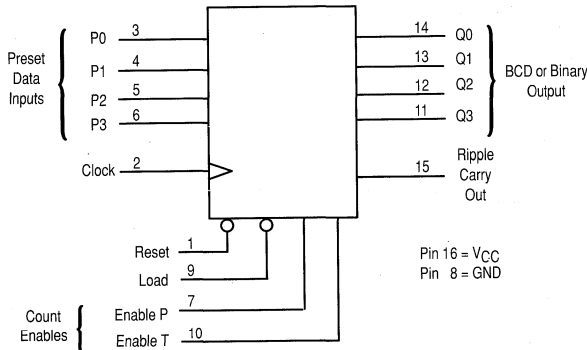
**Presettable Counters**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC161A and HC163A are identical in pinout to the LS161 and LS163. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC161A and HC163A are programmable 4-bit binary counters with asynchronous and synchronous reset, respectively.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 192 FETs or 48 Equivalent Gates

**LOGIC DIAGRAM**

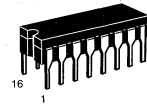


**FUNCTION TABLE**

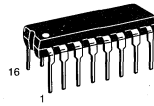
Clock	Inputs				Output Q
	Reset*	Load	Enable P	Enable T	
	L	X	X	X	Reset
	H	L	X	X	Load Preset Data
	H	H	H	H	Count
	H	H	L	X	No Count
	H	H	X	L	No Count

\*HC163A only. HC161A is an Asynchronous-Reset Device  
H = high level  
L = low level  
X = don't care

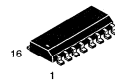
**MC54/74HC161A**  
**MC54/74HC163A**



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



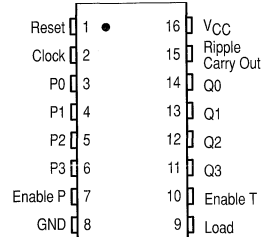
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

**ORDERING INFORMATION**

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXAD	SOIC

T<sub>A</sub> = -55°C to 125°C for all packages.

**PIN ASSIGNMENT**



Device	Count Mode	Reset Mode
HC161A	Binary	Asynchronous
HC163A	Binary	Synchronous

# MC54/74HC161A • MC54/74HC163A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltages (Referenced to GND)	- 0.5 to 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC}+1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC}+0.5$	V
$I_{in}$	DC Input Current, Per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, Per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	- 65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

Ceramic DIP: - 10 mW/°C from 100° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS				
Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	- 55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.9$ V 0 $V_{CC} = 4.5$ V 0 $V_{CC} = 6.0$ V	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND)							
Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to - 55°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out}  \leq 20$ $\mu$ A	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out}  \leq 20$ $\mu$ A	2.0	0.50	0.50	0.50	V
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu$ A	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 6.0$ mA $ I_{out}  \leq 7.8$ mA	4.5	3.98	3.84	3.7	V
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu$ A	2.0	0.10	0.10	0.10	V
			4.5	0.10	0.10	0.10	
			6.0	0.10	0.10	0.10	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 6.0$ mA $ I_{out}  \leq 7.8$ mA	4.5	0.26	0.33	0.40	V
6.0	0.26	0.33	0.40				
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.10$	$\pm 1.00$	$\pm 1.00$	$\mu$ A
$I_{CC}$	Maximum Quiescent Supply Current (Per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ $\mu$ A	6.0	4	40	160	$\mu$ A

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC161A • MC54/74HC163A

<b>AC ELECTRICAL CHARACTERISTICS</b> ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)							
Symbol	Parameter	Fig.	VCC V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
FMAX	Maximum Clock Frequency (50% Duty Cycle) *	1,7	2.0	6	5	4	MHz
			4.5	30	24	20	
			6.0	35	28	24	
t <sub>PLH</sub>	Maximum Propagation Delay Clock to Q	1,7	2.0	120	160	200	ns
			4.5	20	23	28	
			6.0	16	20	22	
t <sub>PHL</sub>	Maximum Propagation Delay Clock to Q	1,7	2.0	145	185	320	ns
			4.5	22	25	30	
			6.0	18	20	23	
t <sub>PHL</sub>	Maximum Propagation Delay Reset to Q (HC161A Only)	2,7	2.0	145	185	220	ns
			4.5	20	22	25	
			6.0	17	19	21	
t <sub>PLH</sub>	Maximum Propagation Delay Enable T to Ripple Carry Out	3,7	2.0	110	150	190	ns
			4.5	16	18	20	
			6.0	14	15	17	
t <sub>PHL</sub>	Maximum Propagation Delay Enable T to Ripple Carry Out	3,7	2.0	135	175	210	ns
			4.5	18	20	22	
			6.0	15	16	20	
t <sub>PLH</sub>	Maximum Propagation Delay Clock to Ripple Carry Out	1,7	2.0	120	160	200	ns
			4.5	22	27	30	
			6.0	18	22	25	
t <sub>PHL</sub>	Maximum Propagation Delay Clock to Ripple Carry Out	1,7	2.0	145	185	220	ns
			4.5	22	28	35	
			6.0	20	24	28	
t <sub>PHL</sub>	Maximum Propagation Delay Reset to Ripple Carry Out (HC161A Only)	2,7	2.0	155	190	230	ns
			4.5	22	26	30	
			6.0	18	22	25	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output	2,7	2.0	75	95	110	ns
			4.5	15	19	22	
			6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	1,7	—	10	10	10	pF
C <sub>pd</sub>	Power Dissipation Capacitance (Per Gate). Used to determine no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	<b>Typical @ 25°C. V<sub>CC</sub> = 5.0 V</b>				30	pF
		30					

\* Applies to noncascaded/nonsynchronous clocked configurations only. With synchronously cascaded counters, (1) Clock to Ripple Carry Out propagation delays, (2) Enable T or Enable P to Clock setup times, and (3) Clock to Enable T or Enable P hold times determine  $f_{max}$ . However, if Ripple Carry Out of each stage is tied to the Clock of the next stage (nonsynchronously clocked), the  $f_{max}$  in the table above is applicable. See Applications information in this data sheet.

## MC54/74HC161A • MC54/74HC163A

TIMING REQUIREMENTS ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)							
Symbol	Parameter	Fig.	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
$t_{SU}$	Minimum Setup Time, Preset Data Inputs to Clock	5	2.0	40	60	80	ns
			4.5	15	20	30	
			6.0	12	18	20	
$t_{SU}$	Minimum Setup Time, Load to Clock	5	2.0	60	75	90	ns
			4.5	15	20	30	
			6.0	12	18	20	
$t_{SU}$	Minimum Setup Time, Reset to Clock (HC163A Only)	4	2.0	60	75	90	ns
			4.5	20	25	35	
			6.0	17	23	25	
$t_{SU}$	Minimum Setup Time, Enable T or Enable P to Clock	6	2.0	80	95	110	ns
			4.5	20	25	35	
			6.0	17	23	25	
$t_H$	Minimum Hold Time, Clock to Load or Preset Data Inputs	5	2.0	3	3	3	ns
			4.5	3	3	3	
			6.0	3	3	3	
$t_H$	Minimum Hold Time, Clock to Reset (HC163A Only)	4	2.0	3	3	3	ns
			4.5	3	3	3	
			6.0	3	3	3	
$t_H$	Minimum Hold Time, Clock to Enable T or Enable P	6	2.0	3	3	3	ns
			4.5	3	3	3	
			6.0	3	3	3	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (HC161A Only)	2	2.0	80	95	110	ns
			4.5	15	20	26	
			6.0	12	17	23	
$t_{rec}$	Minimum Recovery Time Load Inactive to Clock	5	2.0	80	95	110	ns
			4.5	15	20	26	
			6.0	12	17	23	
$t_w$	Minimum Pulse Width, Clock	1	2.0	60	75	90	ns
			4.5	12	15	18	
			6.0	10	13	15	
$t_w$	Minimum Pulse Width, Reset	2	2.0	60	75	90	ns
			4.5	12	15	18	
			6.0	10	13	15	
$t_r, t_f$	Maximum Input Rise and Fall Times		2.0	1000	1000	1000	ns
			4.5	500	500	500	
			6.0	400	400	400	

5



# MC54/74HC161A • MC54/74HC163A

## FUNCTION DESCRIPTION

The HC161A/163A are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading and count-enable controls.

The HC161A and HC163A are binary counters with asynchronous Reset and synchronous Reset, respectively.

### INPUTS

#### Clock (Pin 2)

The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting and loading occur with the rising edge of the Clock input.

#### Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (Pin 3) is the least-significant bit and P3 (Pin 6) is the most-significant bit.

### OUTPUTS

#### Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs. Q0 (Pin 14) is the least-significant bit and Q3 (Pin 11) is the most-significant bit.

#### Ripple Carry Out (Pin 15)

When the counter is in its maximum state 1111, this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

$$\text{Ripple Carry Out} = \text{Enable T} \cdot \text{Q0} \cdot \text{Q1} \cdot \text{Q2} \cdot \text{Q3}$$

### CONTROL FUNCTIONS

#### Resetting

A low level on the Reset pin (Pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to a low level. The HC161A resets asynchronously, and the HC163A resets with the rising edge of the Clock input (synchronous reset).

#### Loading

With the rising edge of the Clock, a low level on Load (Pin 9) loads the data from the Preset Data input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

#### Count Enable/Disable

These devices have two count-enable control pins: Enable P (Pin 7) and Enable T (Pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \cdot \text{Enable T} \cdot \text{Load}$$

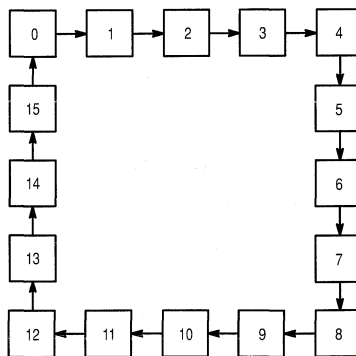
The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control: Enable T is both a count-enable and a Ripple-Carry Output control.

Table 1. Count Enable/Disable

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0-Q3	Ripple Carry Out
H	H	H	Count	High when Q0-Q3 are maximum*
L	H	H	No Count	High when Q0-Q3 are maximum*
X	L	H	No Count	High when Q0-Q3 are maximum*
X	X	L	No Count	L

\*Q0 through Q3 are maximum when Q3 Q2 Q1 Q0 = 1111.

### OUTPUT STATE DIAGRAM



Binary Counters

SWITCHING WAVEFORMS

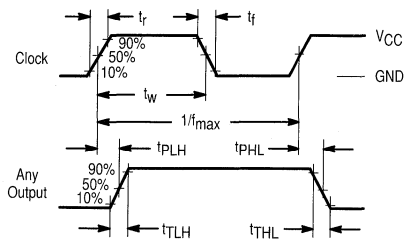


Figure 1.

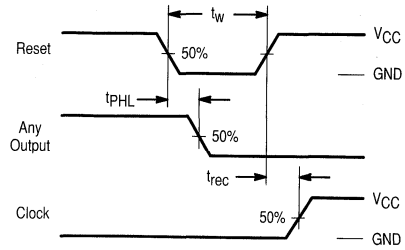


Figure 2.

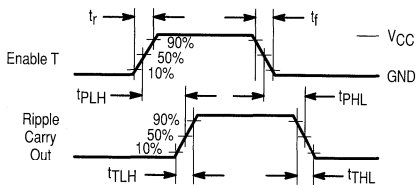


Figure 3.

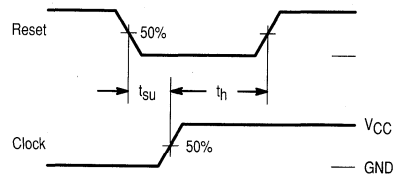


Figure 4. HC163A Only

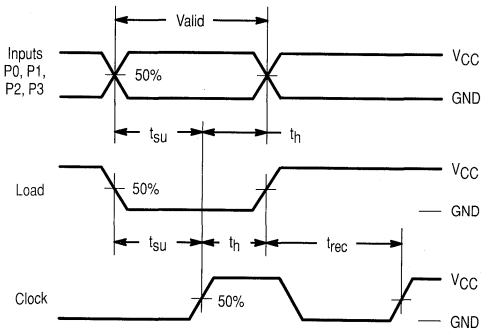


Figure 5.

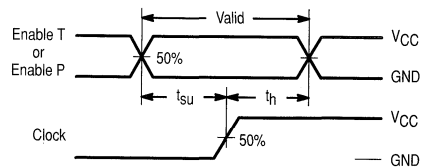
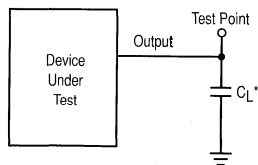


Figure 6.

5

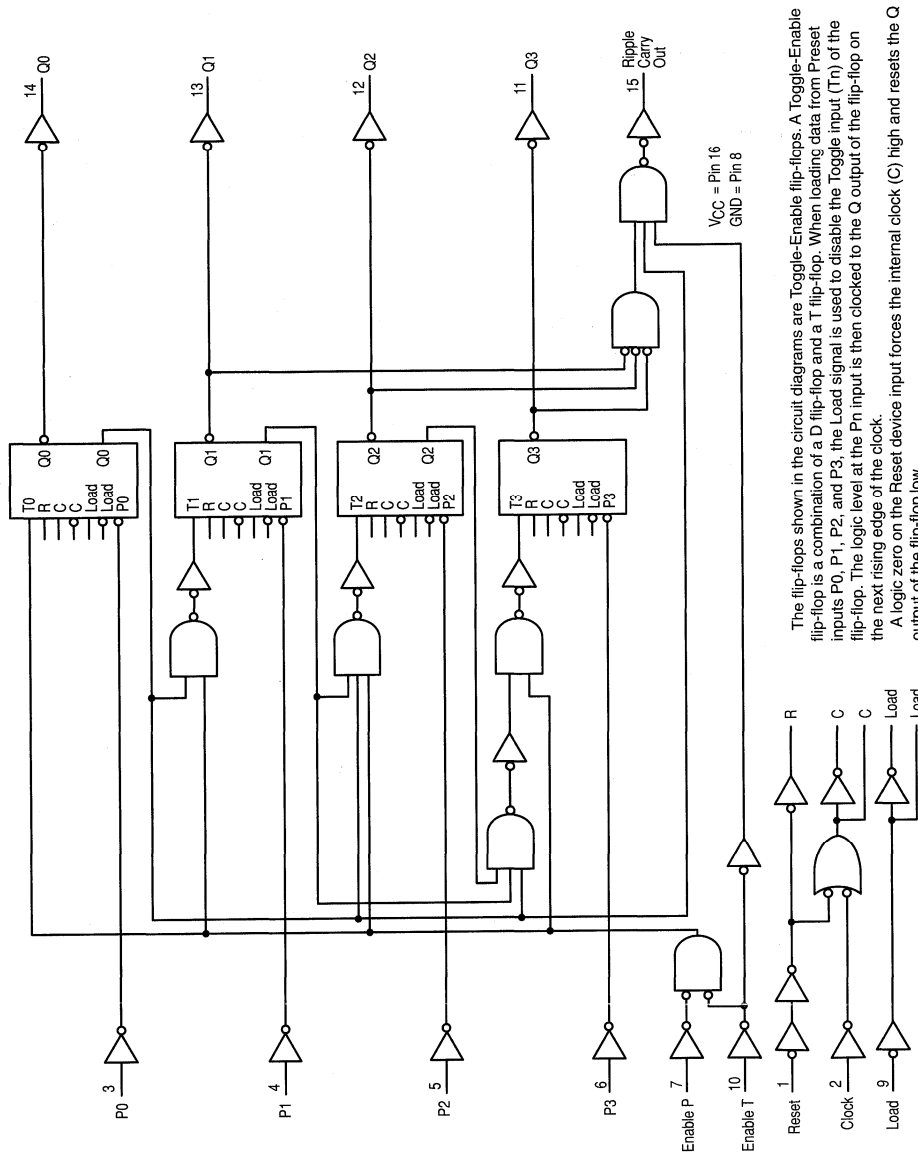
TEST CIRCUIT



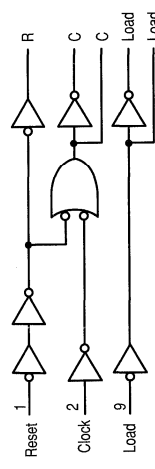
\*Includes all probe and jig capacitance.

Figure 7.

Figure 8. 4-Bit Binary Counter with Asynchronous Reset (MC54/74HC161A)



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.  
 A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

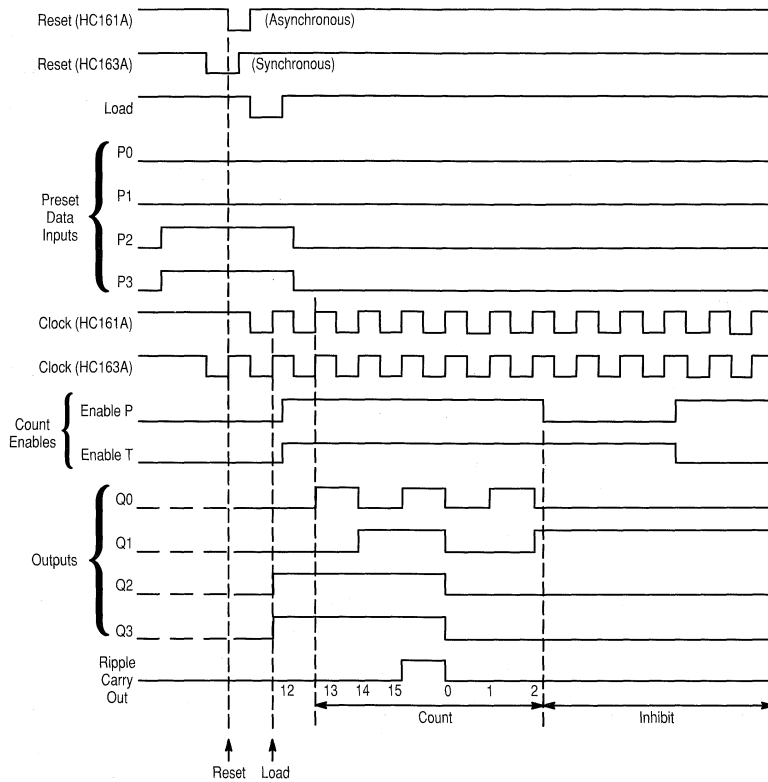


# MC54/74HC161A • MC54/74HC163A

Figure 9. Timing Diagram

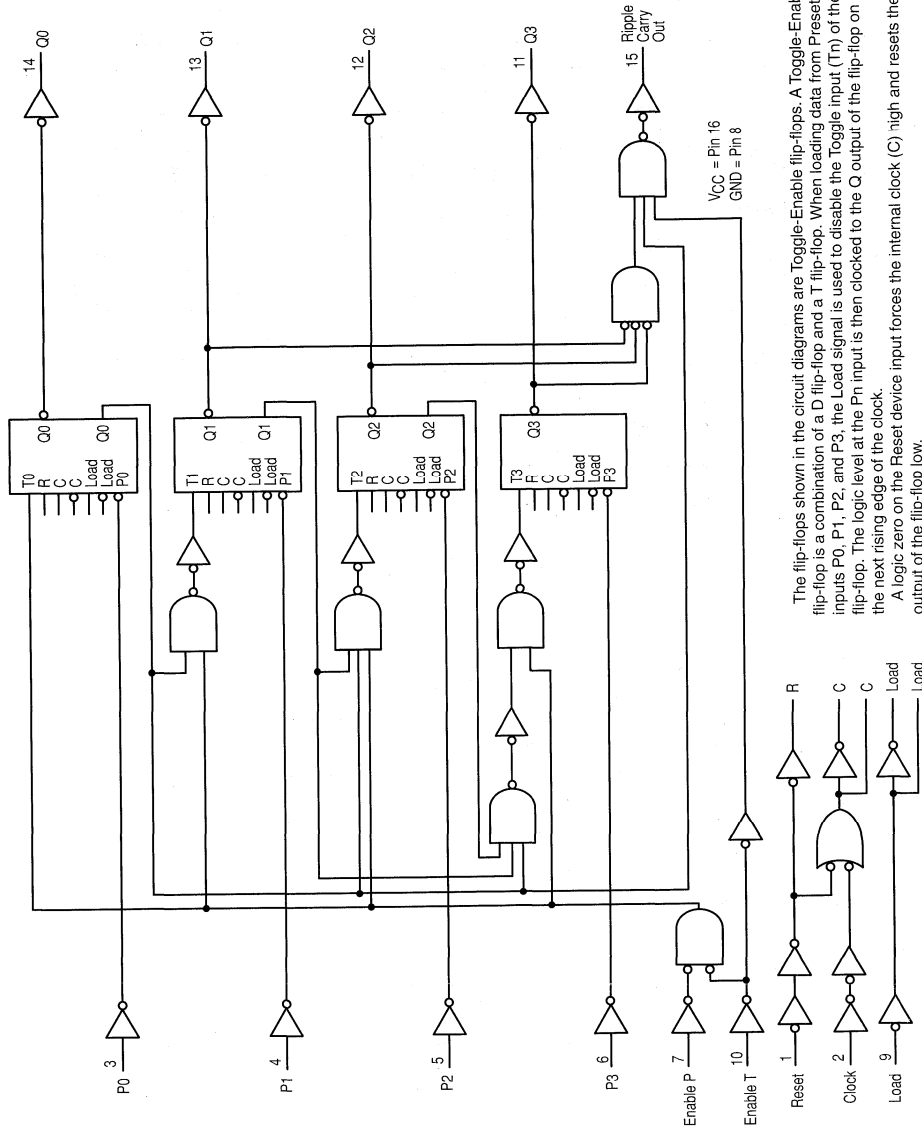
Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



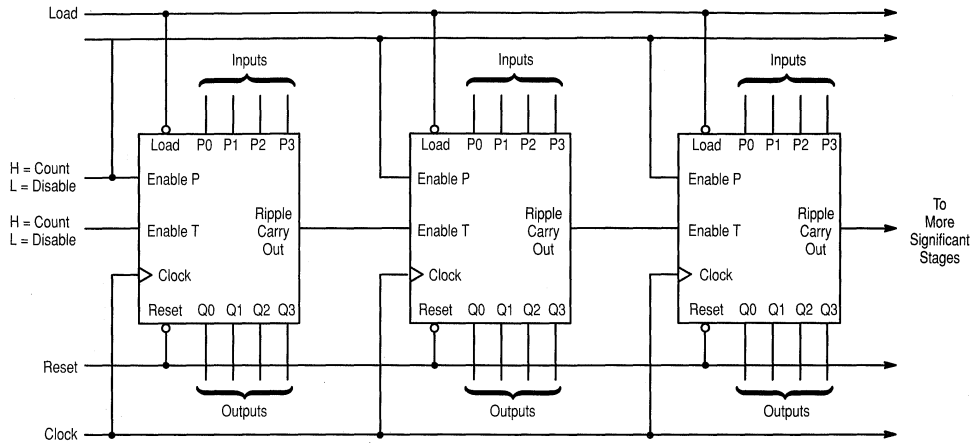
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Figure 10. 4-Bit Binary Counter with Synchronous Reset  
(MC54/74HC163A)



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tr) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.  
A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

TYPICAL APPLICATIONS CASCADING



NOTE: When used in these cascaded configurations the clock  $f_{max}$  guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and clock.

Figure 11. N-Bit Synchronous Counters

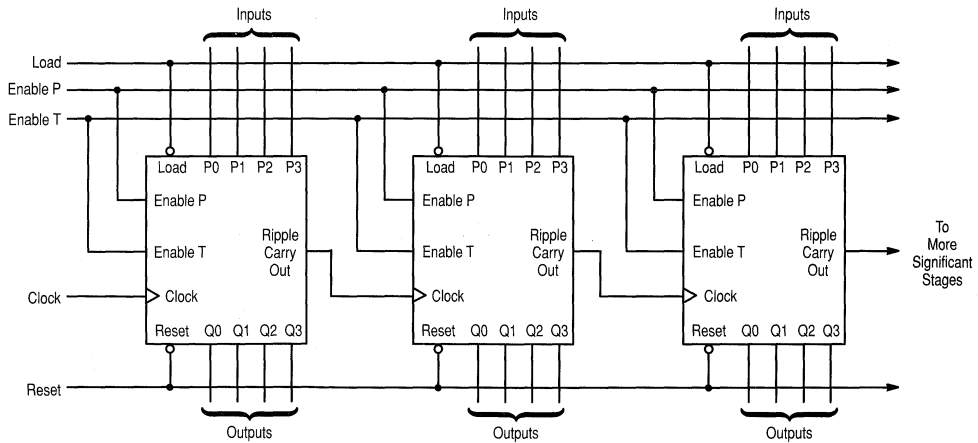


Figure 12. Nibble Ripple Counter

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# MC54/74HC161A • MC54/74HC163A

## TYPICAL APPLICATIONS VARYING THE MODULUS

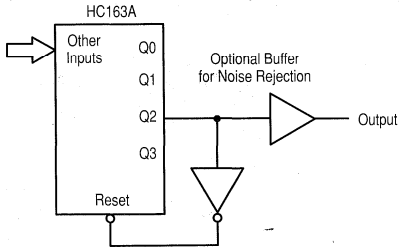


Figure 13. Modulo-5 Counter

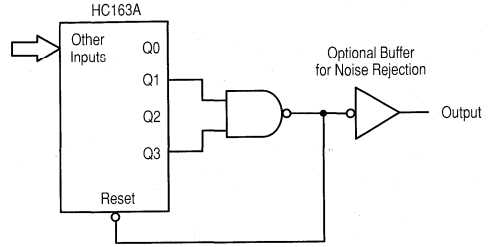


Figure 14. Modulo-11 Counter

The HC163A facilitates designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous Reset.

# 8-Bit Serial-Input/Parallel-Output Shift Register

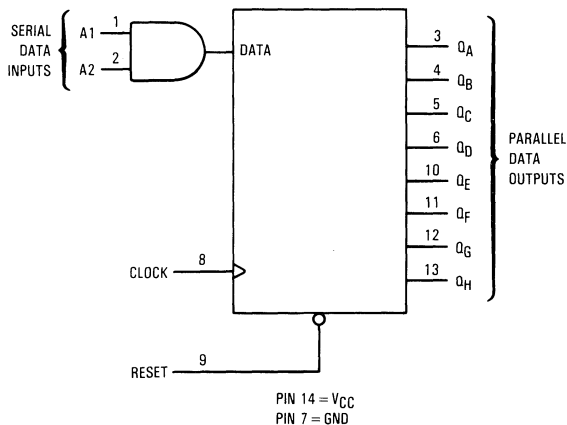
## High-Performance Silicon-Gate CMOS

The MC54/74HC164 is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

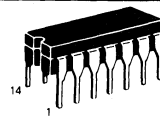
The MC54/74HC164 is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates

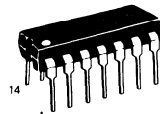
LOGIC DIAGRAM



## MC54/74HC164



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



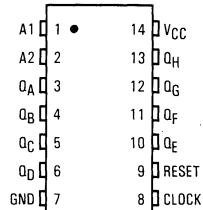
D SUFFIX  
 SOIC  
 CASE 751A-02

### ORDERING INFORMATION

MC74HCXXXD	SOIC
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Outputs		
Reset	Clock	A1 A2	Q <sub>A</sub> Q <sub>B</sub> . . . Q <sub>H</sub>	
L	X	X X	L . . . L	
H		X X	no change	
H		H D	D Q <sub>A</sub> n . . . Q <sub>G</sub> n	
H		D H	D Q <sub>A</sub> n . . . Q <sub>G</sub> n	

D = data input  
 Q<sub>A</sub>n - Q<sub>G</sub>n = data shifted from the previous stage on a rising edge at the clock input.

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# MC54/74HC164

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out}  \leq 20$ $\mu$ A	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out}  \leq 20$ $\mu$ A	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu$ A	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0$ mA $ I_{out}  \leq 5.2$ mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu$ A	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0$ mA $ I_{out}  \leq 5.2$ mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu$ A
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ $\mu$ A	6.0	8	80	160	$\mu$ A

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC164

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
$t_{PHL}$	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	205	255	310	ns
		4.5	41	51	62	
		6.0	35	43	53	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

$C_{PD}$	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, VCC = 5.0 V	pF
		140	

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
$t_{su}$	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_h$	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_w$	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_r$ , $t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC164

## PIN DESCRIPTIONS

### INPUTS

**A1, A2 (PINS 1, 2)** — Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data-enable input. When only one serial input is used, the other must be connected to  $V_{CC}$ .

**CLOCK (PIN 8)** — Shift Register Clock. A positive-going transition on this pin shifts the data at each stage to the next stage. The shift register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

### OUTPUTS

**$Q_A - Q_H$  (PINS 3, 4, 5, 6, 10, 11, 12, 13)** — Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

### CONTROL INPUT

**RESET (PIN 9)** — Active-Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip-flops and sets outputs  $Q_A - Q_H$  to the low level state.

## SWITCHING WAVEFORMS

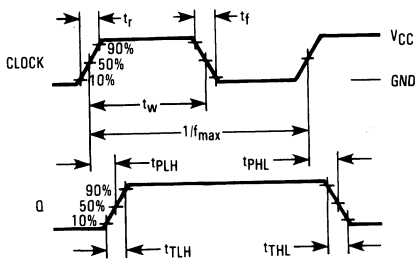


Figure 1

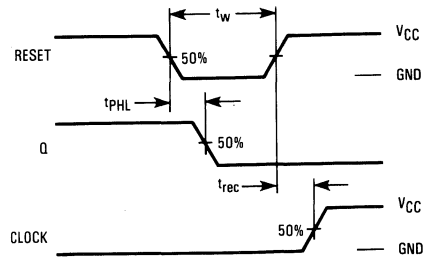


Figure 2

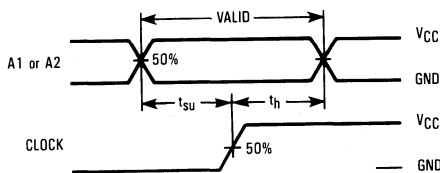
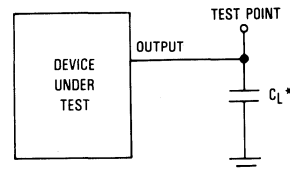


Figure 3

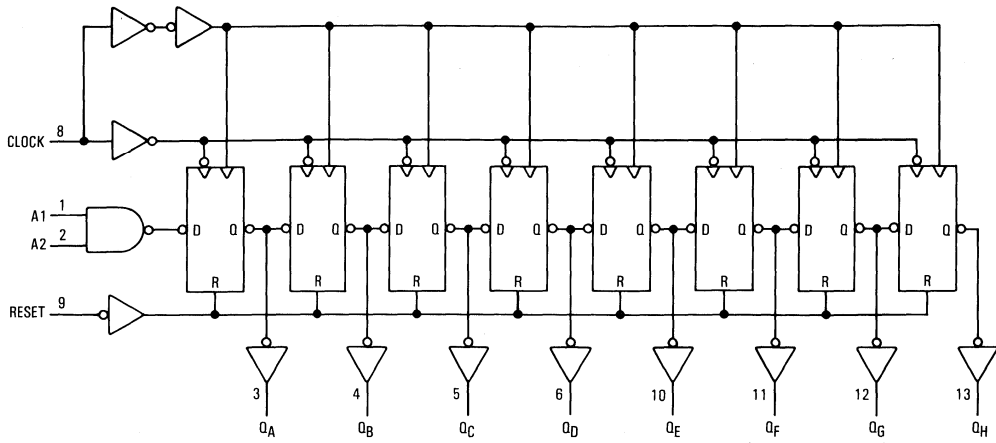


\*Includes all probe and jig capacitance.

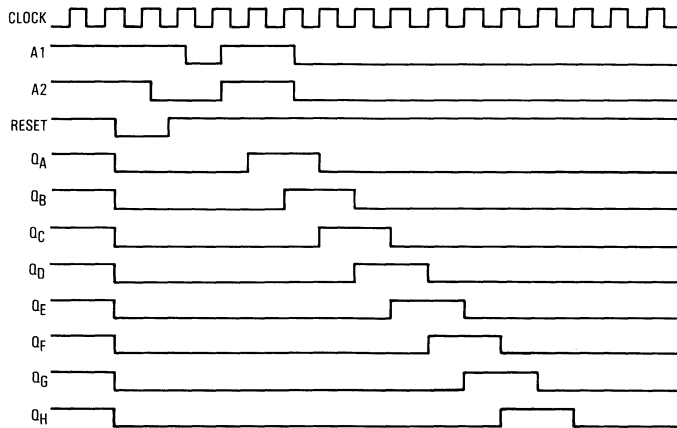
Figure 4. Test Circuit

# MC54/74HC164

## EXPANDED LOGIC DIAGRAM



## TIMING DIAGRAM



5

# 8-Bit Serial or Parallel-Input/ Serial-Output Shift Register High-Performance Silicon-Gate CMOS

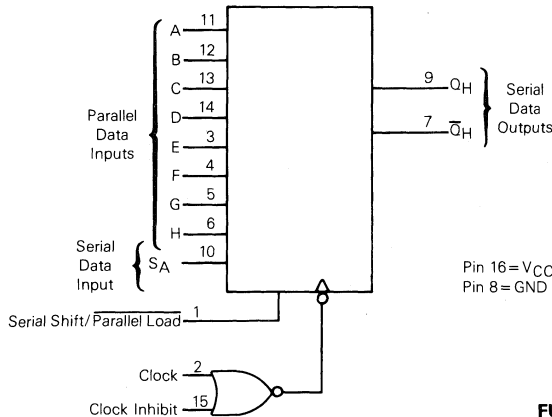
The MC54/74HC165 is identical in pinout to the LS165. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is an 8-bit shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Serial Shift/Parallel Load input is low, the data is loaded asynchronously in parallel. When the Serial Shift/Parallel Load input is high, the data is loaded serially on the rising edge of either Clock or Clock Inhibit (see the Function Table).

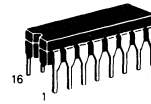
The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates

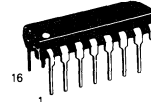
### LOGIC DIAGRAM



## MC54/74HC165



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**



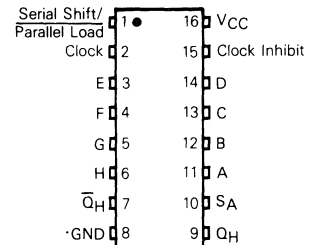
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXD SOIC  
 MC74HCXXN Plastic  
 MC54HCXXJ Ceramic

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Serial Shift/ Parallel Load	Inputs				Internal Stages QA QB	Output QH	Operation
	Clock	Clock Inhibit	SA	A-H			
L	X	X	X	a...h	a b	h	Asynchronous Parallel Load
H		L	L	X	L QA H QAn	QH QGn	Serial Shift via Clock
H	L		L	X	L QA H QAn	QH QGn	Serial Shift via Clock Inhibit
H	X	X	X	X	no change		Inhibited Clock
H	H	X	X	X	no change		No Clock
H	L	L	X	X	no change		No Clock

X = don't care  
 QAn-QGn = Data shifted from the preceding stage

# MC54/74HC165

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP or SOIC Package)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	5.9	5.9	5.9	
			6.0	3.98	3.84	3.70	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC165

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 8)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock (or Clock Inhibit) to Q <sub>H</sub> or $\bar{Q}_H$ (Figures 1 and 8)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Serial Shift/Parallel Load to Q <sub>H</sub> or $\bar{Q}_H$ (Figures 2 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input H to Q <sub>H</sub> or $\bar{Q}_H$ (Figures 3 and 8)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		85	

# MC54/74HC165

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
$t_{su}$	Minimum Setup Time, Parallel Data Inputs to Serial Shift/Parallel Load (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_{su}$	Minimum Setup Time, Input $S_A$ to Clock (or Clock Inhibit) (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_{su}$	Minimum Setup Time, Serial Shift/Parallel Load to Clock (or Clock Inhibit) (Figure 6)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_{su}$	Minimum Setup Time, Clock to Clock Inhibit (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_h$	Minimum Hold Time, Serial Shift/Parallel Load to Parallel Data Inputs (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_h$	Minimum Hold Time, Clock (or Clock Inhibit) to Input $S_A$ (Figure 5)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_h$	Minimum Hold Time, Clock (or Clock Inhibit) to Serial Shift/Parallel Load (Figure 6)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_{rec}$	Minimum Recovery Time, Clock to Clock Inhibit (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_w$	Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

5

## PIN DESCRIPTIONS

### INPUTS

**A, B, C, D, E, F, G, H (PINS 11, 12, 13, 14, 3, 4, 5, 6)** — Parallel Data inputs. Data on these inputs are asynchronously entered in parallel into the internal flip-flops when the Serial Shift/Parallel Load input is low.

**$S_A$  (PIN 10)** — Serial Data input. When the Serial Shift/Parallel Load input is high, data on this pin is serially entered into the first stage of the shift register with the rising edge of the Clock.

### CONTROL INPUTS

**SERIAL SHIFT/PARALLEL LOAD (PIN 1)** — Data-entry control input. When a high level is applied to this pin, data at the Serial Data input ( $S_A$ ) are shifted into the register with the rising edge of the Clock. When a low level is applied to

this pin, data at the Parallel Data inputs are asynchronously loaded into each of the eight internal stages.

**CLOCK, CLOCK INHIBIT (PINS 2, 15)** — Clock inputs. These two clock inputs function identically. Either may be used as an active-high clock inhibit. However, to avoid double clocking, the inhibit input should go high only while the clock input is high.

The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

### OUTPUTS

**$Q_H, \bar{Q}_H$  (PINS 9, 7)** — Complementary Shift Register outputs. These pins are the noninverted and inverted outputs of the eighth stage of the shift register.



# MC54/74HC165

## SWITCHING WAVEFORMS

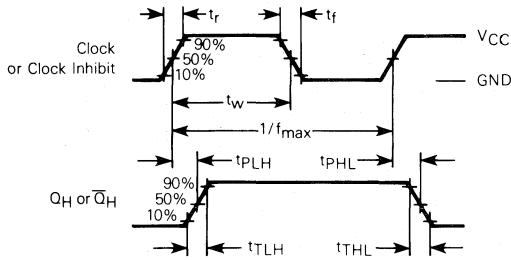


Figure 1. Serial-Shift Mode

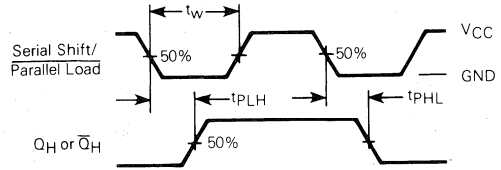


Figure 2. Parallel-Load Mode

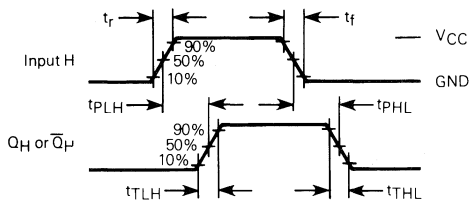


Figure 3. Parallel-Load Mode

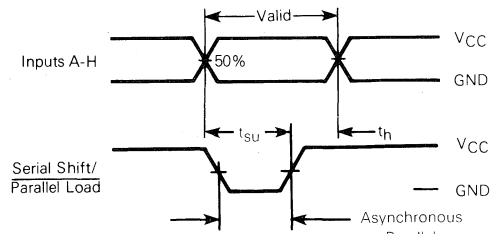


Figure 4. Parallel-Load Mode (level sensitive)

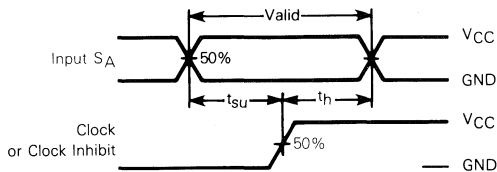


Figure 5. Serial-Shift Mode

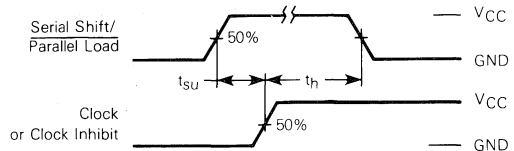


Figure 6. Serial-Shift Mode

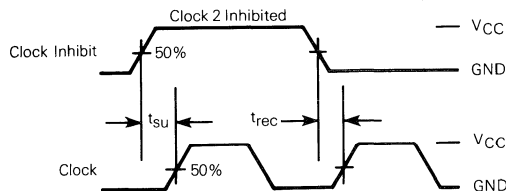
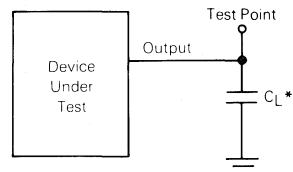


Figure 7. Serial-Shift, Clock-Inhibit Mode

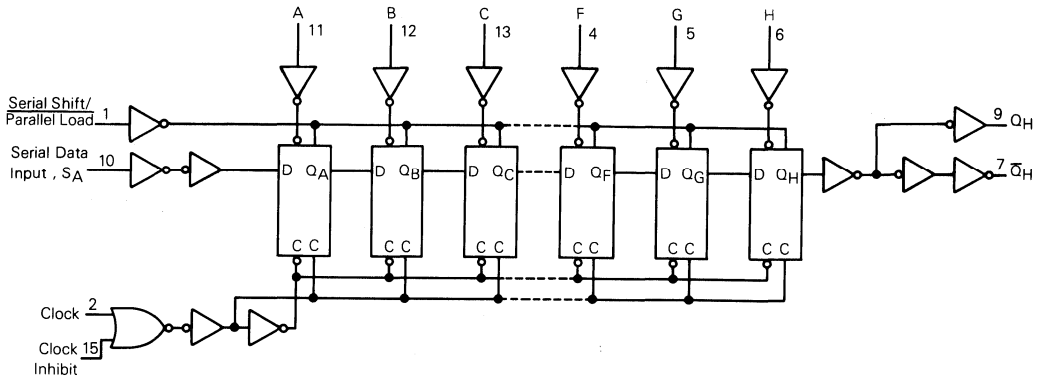


\* Includes all probe and jig capacitance.

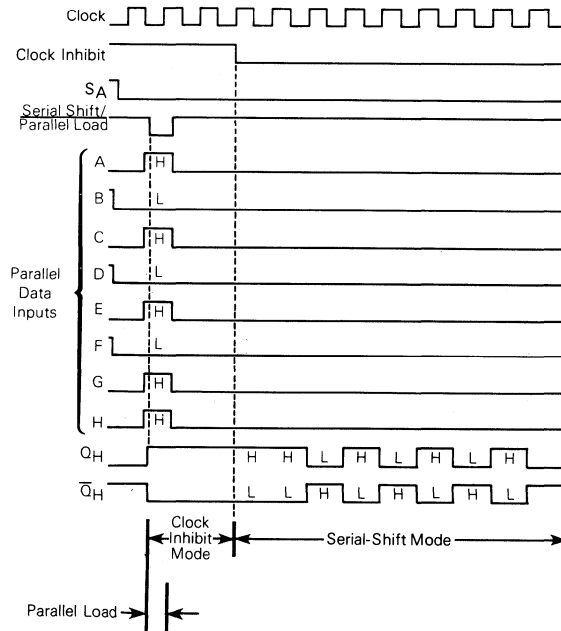
Figure 8. Test Circuit

# MC54/74HC165

## EXPANDED LOGIC DIAGRAM



## TIMING DIAGRAM



5

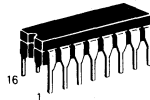
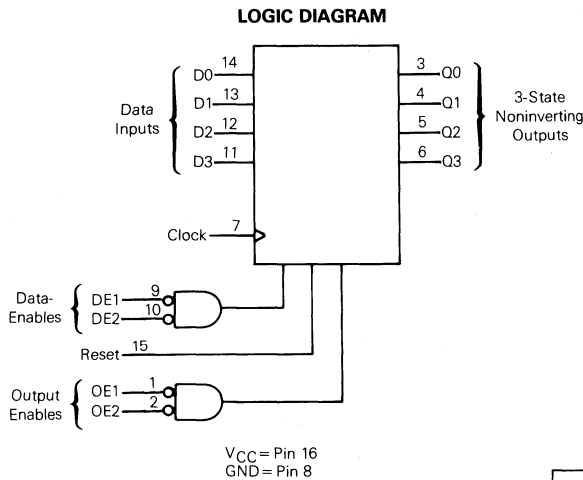
**MC54/74HC173**

**Quad 3-State D Flip-Flop with  
 Common Clock and Reset  
 High-Performance Silicon-Gate CMOS**

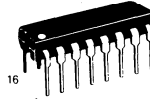
The MC54/74HC173 is identical in pinout to the LS173. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data, when enabled, are clocked into the four D flip-flops with the rising edge of the common Clock. When either or both of the Output Enable Controls is high, the outputs are in a high-impedance state. This feature allows the HC173 to be used in bus-oriented systems. The Reset feature is asynchronous and active-high.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 208 FETs or 52 Equivalent Gates



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



**N SUFFIX  
 PLASTIC  
 CASE 648-06**



**D SUFFIX  
 SOIC  
 CASE 751B-04**

**ORDERING INFORMATION**

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

**PIN ASSIGNMENT**

OE1	1	16	V <sub>CC</sub>
OE2	2	15	Reset
Q0	3	14	D0
Q1	4	13	D1
Q2	5	12	D2
Q3	6	11	D3
Clock	7	10	DE2
GND	8	9	DE1

**5**

**FUNCTION TABLE**

Output Enables		Inputs					Output
OE1	OE2	Reset	Clock	Data Enables		Data D	Q
OE1	OE2	Reset	Clock	DE1	DE2	D	Q
L	L	H	X	X	X	X	L
L	L	L	L	X	X	X	no change
L	L	L	H	X	X	X	no change
L	L	L	↗	H	X	X	no change
L	L	L	↘	X	H	X	no change
L	L	L	↗	L	L	L	L
L	L	L	↘	L	L	H	H
L	L	L	↔	X	X	X	no change
L	H	X	X	X	X	X	high impedance
H	L	X	X	X	X	X	high impedance
H	H	X	X	X	X	X	high impedance

# MC54/74HC173

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
PD	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC173

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Input D or DE to Clock (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Clock to Input D or DE (Figure 4)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	90	115	135	ns
		4.5	18	23	27	
		6.0	15	20	23	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC173

## PIN DESCRIPTIONS

### INPUTS

**D0, D1, D2, D3 (PINS 14, 13, 12, 11)** — 4-bit data inputs. Data on these pins, when enabled by the Data-Enable Controls, are entered into the flip-flops on the rising edge of the clock.

**CLOCK (PIN 7)** — Clock input.

### OUTPUTS

**Q0, Q1, Q2, Q3 (PINS 3, 4, 5, 6)** — 3-state register outputs. During normal operation of the device, the outputs of the D flip-flops appear at these pins. During 3-state operation, these outputs assume a high-impedance state.

### CONTROL INPUTS

**RESET (PIN 15)** — Asynchronous reset input. A high level

on this pin resets all flip-flops and forces the Q outputs low, if they are not already in high-impedance state.

**DE1, DE2 (Pins 9, 10)** — Active-low Data Enable Control inputs. When both Data Enable Controls are low, data at the D inputs are loaded into the flip-flops with the rising edge of the Clock input. When either or both of these controls are high, there is no change in the state of the flip-flops, regardless of any changes at the D or Clock inputs.

**OE1, OE2 (Pins 1, 2)** — Output Enable Control inputs. When either or both of the Output Enable Controls are high, the Q outputs of the device are in the high-impedance state. When both controls are low, the device outputs display the data in the flip-flops.

## SWITCHING WAVEFORMS

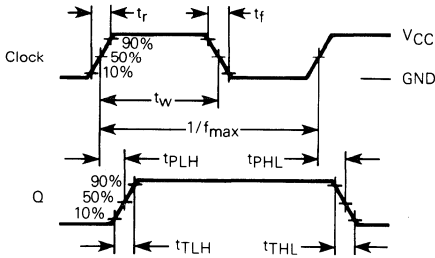


Figure 1.

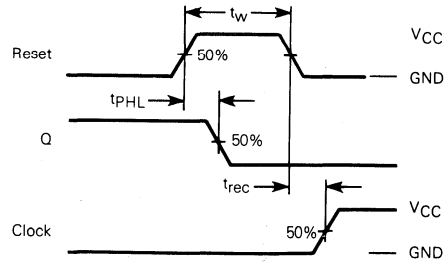


Figure 2.

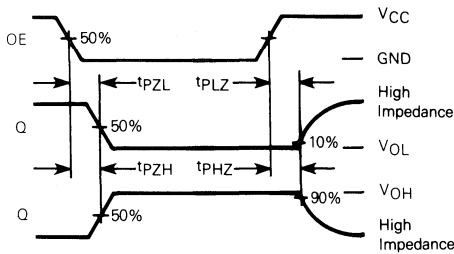


Figure 3.

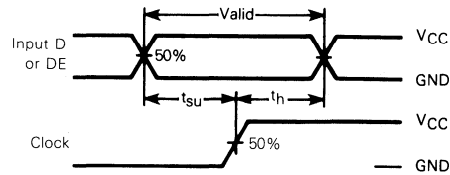
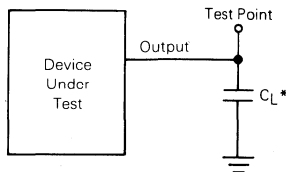


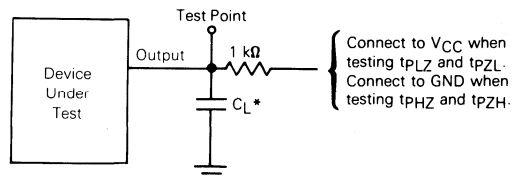
Figure 4.

## TEST CIRCUITS



\* Includes all probe and jig capacitance.

Figure 5.

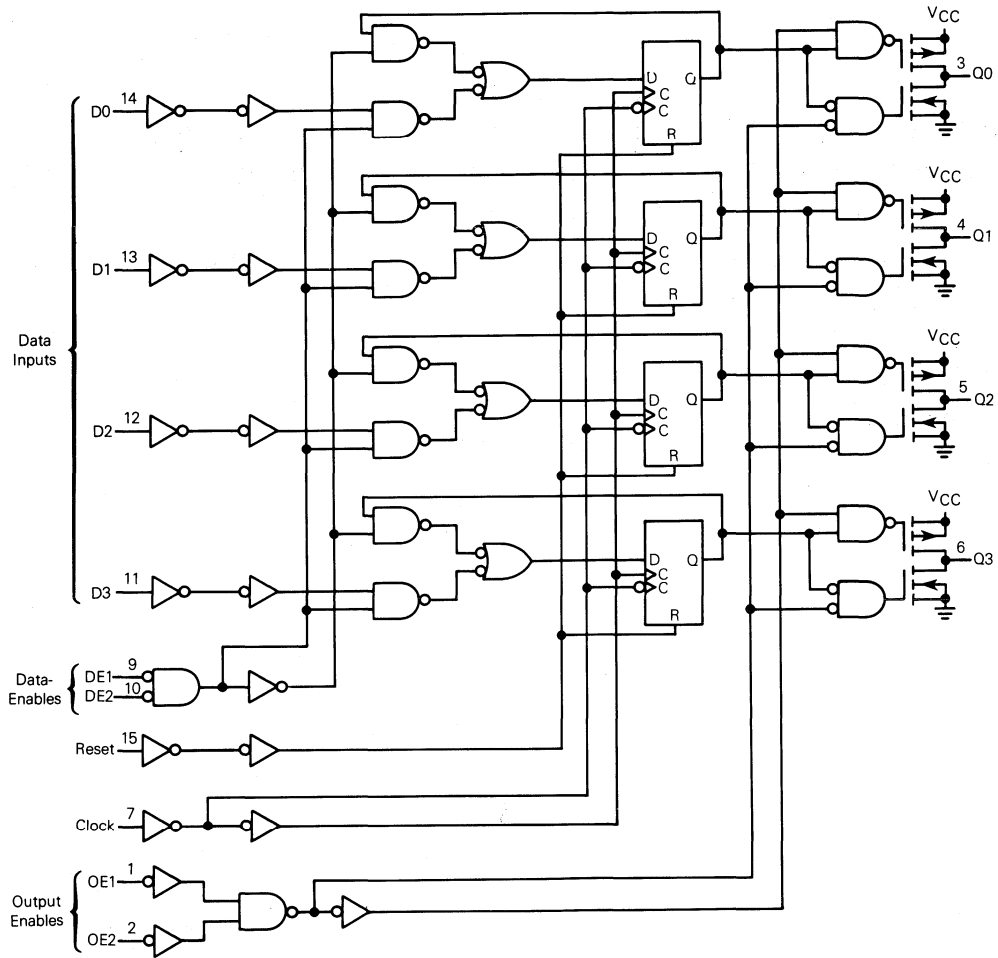


\* Includes all probe and jig capacitance.

Figure 6.

# MC54/74HC173

## LOGIC DETAIL



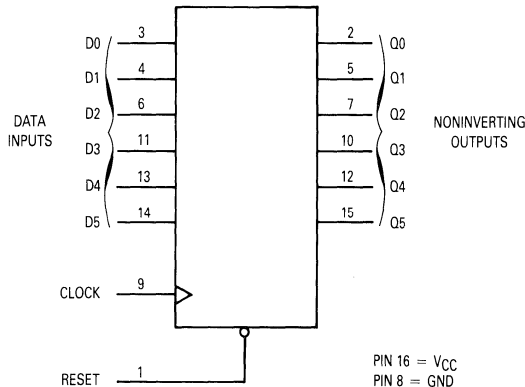
## Hex D Flip-Flop with Common Clock and Reset High-Performance Silicon-Gate CMOS

The MC54/74HC174A is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 162 FETs or 40.5 Equivalent Gates

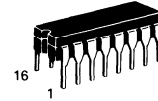
LOGIC DIAGRAM



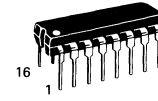
Design Criteria	Value	Units
Internal Gate Count*	40.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	.0075	pJ

\*Equivalent to a two-input NAND gate.

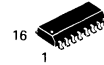
### MC54/74HC174A



J SUFFIX  
 CERAMIC  
 CASE 620-09



N SUFFIX  
 PLASTIC  
 CASE 648-08

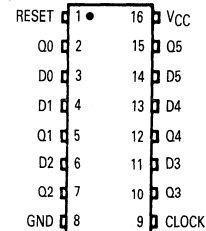


D SUFFIX  
 SOIC  
 CASE 751B-04

#### ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXAD	SOIC

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change



# MC54/74HC174A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1.0 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	V	
		6.0	5.48	5.34	5.2		
		4.5	0.26	0.33	0.4		
6.0	0.26	0.33	0.4				
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4.0	40	160	μA

NOTES: 1. Information on typical parametric values along with high frequency or heavy load considerations, can be found in Chapter 4.  
 2. Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

# MC54/74HC174A

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>PLH</sub> t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	110	140	160	ns
		4.5	21	28	32	
		6.0	19	24	27	
t <sub>TLH</sub> t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance		10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF	
		62				

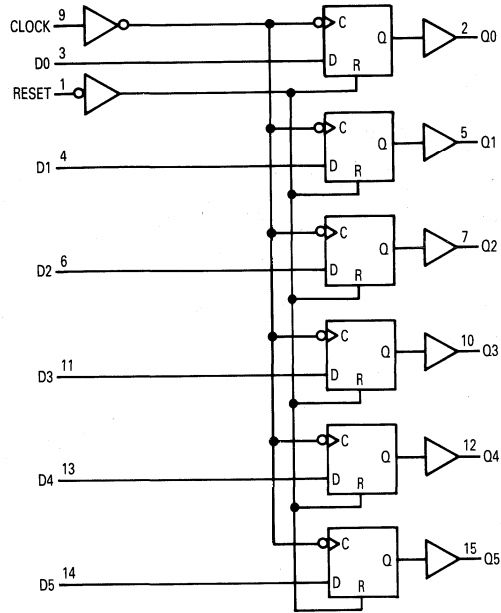
## TIMING REQUIREMENTS ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	Fig.	VCC V	Guaranteed Limit						Units
				25°C to -55°C		≤85°C		≤125°C		
				Min	Max	Min	Max	Min	Max	
t <sub>su</sub>	Minimum Setup Time, Data to Clock	3	2.0	50		65		75		ns
			4.5	10		13		15		
			6.0	9.0		11		13		
t <sub>h</sub>	Minimum Hold Time, Clock to Data	3	2.0	5.0		5.0		5.0		ns
			4.5	5.0		5.0		5.0		
			6.0	5.0		5.0		5.0		
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock	2	2.0	5.0		5.0		5.0		ns
			4.5	5.0		5.0		5.0		
			6.0	5.0		5.0		5.0		
t <sub>w</sub>	Minimum Pulse Width, Clock	1	2.0	75		95		110		ns
			4.5	15		19		22		
			6.0	13		16		19		
t <sub>w</sub>	Minimum Pulse Width, Reset	2	2.0	75		95		110		ns
			4.5	15		19		22		
			6.0	13		16		19		
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1	2.0		1000		1000		1000	ns
			4.5		500		500		500	
			6.0		400		400		400	

5

# MC54/74HC174A

## EXPANDED LOGIC DIAGRAM



## SWITCHING WAVEFORMS

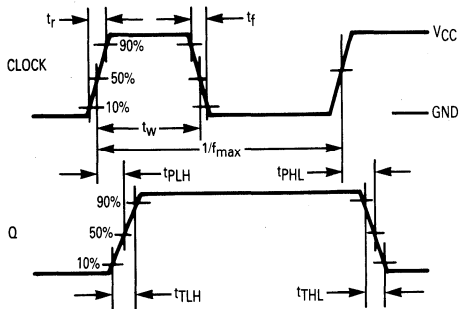


Figure 1.

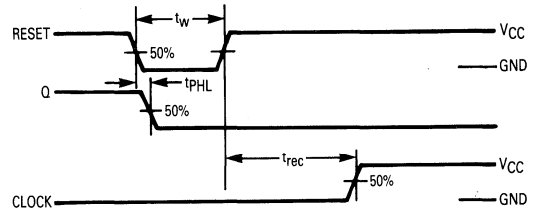


Figure 2.

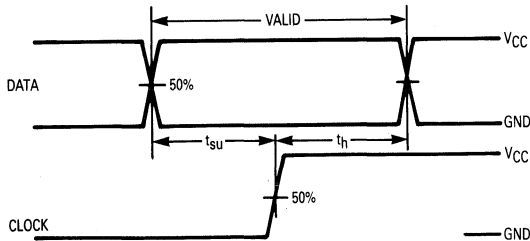
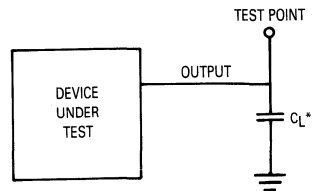


Figure 3.



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

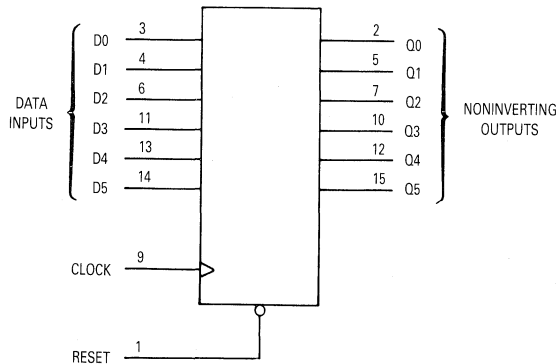
## Hex D Flip-Flop with Common Clock and Reset with LSTTL Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT174A is identical in pinout to the LS174. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 178 FETs or 44.5 Equivalent Gates

### LOGIC DIAGRAM

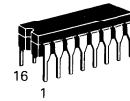


PIN 16 = V<sub>CC</sub>  
 PIN 8 = GND

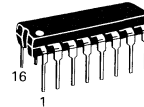
Design Criteria	Value	Unit
Internal Gate Count*	44.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	0.005	$\mu$ W
Speed Power Product	0.0075	pJ

\*Equivalent to a two-input NAND gate.

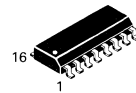
## MC54/74HCT174A



J SUFFIX  
 CERAMIC  
 CASE 620-08



N SUFFIX  
 PLASTIC  
 CASE 648-08

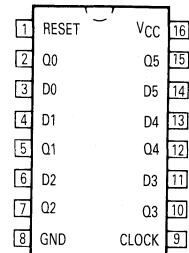


D SUFFIX  
 SOIC  
 CASE 751B-04

### ORDERING INFORMATION

MC74HCTXXXAN	Plastic
MC54HCTXXXAJ	Ceramic
MC74HCTXXXAD	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change

# MC54/74HCT174A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4.0	40	160	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HCT174A

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
f <sub>MAX</sub>	Maximum Clock Frequency (50% Duty Cycle)	30	24	20	MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	24	30	36	ns
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	23	28	35	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
C <sub>in</sub>	Maximum Input Capacitance	10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$			pF
		79			

## TIMING REQUIREMENTS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			25°C to -55°C		≤85°C		≤125°C		
			Min	Max	Min	Max	Min	Max	
t <sub>SU</sub>	Minimum Setup Time, Data to Clock	3	10		13		15		ns
t <sub>H</sub>	Minimum Hold Time, Clock to Data	3	5.0		6.0		8.0		ns
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock	2	5.0		6.0		8.0		ns
t <sub>W</sub>	Minimum Pulse Width, Clock	1	15		19		22		ns
t <sub>W</sub>	Minimum Pulse Width, Reset	2	15		19		22		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1		500		500		500	ns

# MC54/74HCT174A

## SWITCHING WAVEFORMS

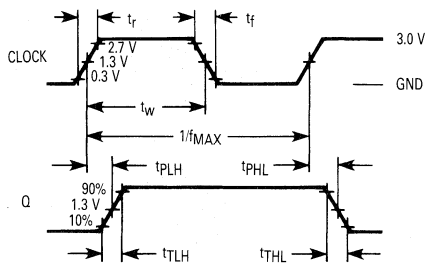


Figure 1.

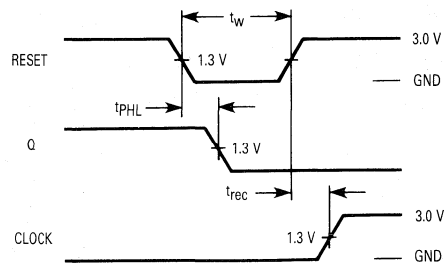


Figure 2.

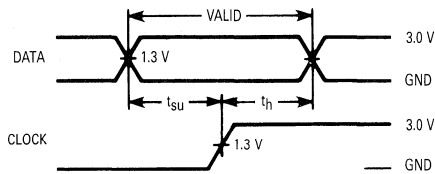
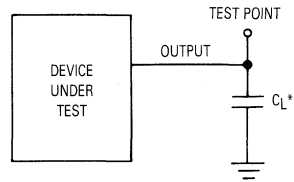


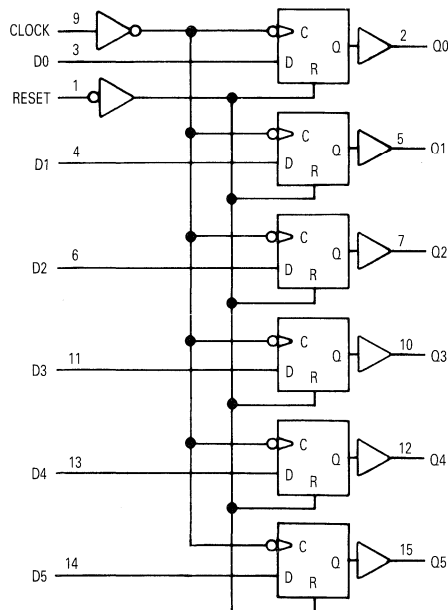
Figure 3.



\*Includes all probe and jig capacitance

Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM



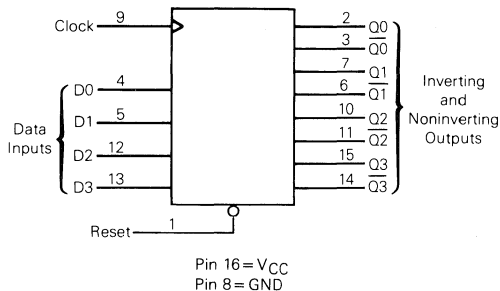
## Quad D Flip-Flop with Common Clock and Reset High-Performance Silicon-Gate CMOS

The MC54/74HC175 is identical in pinout to the LS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

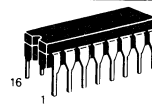
This device consists of four D flip-flops with common Reset and Clock inputs, and separate D inputs. Reset (active-low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive-going edge of the Clock input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 166 FETs or 41.5 Equivalent Gates

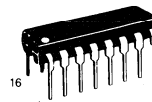
**LOGIC DIAGRAM**



## MC54/74HC175



**J SUFFIX  
CERAMIC  
CASE 620-09**



**N SUFFIX  
PLASTIC  
CASE 648-08**



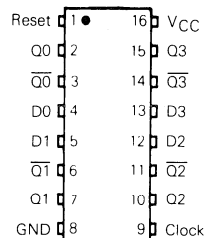
**D SUFFIX  
SOIC  
CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Outputs	
Reset	Clock	D	Q $\bar{Q}$
L	X	X	L H
H		H	H L
H		L	L H
H	L	X	no change



# MC54/74HC175

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC175

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figures 1 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
$t_{PHL}$	Maximum Propagation Delay, Reset to Q or $\bar{Q}$ (Figures 2 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, VCC = 5.0 V	pF
		35	

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{su}$	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_h$	Minimum Hold Time, Clock to Data (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_w$	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_r$ , $t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC175

## SWITCHING WAVEFORMS

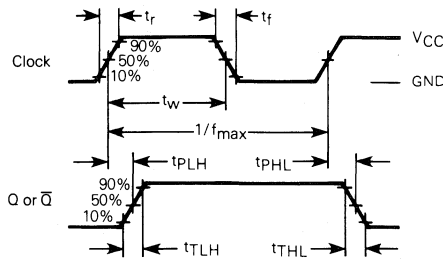


Figure 1.

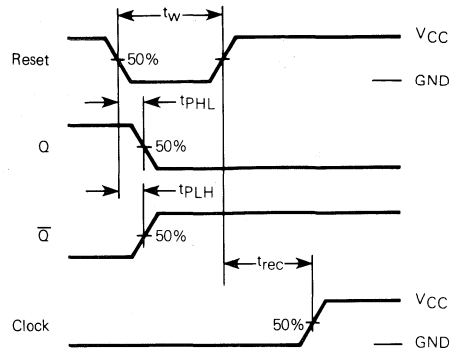


Figure 2.

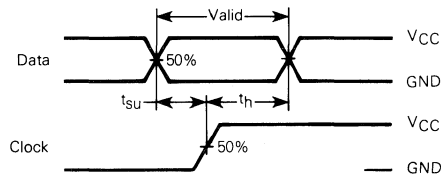
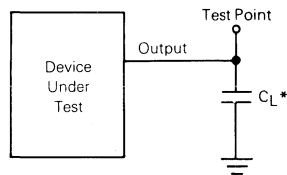


Figure 3.

### TEST CIRCUIT

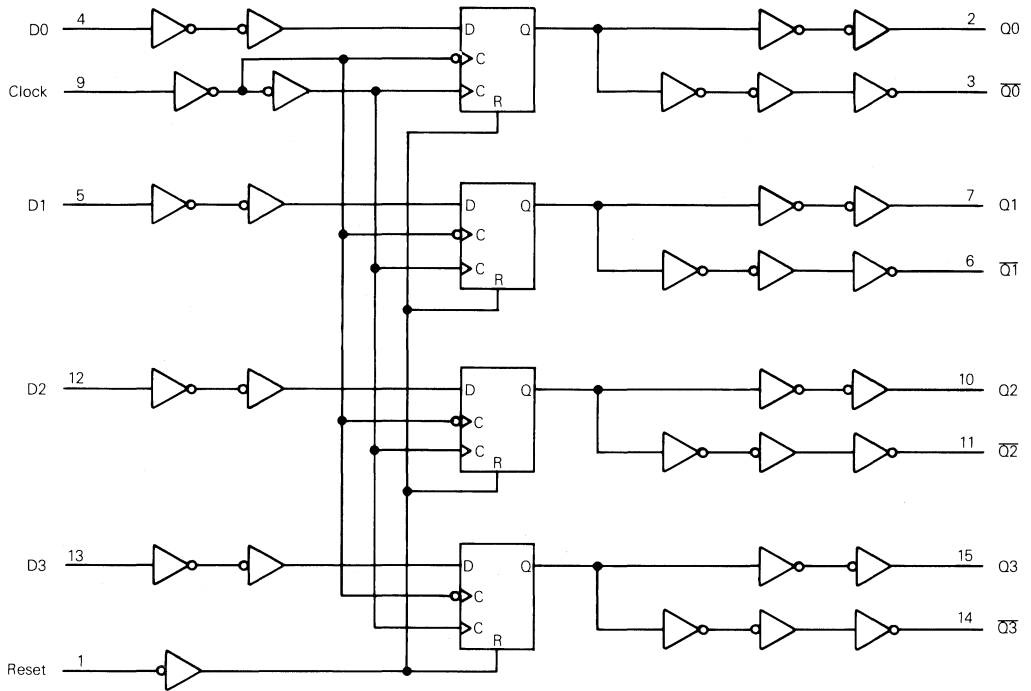


\* Includes all probe and jig capacitance.

Figure 4.

# MC54/74HC175

## EXPANDED LOGIC DIAGRAM



5

# 4-Bit Bidirectional Universal Shift Register

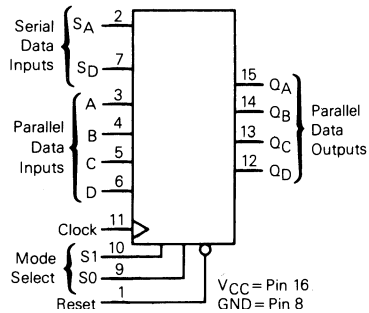
## High-Performance Silicon-Gate CMOS

The MC54/74HC194 is identical in pinout to the LS194 and the MC14194B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

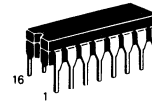
This static shift register features parallel load, serial load (shift right and shift left), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 164 FETs or 41 Equivalent Gates

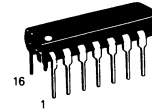
### LOGIC DIAGRAM



## MC54/74HC194



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



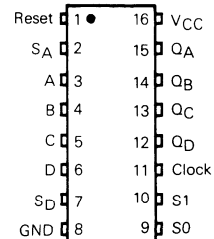
**N SUFFIX  
 PLASTIC  
 CASE 648-06**

### ORDERING INFORMATION

MC74HCXXXN Plastic  
 MC54HCXXXJ Ceramic

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Reset	Mode Select			Inputs				Outputs				Operating Mode		
	S1	S0	Clock	Serial Data		Parallel Data		QA	QB	QC	QD			
				SD	SA	A	B	C	D	QA	QB	QC	QD	
L	X	X	X	X	X	X	X	X	X	L	L	L	L	Reset
H	H	H	$\nearrow$	X	X	a	b	c	d	a	b	c	d	Parallel Load
H	L	H	$\nearrow$	X	H	X	X	X	X	H	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	Shift Right
H	L	H	$\nearrow$	X	L	X	X	X	X	L	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	Shift Left
H	H	L	$\nearrow$	H	X	X	X	X	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	H	Shift Left
H	H	L	$\nearrow$	L	X	X	X	X	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	L	Shift Left
H	L	L	X	X	X	X	X	X	X	no change			Hold	
H	X	X	L	X	X	X	X	X	X	no change				
H	X	X	H	X	X	X	X	X	X	no change				

H = high level (steady state)  
 L = low level (steady state)  
 X = don't care  
 $\nearrow$  = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.  
 QA<sub>n</sub>, QB<sub>n</sub>, QC<sub>n</sub>, QD<sub>n</sub> = the level of QA, QB, QC, or QD, respectively, before the most-recent  $\nearrow$  transition of the clock.

# MC54/74HC194

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	2.0	0.26	0.33	0.40	μA
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	2.0	±0.1	±1.0	±1.0	μA
			4.5	8	80	160	
			6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.

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# MC54/74HC194

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = CPD V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		90	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Parallel Data Inputs to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, S1 or S2 to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, S <sub>A</sub> or S <sub>D</sub> to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Clock to any Input (except Reset) (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC194

## PIN DESCRIPTIONS

### DATA INPUTS

- A, B, C, D (PINS 3, 4, 5, 6)** — Parallel data inputs.
- S<sub>A</sub> (PIN 2)** — Serial-data input when using shift-right mode.
- S<sub>D</sub> (PIN 7)** — Serial-data input when using shift-left mode.

### OUTPUTS

- Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, Q<sub>D</sub> (PINS 15, 14, 13, 12)** — Parallel data outputs.

### CONTROL INPUTS

**CLOCK (PIN 11)** — Clock Input. The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

**RESET (PIN 1)** — A low level applied to this pin resets all stages and forces all outputs low.

**S<sub>0</sub>, S<sub>1</sub> (PINS 9, 10)** — Mode-select inputs. These inputs control the mode of operation as described in the function table and below.

**Parallel Load Mode (S<sub>1</sub>=H, S<sub>0</sub>=H)** — Data is loaded into the device with a positive transition of the Clock input.

**Shift Right Mode (S<sub>1</sub>=L, S<sub>0</sub>=H)** — With a positive transition of the Clock input, each bit is shifted right (in the direction Q<sub>A</sub> toward Q<sub>D</sub>) one stage and data on the S<sub>A</sub> Serial Data Input is shifted into stage A.

**Shift Left Mode (S<sub>1</sub>=H, S<sub>0</sub>=L)** — With a positive transition of the Clock input, each bit is shifted left (in the direction Q<sub>D</sub> toward Q<sub>A</sub>) one stage and data on the S<sub>D</sub> Serial Data Input is shifted into stage D.

**Hold Mode (S<sub>1</sub>=L, S<sub>0</sub>=L)** — Outputs are held.

## SWITCHING WAVEFORMS

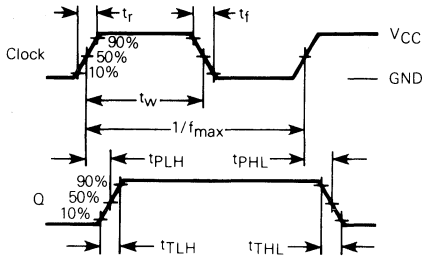


Figure 1.

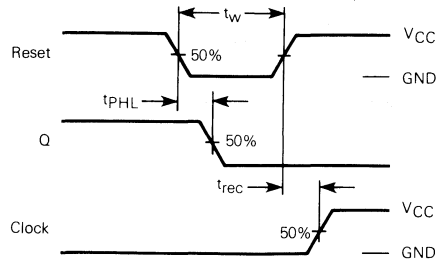


Figure 2.

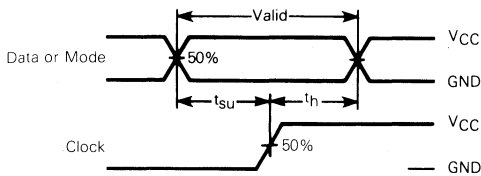
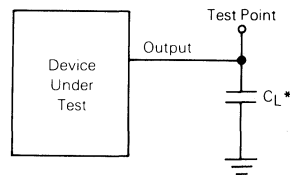


Figure 3.



\* Includes all probe and jig capacitance.

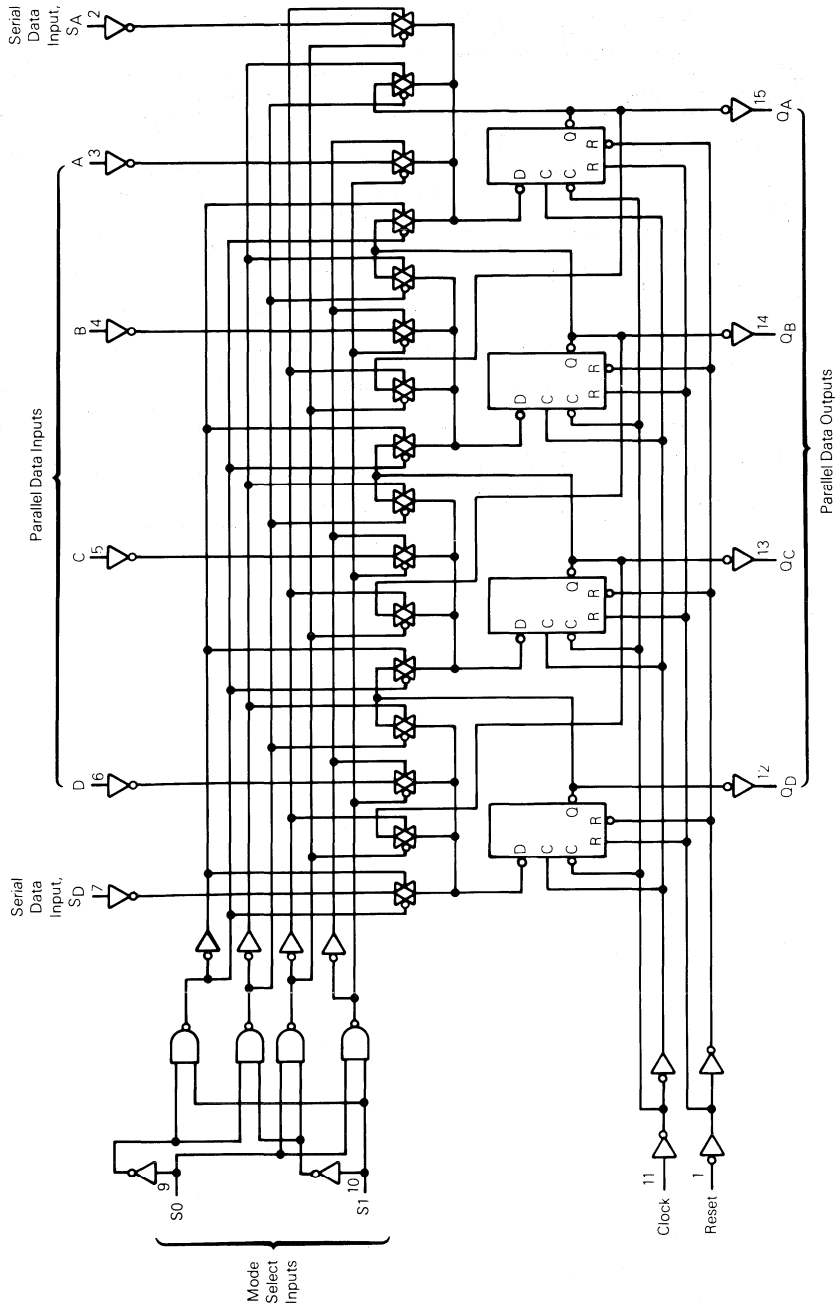
Figure 4. Test Circuit

5



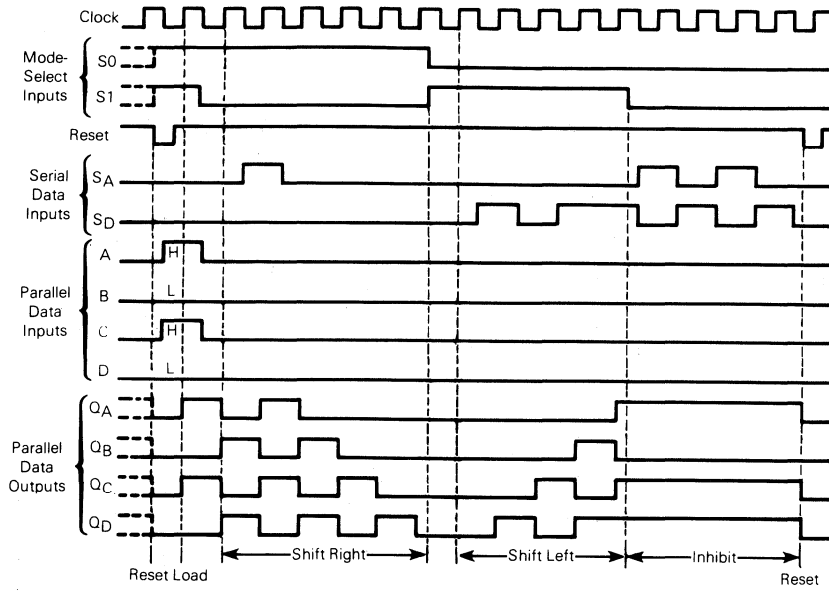
# MC54/74HC194

EXPANDED LOGIC DIAGRAM



# MC54/74HC194

## TIMING DIAGRAM



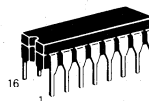
**MC54/74HC195**

**4-Bit Universal Shift Register**  
**High-Performance Silicon-Gate CMOS**

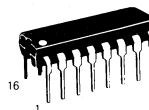
The MC54/74HC195 is identical in pinout to the LS195. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This static shift register features parallel load, serial load (shift right), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 150 FETs or 37.5 Equivalent Gates



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



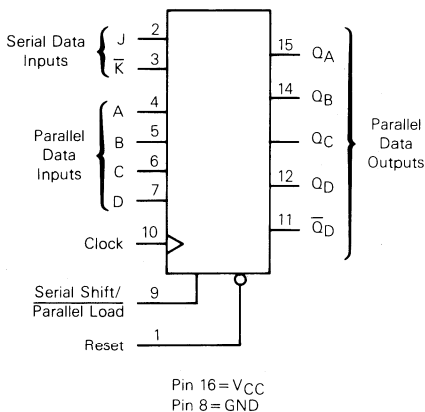
**N SUFFIX**  
**PLASTIC**  
**CASE 648-06**

**ORDERING INFORMATION**

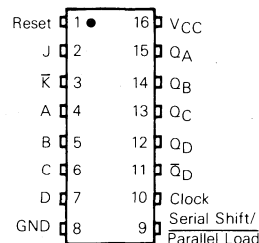
MC74HCXXXN Plastic  
 MC54HCXXXJ Ceramic

$T_A = -55^\circ$  to  $125^\circ$ C for all packages.  
 Dimensions in Chapter 6.

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**



**FUNCTION TABLE**

		Inputs						Outputs						
Reset	Shift/Load	Clock	Serial	Parallel			$Q_A$	$Q_B$	$Q_C$	$Q_D$	$\bar{Q}_D$	Operating Mode		
L	X	X	X X X X X X	X	X	X	L	L	L	L	H	Reset		
H	L		X X	a	b	c	a	b	c	d	$\bar{d}$	Parallel Load		
H	H	L	X X	X	X	X	no change					Hold		
H	H		L	H	X	X	$Q_{A0}$	$Q_{A0}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$	Serial Shift	Retain First Stage	
H	H		L	L	X	X	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$		Reset First Stage	
H	H		H	H	X	X	H	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$		Set First Stage	
H	H		H	L	X	X	$\bar{Q}_{An}$	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$		Toggle First Stage	

H = high level (steady state)  
 L = low level (steady state)  
 X = don't care  
 = transition from low to high level  
 a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

$Q_{A0}$  = the level of  $Q_A$  before the indicated steady-state input conditions were established.  
 $Q_{An}$ ,  $Q_{Bn}$ ,  $Q_{Cn}$  = the level of  $Q_A$ ,  $Q_B$ , or  $Q_C$ , respectively, before the most-recent transition of the clock.

# MC54/74HC195

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	0.26	0.33	0.40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	± 0.1	± 1.0	± 1.0	μA
			6.0	8	80	160	
			6.0	0.26	0.33	0.40	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC195

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to any Q or $\bar{Q}_D$ (Figures 1 and 5)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Reset to any Q or $\bar{Q}_D$ (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		95	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, A, B, C, D, J, or $\bar{K}$ to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>su</sub>	Minimum Setup Time, Serial Shift/Parallel Load to Clock (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Clock to A, B, C, D, J, or $\bar{K}$ (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>h</sub>	Minimum Hold Time, Clock to Serial Shift/Parallel Load (Figure 4)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC195

## PIN DESCRIPTION

### DATA INPUTS

A, B, C, D (PINS 4, 5, 6, 7) — Parallel data inputs.

### OUTPUTS

Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, Q<sub>D</sub>,  $\bar{Q}_D$  (PINS 15, 14, 13, 12, 11) — Parallel data outputs.

### CONTROL INPUTS

**CLOCK (PIN 10)** — Clock input. The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

**SERIAL SHIFT/PARALLEL LOAD (PIN 9)** — Shift or load control. A low level applied to this pin allows data to be loaded from the parallel inputs. Data is loaded with the positive transition of the Clock input. A high level allows data to be shifted in the manner dictated by the J and  $\bar{K}$  control inputs.

**RESET (PIN 1)** — A low level applied to this pin resets all stages and forces all outputs low.

**J,  $\bar{K}$  (PINS 2, 3)** — Shift Control. With Serial Shift/Parallel Load high, J and  $\bar{K}$  control the mode of operation, as illustrated in the Function Table.

**J = L,  $\bar{K} = H$**  — With a positive transition of the Clock input, each bit is shifted to the right (in the direction Q<sub>A</sub> toward Q<sub>D</sub>) one stage and stage A maintains its previous state.

**J = H,  $\bar{K} = L$**  — With a positive transition of the Clock input, each bit is shifted right (in the direction of Q<sub>A</sub> toward Q<sub>D</sub>) one stage and the Q<sub>A</sub> output is inverted.

**J =  $\bar{K} = L$**  — With a positive transition of the Clock input, each bit is shifted right (in the direction Q<sub>A</sub> toward Q<sub>D</sub>) one stage and a low is loaded into stage A.

**J =  $\bar{K} = H$**  — With a positive transition of the Clock input, each bit is shifted right (in the direction Q<sub>A</sub> toward Q<sub>D</sub>) one stage and a high is loaded into stage A.

## SWITCHING WAVEFORMS

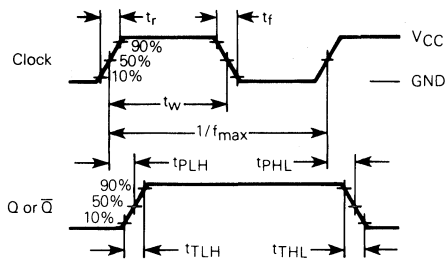


Figure 1.

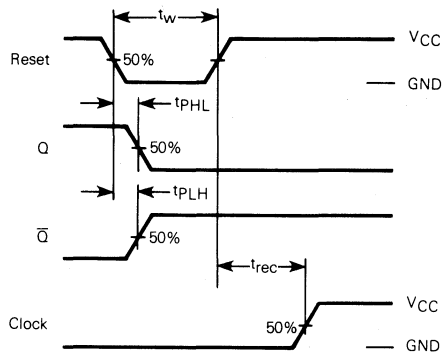


Figure 2.

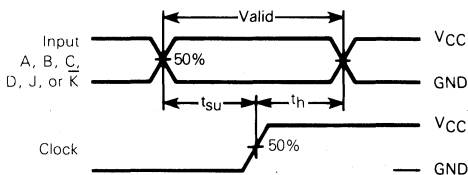


Figure 3.

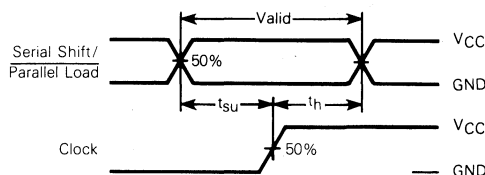
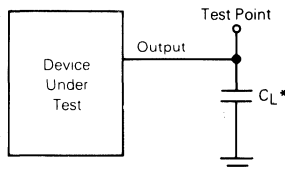


Figure 4.

## TEST CIRCUIT

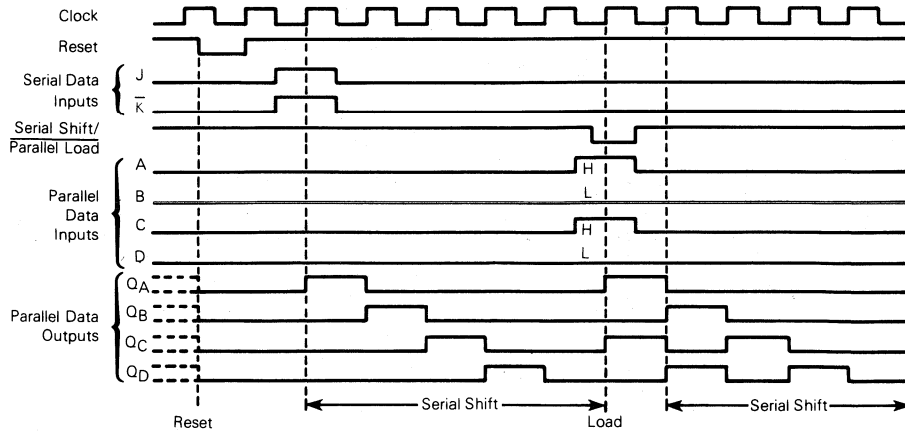


\* Includes all probe and jig capacitance.

Figure 5.

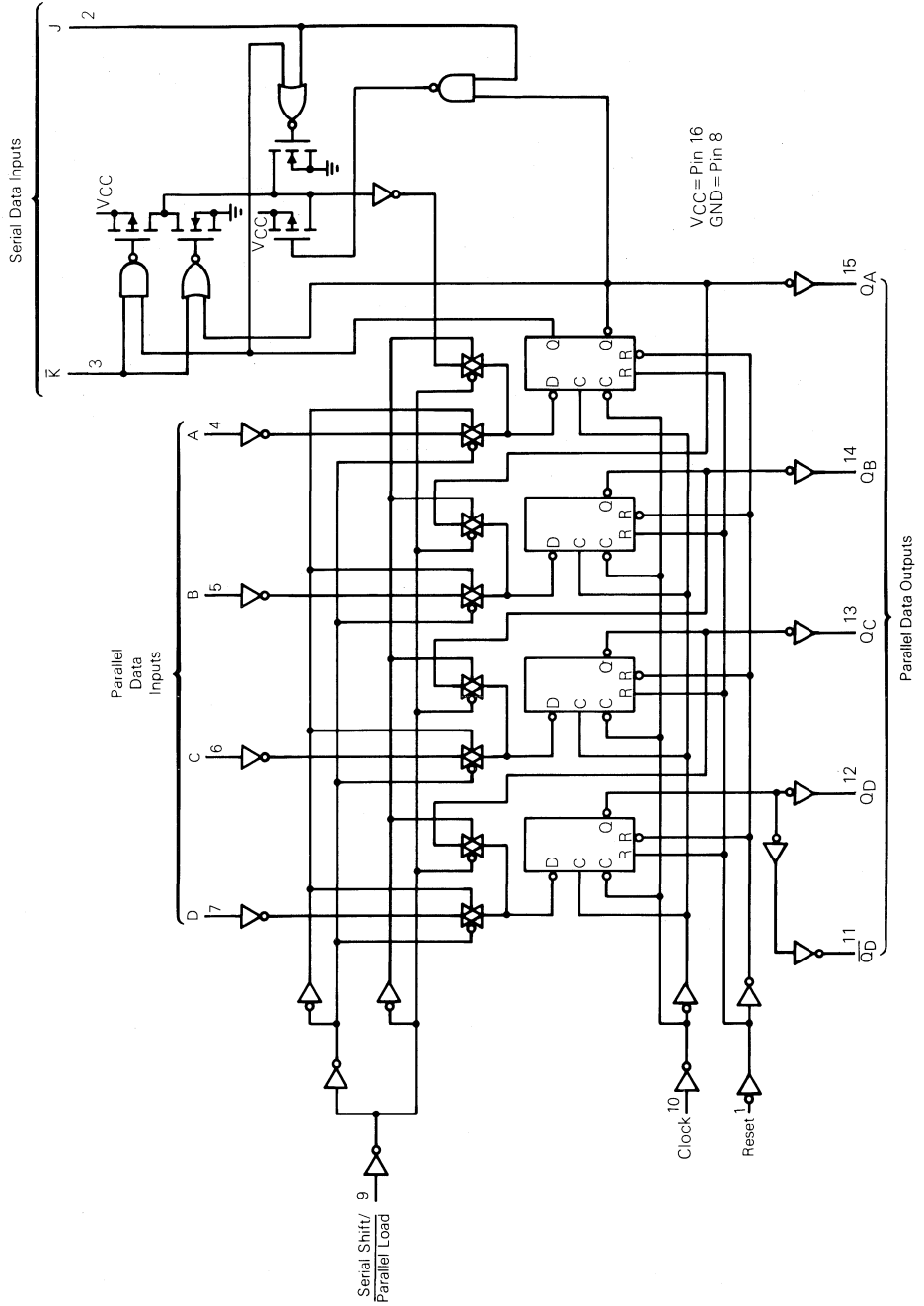
# MC54/74HC195

## TIMING DIAGRAM



# MC54/74HC195

## EXPANDED LOGIC DETAIL





**MC54/74HC237**

**1-of-8 Decoder/Demultiplexer  
 with Address Latch**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC237 is identical in pinout to the LS137, but has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC237 decodes a three-bit Address to one-of-eight active-high outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC237 is the noninverting version of the HC137.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 156 FETs or 39 Equivalent Gates



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



**N SUFFIX  
 PLASTIC  
 CASE 648-06**

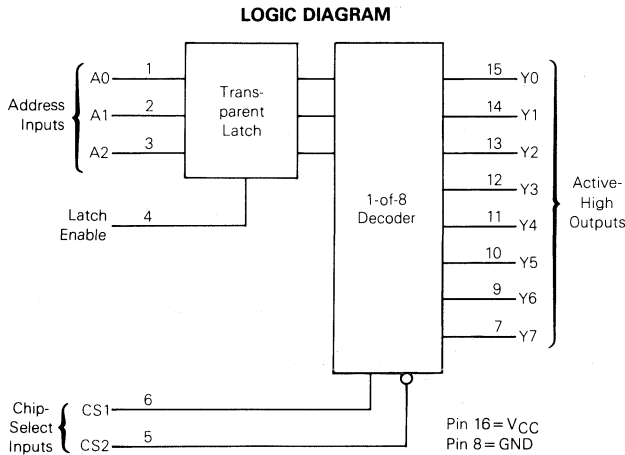


**D SUFFIX  
 SOIC  
 CASE 751B-04**

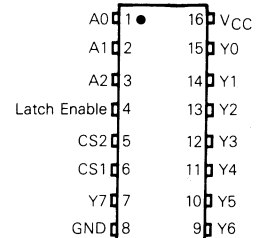
**ORDERING INFORMATION**

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs					Outputs								
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	L	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L
L	H	L	H	H	H	L	L	L	L	L	L	L	L
H	H	L	X	X	X	*							

\* = Depends upon the Address previously applied while LE was at a low level.

# MC54/74HC237

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 2)	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out}  \leq 20$ $\mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out}  \leq 20$ $\mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0$ mA $ I_{out}  \leq 5.2$ mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ $\mu\text{A}$	6.0	8	80	160	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC237

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 6)	2.0	235	295	355	ns
		4.5	47	59	71	
		6.0	40	50	60	
t <sub>PHL</sub>		2.0	185	230	280	
		4.5	37	46	56	
		6.0	31	39	48	
t <sub>PLH</sub>	Maximum Propagation Delay, CS2 to Output Y (Figures 2 and 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t <sub>PHL</sub>		2.0	145	180	220	
		4.5	29	36	44	
		6.0	25	31	38	
t <sub>PLH</sub>	Maximum Propagation Delay, CS1 to Output Y (Figures 3 and 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t <sub>PHL</sub>		2.0	160	200	240	
		4.5	32	40	48	
		6.0	27	34	41	
t <sub>PLH</sub>	Maximum Propagation Delay, Latch Enable to Output Y (Figures 4 and 6)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t <sub>PHL</sub>		2.0	190	240	285	
		4.5	38	48	57	
		6.0	32	41	48	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		100	

5

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Input A to Latch Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input A (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 2)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC237

## PIN DESCRIPTIONS

### ADDRESS INPUTS

**A0, A1, A2 (PINS 1, 2, 3)** — Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

### CONTROL INPUTS

**CS1, CS2 (PINS 6, 5)** — Chip select inputs. For CS1 at a high level and CS2 at a low level, the chip is enabled and the outputs follow the data inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs are at a low level.

**LATCH ENABLE (PIN 4)** — Latch Enable input. A high level at this input latches the Address. A low level at this input allows the outputs to follow the Address (CS1=H and CS2=L).

### OUTPUTS

**Y0-Y7 (PINS 15, 14, 13, 12, 11, 10, 9, 7)** — Active-high outputs. One of these eight outputs is selected when the chip is enabled (CS1=H and CS2=L) and the Address inputs correspond to that particular output. The selected output is at a high level while all others remain at a low level.

## SWITCHING WAVEFORMS

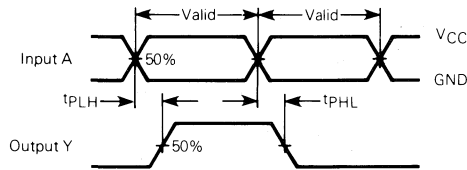


Figure 1.

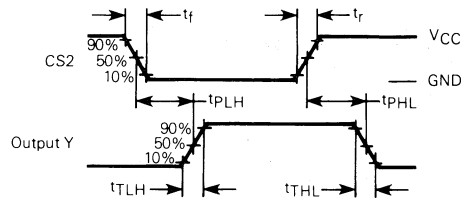


Figure 2.

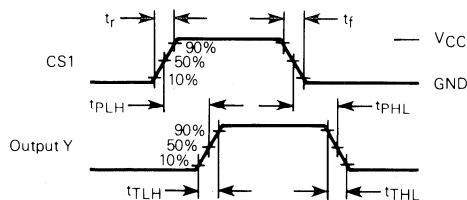


Figure 3.

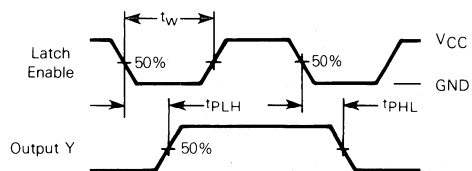


Figure 4.

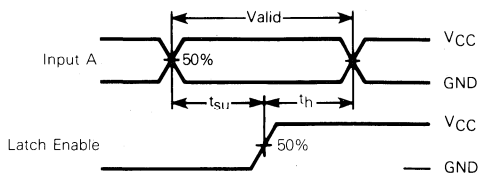
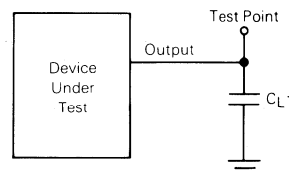


Figure 5.



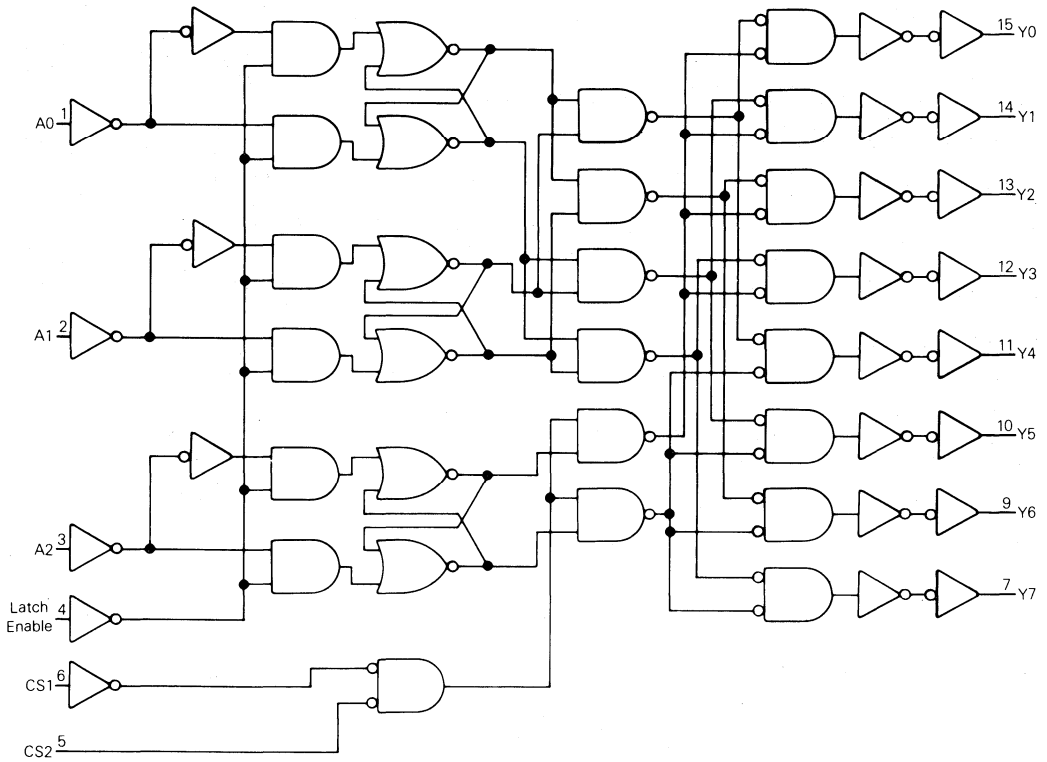
\* Includes all probe and jig capacitance.

Figure 6. Test Circuit

5

# MC54/74HC237

## EXPANDED LOGIC DIAGRAM



**MC54/74HC240A**

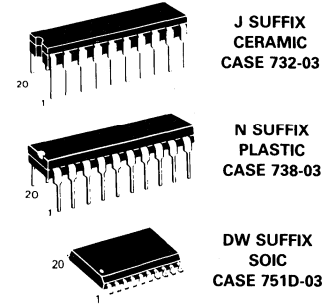
**Octal 3-State Inverting Buffer/  
 Line Driver/Line Receiver**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC240A is identical in pinout to the LS240. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other sub-oriented systems. The device has inverting outputs and two active-low output enables.

The HC240A is similar in function to the HC241A and HC244A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 120 FETs or 30 Equivalent Gates

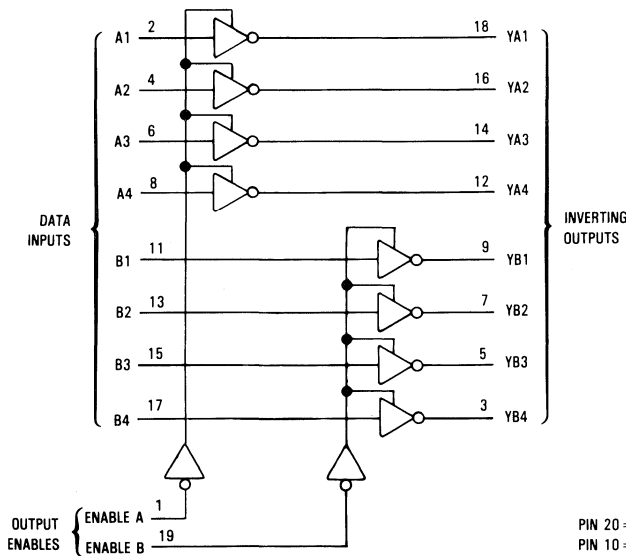


**ORDERING INFORMATION**

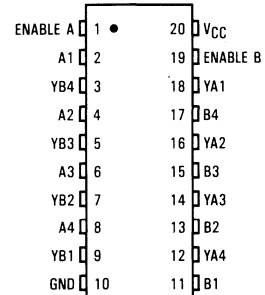
MC74HCXXXAN Plastic  
 MC54HCXXXAJ Ceramic  
 MC74HCXXXADW SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	H
L	H	L
H	X	Z

Z = high impedance

PIN 20 =  $V_{CC}$   
 PIN 10 = GND

# MC54/74HC240A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA	6.0	5.9	5.9	5.9	
			6.0	3.98	3.84	3.70	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 6.0 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
			6.0	±0.5	±5.0	±10.0	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 4.

# MC54/74HC240A

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	

NOTE: For propagation delays with loads other than 50 pF, see Chapter 4.

## SWITCHING WAVEFORMS

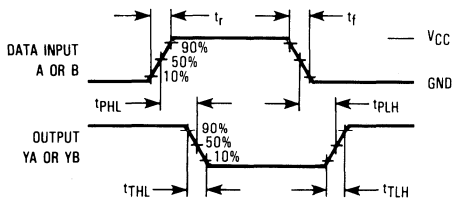


Figure 1

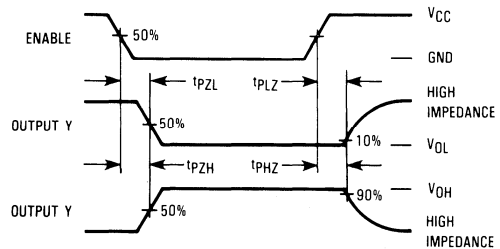
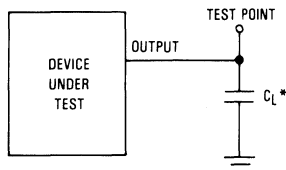
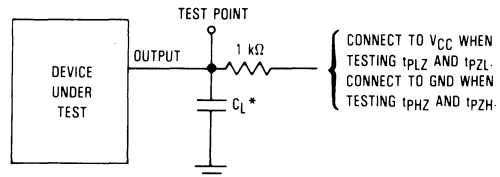


Figure 2



\*Includes all probe and jig capacitance.

Figure 3. Test Circuit



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit



# MC54/74HC240A

## PIN DESCRIPTIONS

### INPUTS

**A1, A2, A3, A4, B1, B2, B3, B4 (Pins 2, 4, 6, 8, 11, 13, 15, 17)** — Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROLS

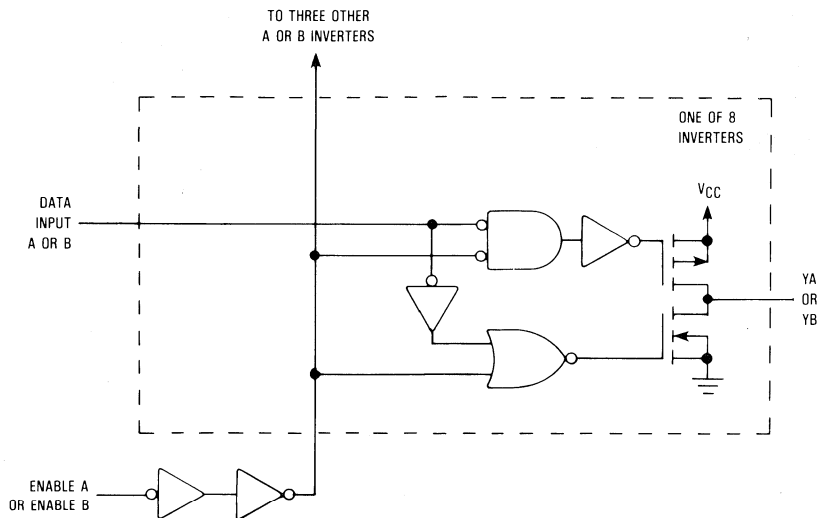
**Enable A, Enable B (Pins 1, 19)** — Output enables (active-low). When a low level is applied to these pins, the outputs

are enabled and the devices function as inverters. When a high level is applied, the outputs assume the high-impedance state.

### OUTPUTS

**YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (Pins 18, 16, 14, 12, 9, 7, 5, 3)** — Device outputs. Depending upon the state of the output-enable pins, these outputs are either inverting outputs or high-impedance outputs.

## LOGIC DETAIL



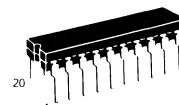
# Octal 3-State Inverting Buffer/ Line Driver/Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT240A is identical in pinout to the LS240. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT240A is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

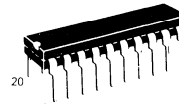
The HCT240A is the inverting version of the HCT244. See also HCT241.

- Output Drive Capability: 15 LSTTL Loads
- TTL NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 110 FETs or 27.5 Equivalent Gates

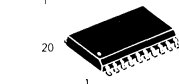
## MC54/74HCT240A



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03



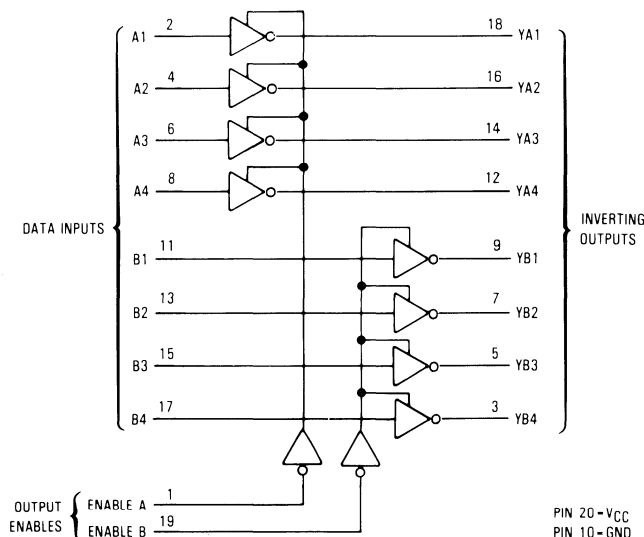
DW SUFFIX  
 SOIC  
 CASE 751D-03

### ORDERING INFORMATION

MC74HCTXXXAN	Plastic
MC54HCTXXXAJ	Ceramic
MC74HCTXXXADW	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### LOGIC DIAGRAM



### PIN ASSIGNMENT

ENABLE A	1	20	V <sub>CC</sub>
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

### FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	H
L	H	L
H	X	Z

Z = High Impedance  
 X = Don't Care

# MC54/74HCT240A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating – Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2	2	2	V
			5.5	2	2	2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6 mA	4.5	0.26	0.33	0.4	μA
			5.5	±0.1	±1	±1	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	±0.5	±5	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4	40	160	μA

ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	≥ -55°C	25°C to 125°C	mA
			5.5	2.9	

### NOTES:

- Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 4.
- Total Supply Current - I<sub>CC</sub> + ΔI<sub>CC</sub>.

# MC54/74HCT240A

AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	20	25	30	ns
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	28	35	42	ns
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	25	31	38	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

$C_{PD}$	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical ( $\alpha$ 25°C, $V_{CC} = 5 \text{ V}$ )	
			55

NOTE: 1. For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

## SWITCHING WAVEFORMS

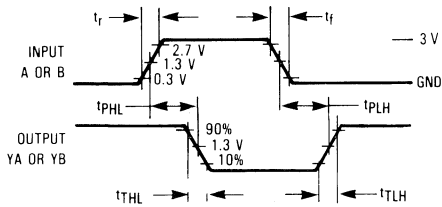


Figure 1.

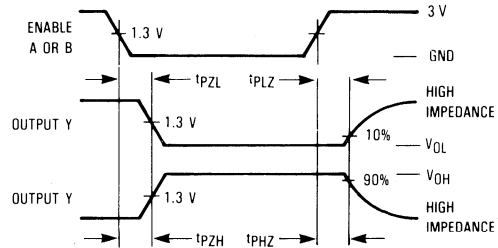
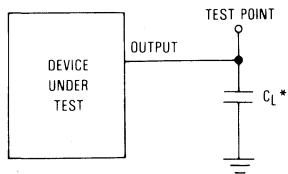
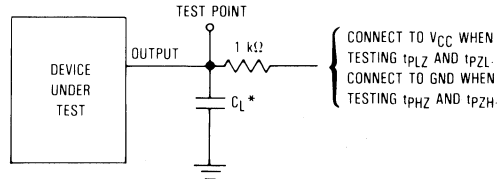


Figure 2.



\*Includes all probe and jig capacitance.

Figure 3. Test Circuit

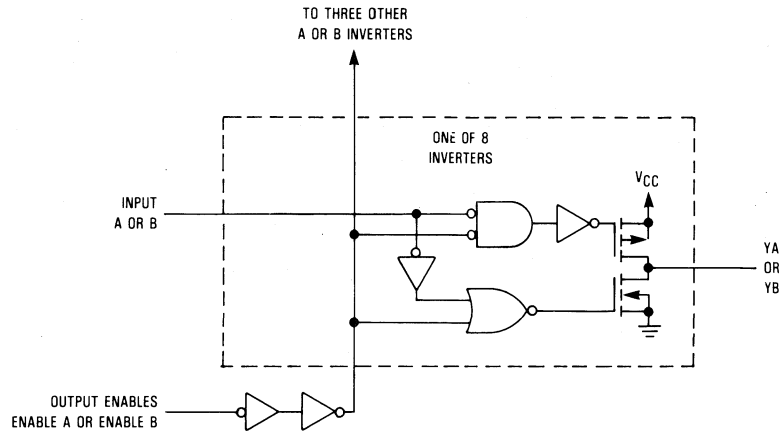


\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

# MC54/74HCT240A

## LOGIC DETAIL



# Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

## High-Performance Silicon-Gate CMOS

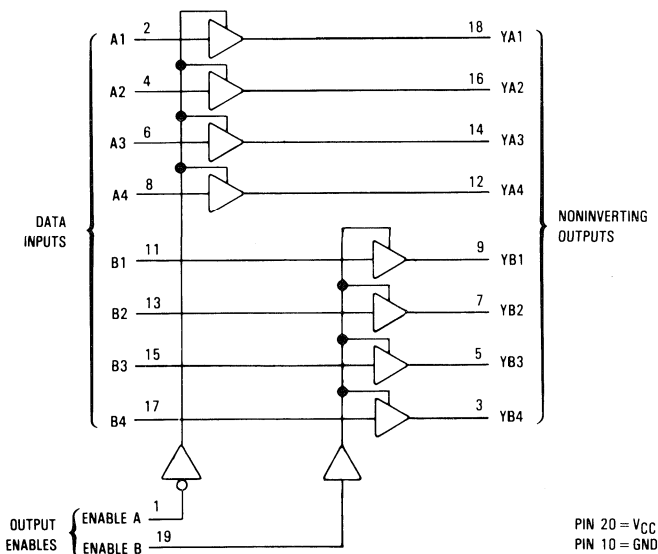
The MC54/74HC241A is identical in pinout to the LS241. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other sub-oriented systems. The device has noninverted outputs and two output enables. Enable A is active-low and Enable B is active-high.

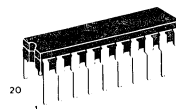
The HC241A is similar in function to the HC244A and HC240A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

### LOGIC DIAGRAM



## MC54/74HC241A



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03



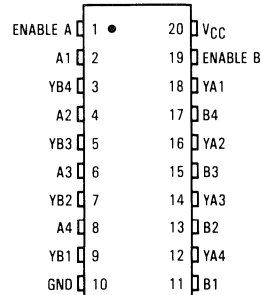
DW SUFFIX  
 SOIC  
 CASE 751D-03

### ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXADW	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output		Inputs		Output	
Enable A	A	YA	Enable B	B	YB		
L	L	L	H	L	L	L	L
L	H	H	H	H	H	H	H
H	X	Z	L	X	Z		

Z = high impedance

# MC54/74HC241A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 35$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			$V_{in} = V_{IH}$ $ I_{out}  \leq 6.0 \text{ mA}$ $ I_{out}  \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			$V_{in} = V_{IL}$ $ I_{out}  \leq 6.0 \text{ mA}$ $ I_{out}  \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND	6.0	$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	4	40	160	$\mu\text{A}$

NOTE: Information on typical parametric values along with high frequency or heavy load considerations, can be found in Chapter 4.

# MC54/74HC241A

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0	90	115	135	ns
		4.5	18	23	27	
		6.0	15	20	23	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

## SWITCHING WAVEFORMS

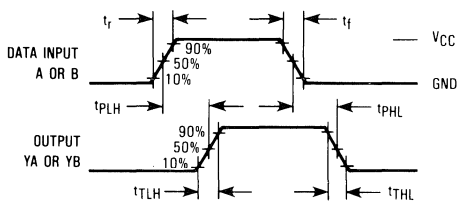


Figure 1

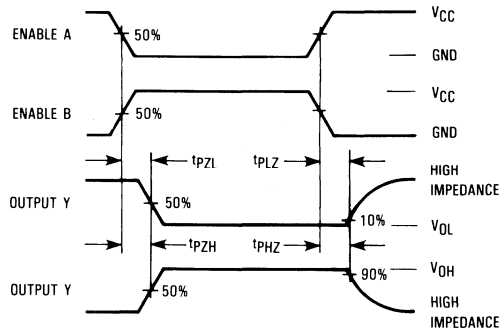
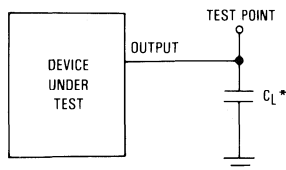
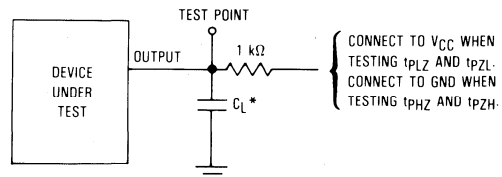


Figure 2



\*Includes all probe and jig capacitance.

Figure 3. Test Circuit



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit



# MC54/74HC241A

## PIN DESCRIPTIONS

### INPUTS

**A1, A2, A3, A4, B1, B2, B3, B4 (PINS 2, 4, 6, 8, 11, 13, 15, 17)** — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs when the outputs are enabled.

### CONTROLS

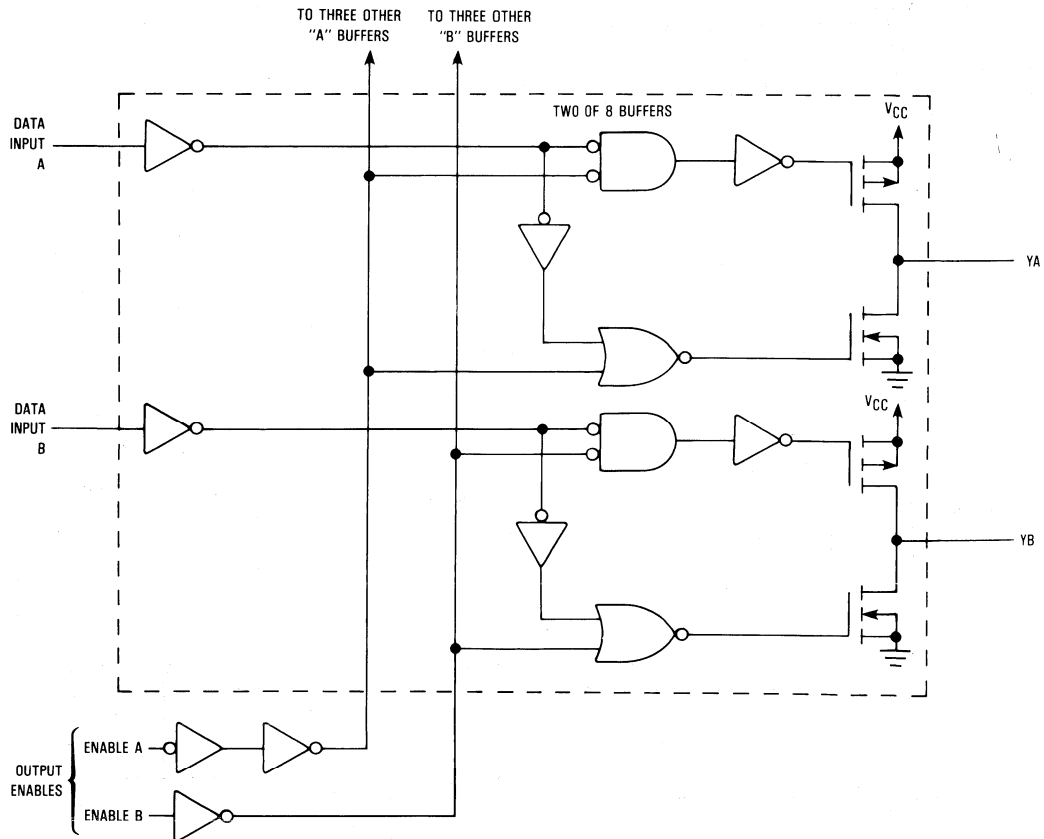
**Enable A (PIN 1)** — Output enable (active-low). When a low level is applied to this pin, the outputs of the "A" devices are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high-impedance state.

**Enable B (PIN 19)** — Output enable (active-high). When a high level is applied to this pin, the outputs of the "B" devices are enabled and the devices function as noninverting buffers. When a low level is applied, the outputs assume the high-impedance state.

### OUTPUTS

**YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (PINS 18, 16, 14, 12, 9, 7, 5, 3)** — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

## LOGIC DETAIL



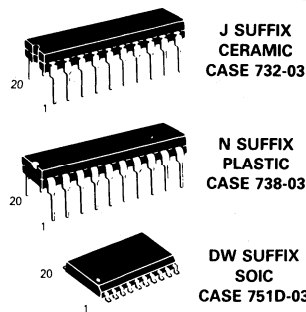
**MC54/74HCT241A**

**Octal 3-State Noninverting  
 Buffer/Line Driver/Line Receiver  
 with LSTTL-Compatible Inputs  
 High-Performance Silicon-Gate CMOS**

The MC54/74HCT241A is identical in pinout to the LS241. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT241A is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two output enables. Enable A is active-low and Enable B is active-high.

The HCT241A is similar in function to the HCT244. See also HCT240.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 118 FETs or 29.5 Equivalent Gates



**ORDERING INFORMATION**

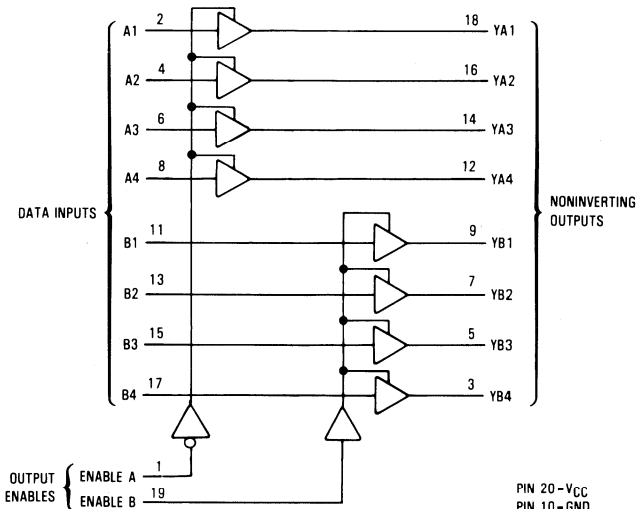
MC74HCTXXXAN	Plastic
MC54HCTXXXAJ	Ceramic
MC74HCTXXXADW	SOIC

$T_A = -55^\circ$  to  $125^\circ$ C for all packages.  
 Dimensions in Chapter 6.

**PIN ASSIGNMENT**

ENABLE A	1	20	V <sub>CC</sub>
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

**LOGIC DIAGRAM**



**FUNCTION TABLE**

Inputs		Output	
Enable A	A	YA	
L	L	L	
L	H	H	
H	X	Z	
Inputs		Output	
Enable B	B	YB	
H	L	L	
H	H	H	
L	X	Z	

Z = high impedance  
 X = don't care

5

# MC54/74HCT241A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
†Derating – Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C  
For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2	2	2	V
			5.5	2	2	2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	4.5	0.26	0.33	0.4	μA
			5.5	±0.1	±1	±1	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	±0.5	±5	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4	40	160	μA

ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

### NOTES:

- Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 4.
- Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

5

# MC54/74HCT241A

AC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5.0\text{ V} \pm 10\%$ ,  $C_L=50\text{ pF}$ , Input  $t_r = t_f = 6\text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	23	29	35	ns
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	26	33	39	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

$C_{PD}$	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical ( $\alpha 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ )	pF
		55	

NOTE: 1. For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

## SWITCHING WAVEFORMS

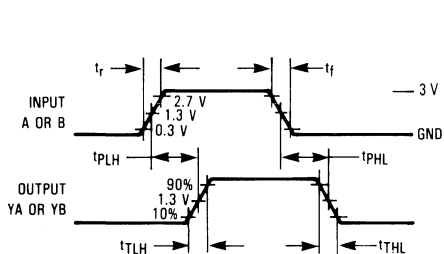


Figure 1.

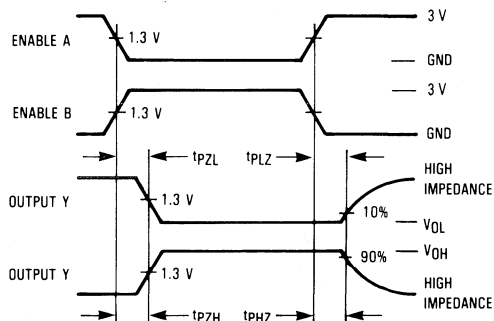
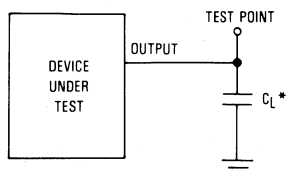
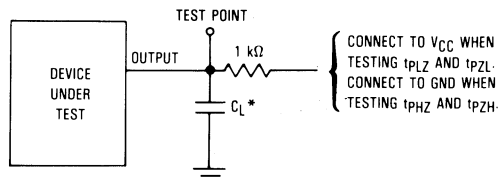


Figure 2.



\*Includes all probe and jig capacitance.

Figure 3. Test Circuit

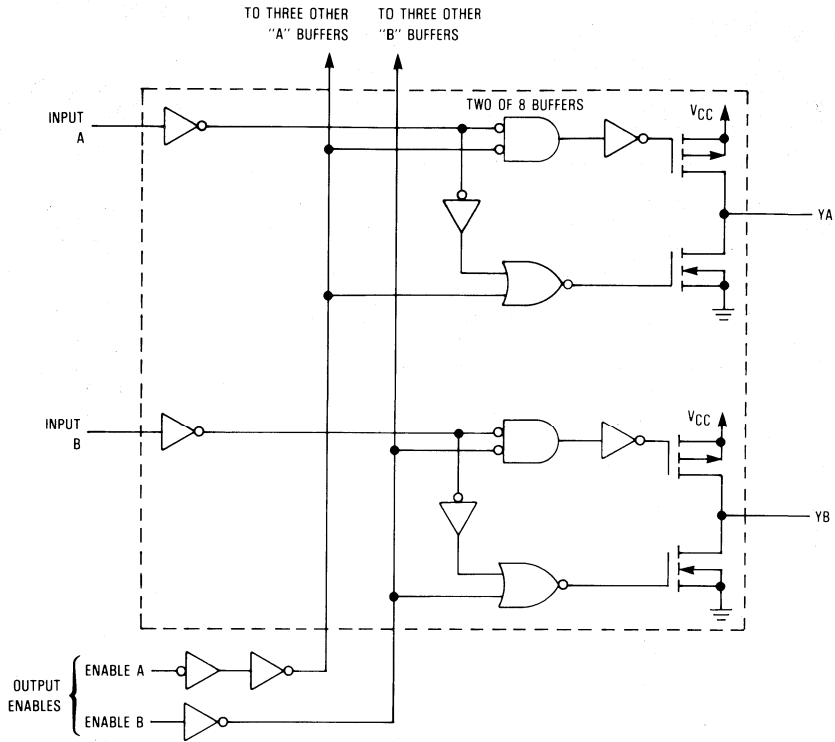


\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

# MC54/74HCT241A

## LOGIC DETAIL



**MC54/74HC244A**

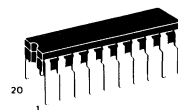
**Octal 3-State Noninverting  
 Buffer/Line Driver/  
 Line Receiver**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC244A is identical in pinout to the LS244. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

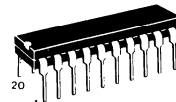
This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs and two active-low output enables.

The HC244A is similar in function to the HC240A and HC241A.

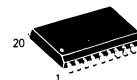
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates



**J SUFFIX  
 CERAMIC  
 CASE 732-03**



**N SUFFIX  
 PLASTIC  
 CASE 738-03**



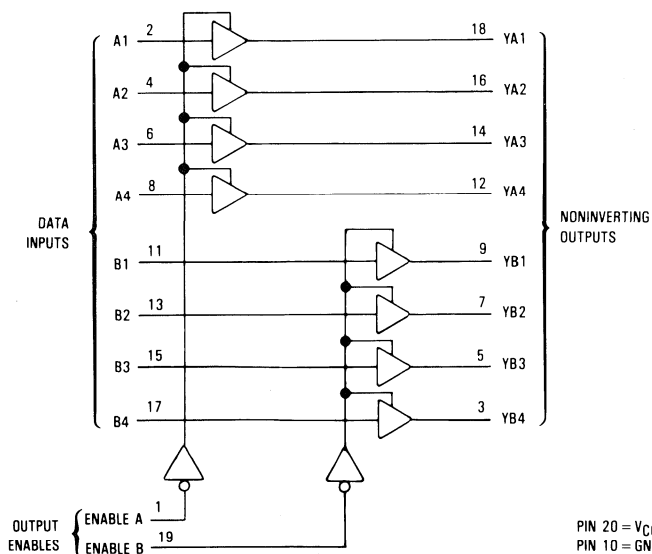
**DW SUFFIX  
 SOIC  
 CASE 751D-03**

**ORDERING INFORMATION**

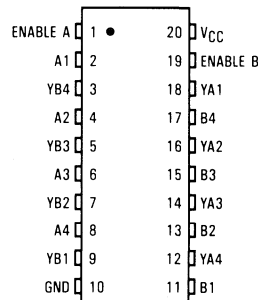
MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXADW	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance

PIN 20 = VCC  
 PIN 10 = GND

# MC54/74HC244A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 35$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		$V_{in} = V_{IH}$ $ I_{out}  \leq 6.0 \text{ mA}$ $ I_{out}  \leq 7.8 \text{ mA}$	6.0	5.9	5.9	5.9	
			6.0	5.98	5.34	3.70 5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		$V_{in} = V_{IL}$ $ I_{out}  \leq 6.0 \text{ mA}$ $ I_{out}  \leq 7.8 \text{ mA}$	6.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.40	
6.0	0.26	0.33	0.40				
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND	6.0	$\pm 0.5$	+5.0	$\pm 10.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	4	40	160	$\mu\text{A}$

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 4.

# MC54/74HC244A

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0 4.5 6.0	96 18 15	115 23 20	135 27 23	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		34	

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

## SWITCHING WAVEFORMS

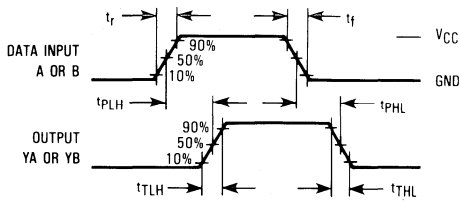


Figure 1.

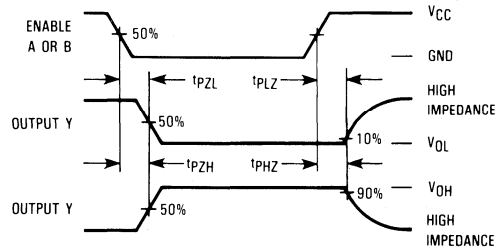
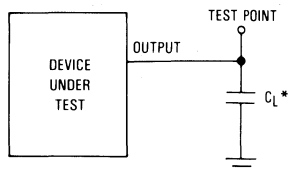


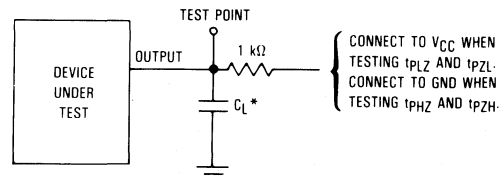
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.



\*Includes all probe and jig capacitance.

Figure 4.



# MC54/74HC244A

## PIN DESCRIPTIONS

### INPUTS

**A1, A2, A3, A4, B1, B2, B3, B4 (PINS 2, 4, 6, 8, 11, 13, 15, 17)** — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROLS

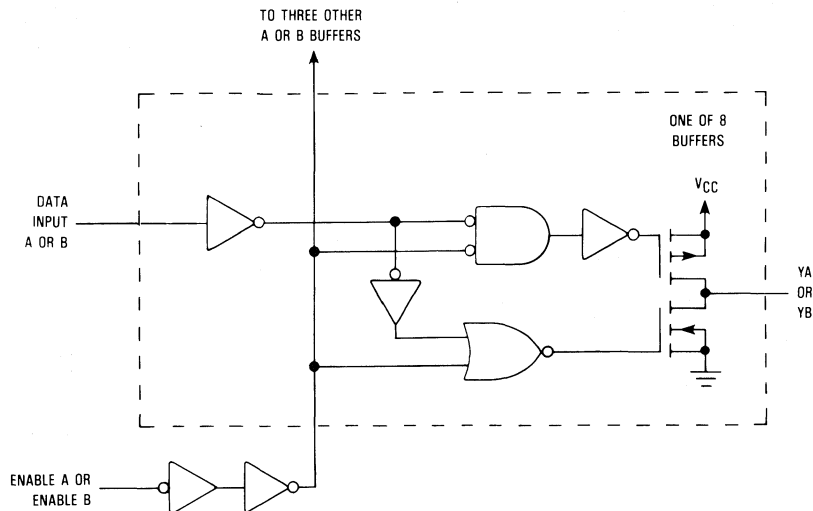
**Enable A, Enable B (PINS 1, 19)** — Output enables (active-low). When a low level is applied to these pins, the outputs

are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high-impedance state.

### OUTPUTS

**YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (PINS 18, 16, 14, 12, 9, 7, 5, 3)** — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

## LOGIC DETAIL



# Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs

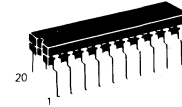
## High-Performance Silicon-Gate CMOS

The MC54/74HCT244A is identical in pinout to the LS244. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT244A is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two active-low output enables.

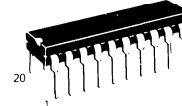
The HCT244A is the noninverting version of the HCT240. See also HCT241.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 112 FETs or 28 Equivalent Gates

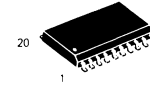
### MC54/74HCT244A



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03



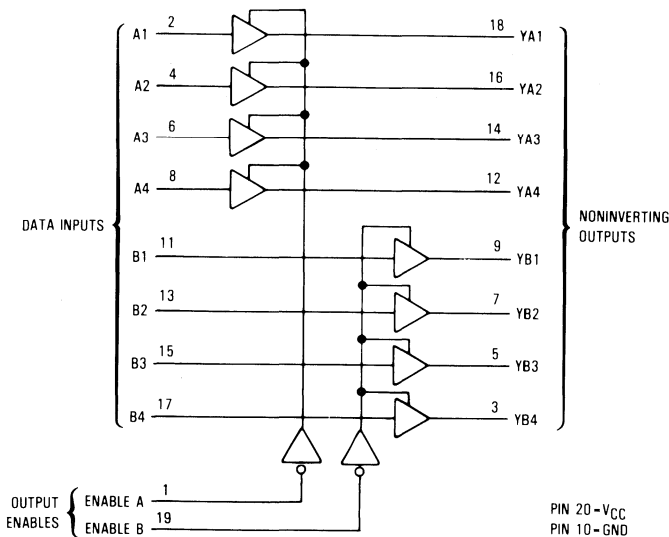
DW SUFFIX  
 SOIC  
 CASE 751D-03

#### ORDERING INFORMATION

MC74HCTXXXAN	Plastic
MC54HCTXXXAJ	Ceramic
MC74HCTXXXADW	SOIC

$T_A = -55^\circ$  to  $125^\circ$ C for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT

ENABLE A	1	20	V <sub>CC</sub>
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

#### FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance  
 X = don't care

# MC54/74HCT244A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2	2	2	V
			5.5	2	2	2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6 mA	4.5	3.98	3.84	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6 mA	4.5	0.26	0.33	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5	±0.1	±1	±1	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	±0.5	±5	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4	40	160	μA

ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

### NOTES:

- Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 4.
- Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

5

# MC54/74HCT244A

AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	20	25	30	ns
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	26	33	39	ns
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	22	28	33	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

$C_{PD}$	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical (at 25°C, $V_{CC} = 5 \text{ V}$ )	pF
		55	

NOTE: 1. For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

## SWITCHING WAVEFORMS

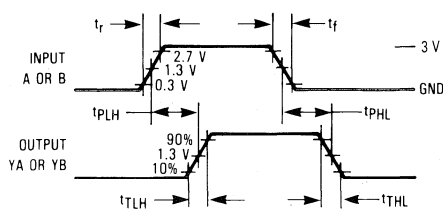


Figure 1.

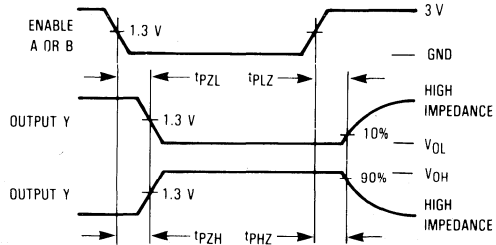
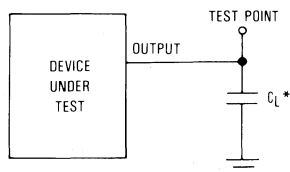


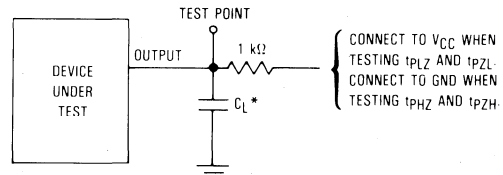
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.

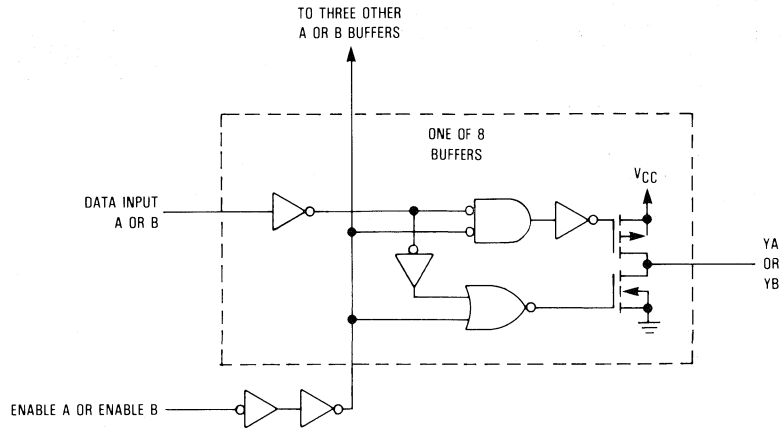


\*Includes all probe and jig capacitance.

Figure 4.

# MC54/74HCT244A

## LOGIC DETAIL



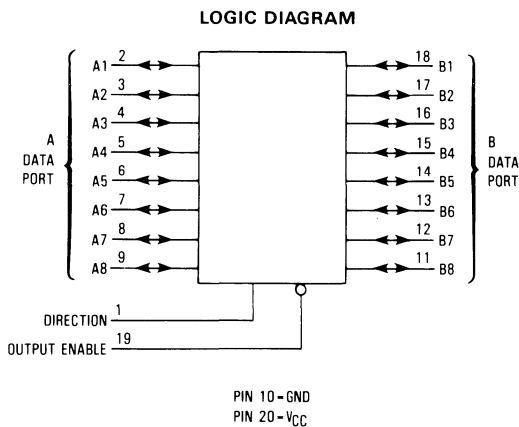
# Octal 3-State Noninverting Bus Transceiver

## High-Performance Silicon-Gate CMOS

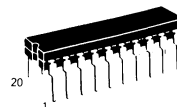
The MC54/74HC245A is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

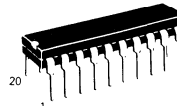
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 308 FETs or 77 Equivalent Gates



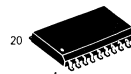
# MC54/74HC245A



**J SUFFIX**  
**CERAMIC**  
**CASE 732-03**



**N SUFFIX**  
**PLASTIC**  
**CASE 738-02**



**DW SUFFIX**  
**SOIC**  
**CASE 751D-03**

### ORDERING INFORMATION

MC74HCXXXAN Plastic  
 MC54HCXXXAJ Ceramic  
 MC74HCXXXADW SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT

DIRECTION	1	20	V <sub>CC</sub>
A1	2	19	OUTPUT ENABLE
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

### FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

X = don't care

# MC54/74HC245A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin 1 or 19	±20	mA
$I_{I/O}$	DC I/O Current, per I/O Pin	±35	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	±75	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 6.0 \text{ mA}$ $ I_{out}  \leq 7.8 \text{ mA}$	6.0	5.9	5.9	5.9	
			6.0	5.48	5.34	5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 6.0 \text{ mA}$ $ I_{out}  \leq 7.8 \text{ mA}$	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
6.0	0.26	0.33	0.40				
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND, Pin 1 or 19	6.0	±0.1	±1.0	±1.0	μA
$I_{OZ}$	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND, I/O Pins	6.0	±0.5	±5.0	±10.0	μA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	4	40	160	μA

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 4.

5

# MC54/74HC245A

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
$C_{in}$	Maximum Input Capacitance (Pin 1 or Pin 19)	—	10	10	10	pF
$C_{out}$	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	—	15	15	15	pF

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		40	

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

## SWITCHING WAVEFORMS

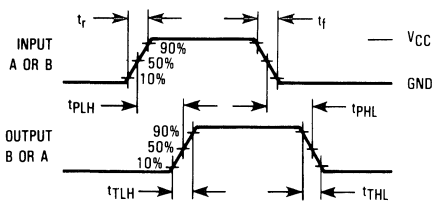


Figure 1.

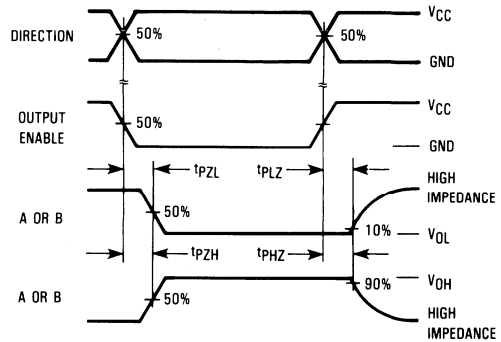
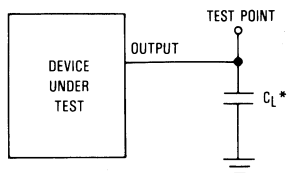


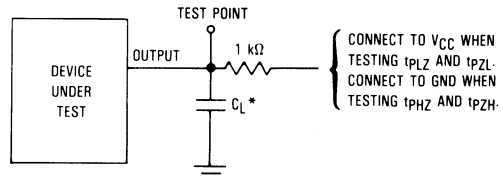
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.



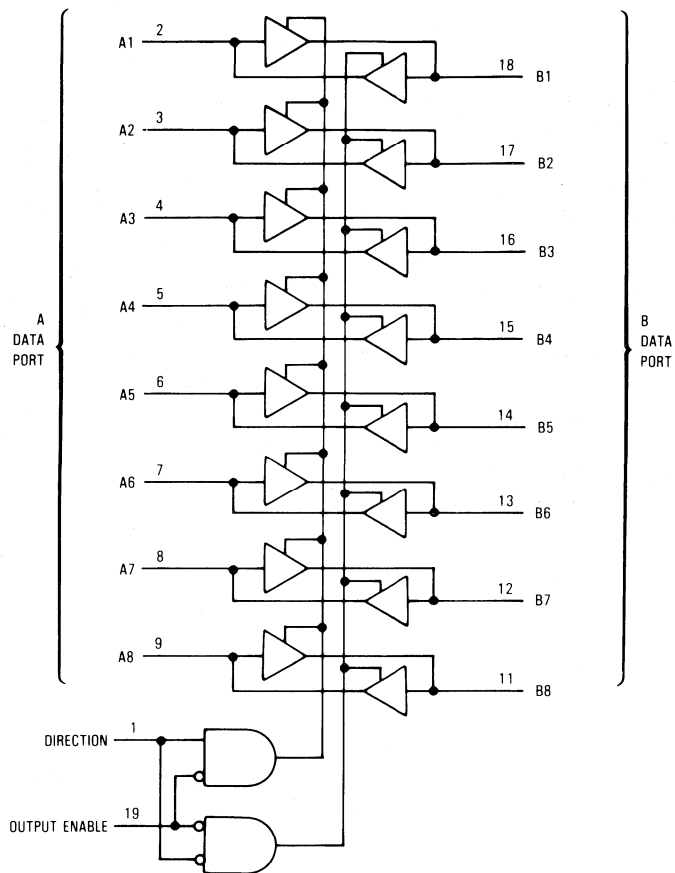
\*Includes all probe and jig capacitance.

Figure 4.



# MC54/74HC245A

## EXPANDED LOGIC DIAGRAM

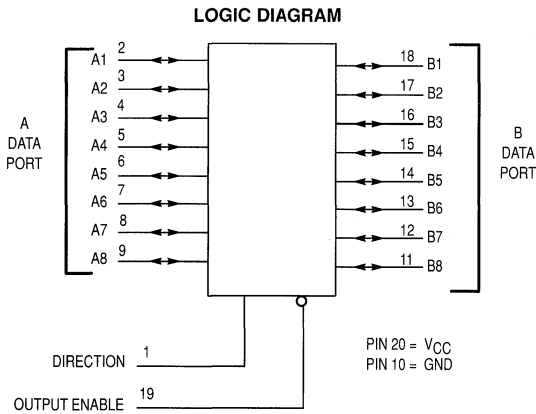


## Octal 3-State Noninverting Bus Transceiver with LSTTL Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT245A is identical in pinout to the LS245. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The MC54/74HCT245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

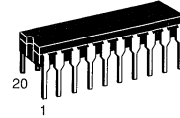
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 304 FETs or 76 Equivalent Gates



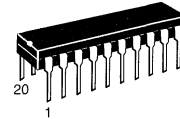
Design Criteria	Value	Unit
Internal Gate Count *	76	ea
Internal Gate Propagation Delay	1.0	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	0.005	pJ

\*Equivalent to a two-input NAND gate.

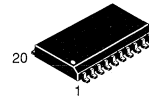
### MC54/74HCT245A



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03

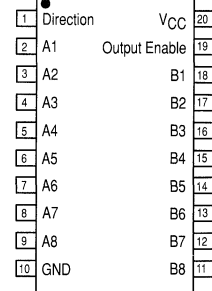


DW SUFFIX  
 SOIC  
 CASE 751D-03

#### ORDERING INFORMATION

MC74HCTXXXAN	Plastic
MC54HCTXXXAJ	Ceramic
MC74HCTXXXADW	SOIC

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

X = Don't Care

# MC54/74HCT245A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC}+0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC}+0.5$	V
$I_{in}$	DC Input Current, per Pin 1 or 19	$\pm 20$	mA
$I_{IO}$	DC Output Current, per Pin (I/O Pins)	$\pm 35$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or Plastic DIP) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating – Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS				
Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
			4.5	3.98	3.84	3.7	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
			4.5	0.26	0.33	0.4	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND, Pins 1 or 19}$	5.5	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	4.0	40	160	$\mu\text{A}$
$I_{OZ}$	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND, I/O Pins}$	5.5	$\pm 0.5$	$\pm 5.0$	$\pm 10$	$\mu\text{A}$
$\Delta I_{CC}$	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HCT245A

AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6.0 \text{ ns}$ )					
Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, A to B or B to A (Figures 1 & 3)	22	28	33	ns
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to A or B (Figures 2 & 4)	32	40	48	ns
$t_{TZL}$ , $t_{TZH}$	Maximum Propagation Delay, Output Enable to A or B (Figures 2 & 4)	30	38	45	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, any Output (Figures 1 & 3)	12	15	18	ns
$C_{in}$	Maximum Input Capacitance (Pin 1 or 19)	10	10	10	pF
$C_{out}$	Maximum Tri-State I/O Capacitance, (I/O in Hi-Impedance State)	15	15	15	pF
$C_{PD}$	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$			pF
		97			

## SWITCHING WAVEFORMS

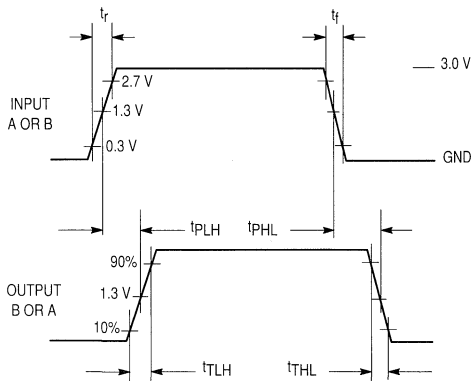


Figure 1.

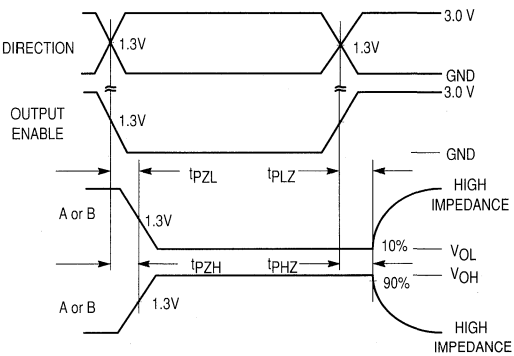
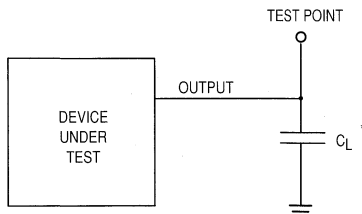
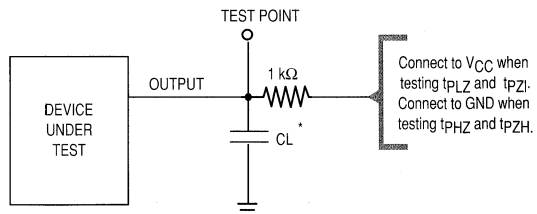


Figure 2.



\* Includes all probe and jig capacitance

Figure 3.

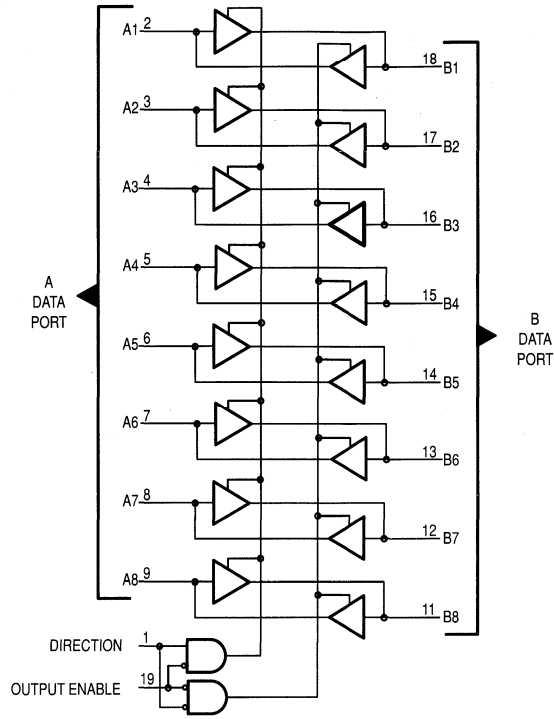


\* Includes all probe and jig capacitance

Figure 4. Test Circuit

# MC54/74HCT245A

## EXPANDED LOGIC DIAGRAM



# 8-Input Data Selector/Multiplexer with 3-State Outputs

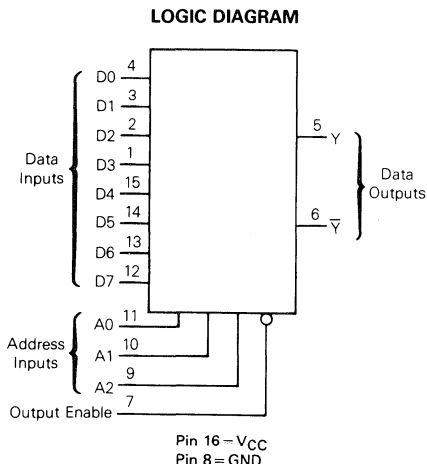
## High-Performance Silicon-Gate CMOS

The MC54/74HC251 is identical in pinout to the LS251. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

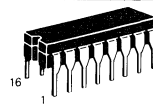
This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be a low level for the selected data to appear at the outputs. If Output Enable is high, both the Y and the  $\bar{Y}$  outputs are in the high-impedance state. This 3-state feature allows the HC251 to be used in bus-oriented systems.

The HC251 is similar in function to the HC151 which does not have 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates



### MC54/74HC251



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



**N SUFFIX  
 PLASTIC  
 CASE 648-08**



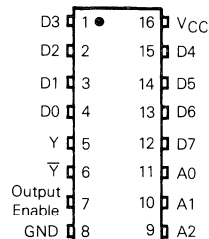
**D SUFFIX  
 SOIC  
 CASE 751B-04**

#### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs				Outputs	
A2	A1	A0	Output Enable	Y	$\bar{Y}$
X	X	X	H	Z	Z
L	L	L	L	D0	$\bar{D}0$
L	L	H	L	D1	$\bar{D}1$
L	H	L	L	D2	$\bar{D}2$
L	H	H	L	D3	$\bar{D}3$
H	L	L	L	D4	$\bar{D}4$
H	L	H	L	D5	$\bar{D}5$
H	H	L	L	D6	$\bar{D}6$
H	H	H	L	D7	$\bar{D}7$

Z = high-impedance state  
 D0, D1, . . . D7 = the level of the respective D input

# MC54/74HC251

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±25	mA
I <sub>out</sub>	DC Output Current, per Pin	±50	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	
6.0	5.48	5.34	5.20				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	
6.0	0.26	0.33	0.40				
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC251

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input D to Output Y or $\bar{Y}$ (Figures 1, 2 and 5)	2.0	185	230	280	ns
		4.5	37	46	56	
		6.0	31	39	48	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y or $\bar{Y}$ (Figures 3 and 5)	2.0	205	255	310	ns
		4.5	41	51	62	
		6.0	35	43	53	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6)	2.0	195	245	295	ns
		4.5	39	49	59	
		6.0	33	42	50	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output $\bar{Y}$ (Figures 4 and 6)	2.0	220	275	330	ns
		4.5	44	55	66	
		6.0	37	47	56	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output $\bar{Y}$ (Figures 4 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
		36			

# 5

## PIN DESCRIPTIONS

### INPUTS

D0, D1, . . . , D7 (PINS 4, 3, 2, 1, 15, 14, 13, 12) — Data inputs. Data on one of these eight binary inputs may be selected to appear on the output.

### CONTROL INPUTS

A0, A1, A2 (PINS 11, 10, 9) — Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

OUTPUT ENABLE (PIN 7) — Output Enable. This input pin must be at a low level for the selected data to appear at the outputs. If the Output Enable pin is high, both the Y and  $\bar{Y}$  outputs are taken to the high-impedance state.

### OUTPUTS

Y,  $\bar{Y}$  (PINS 5, 6) — Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ( $\bar{Y}$  output) forms.



# MC54/74HC251

## SWITCHING WAVEFORMS

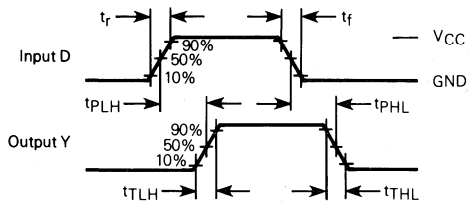


Figure 1.

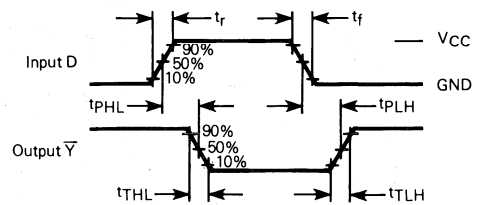


Figure 2.

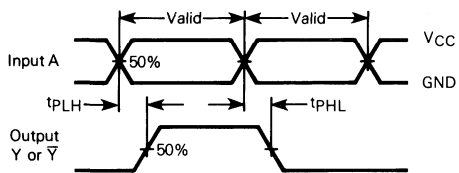


Figure 3.

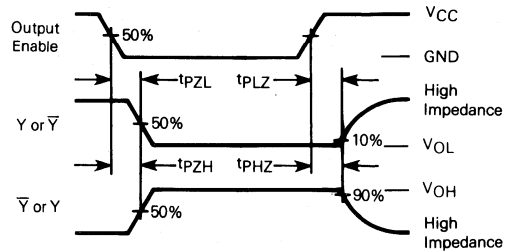
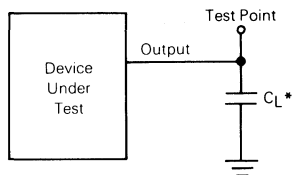


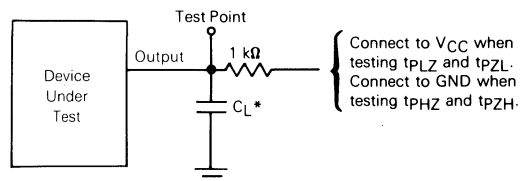
Figure 4.

### TEST CIRCUITS



\* Includes all probe and jig capacitance.

Figure 5.

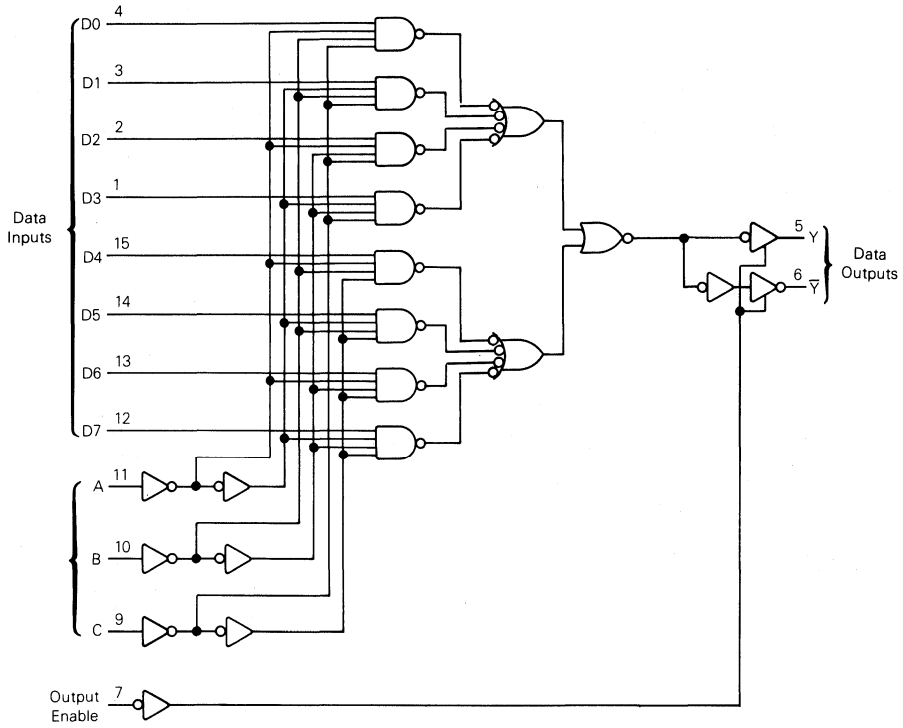


\* Includes all probe and jig capacitance.

Figure 6.

# MC54/74HC251

## EXPANDED LOGIC DIAGRAM



5

**MC54/74HC253**

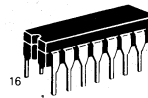
**Dual 4-Input Data Selector/  
 Multiplexer with 3-State Outputs**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC253 is identical in pinout to the LS253. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

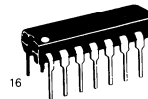
The Address inputs select one of four Data inputs from each multiplexer. Each multiplexer has an active-low Output Enable control and a three-state noninverting output.

The HC253 is similar in function to the HC153 which does not have three-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



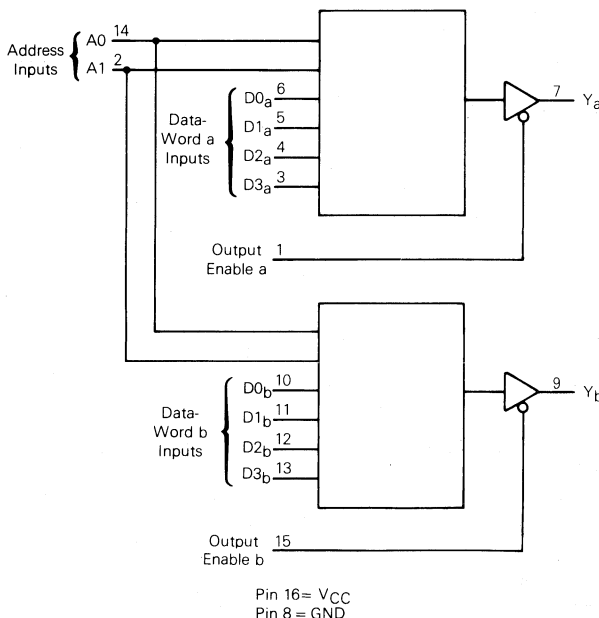
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

**ORDERING INFORMATION**

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**

Output Enable a	1	16	V <sub>CC</sub>
A1	2	15	Output Enable b
D3 <sub>a</sub>	3	14	A0
D2 <sub>a</sub>	4	13	D3 <sub>b</sub>
D1 <sub>a</sub>	5	12	D2 <sub>b</sub>
D0 <sub>a</sub>	6	11	D1 <sub>b</sub>
Y <sub>a</sub>	7	10	D0 <sub>b</sub>
GND	8	9	Y <sub>b</sub>

**5**

**FUNCTION TABLE**

Inputs			Output
A1	A0	Output Enable	Y
X	X	H	Z
L	L	L	D0
L	H	L	D1
H	L	L	D2
H	H	L	D3

D0, D1, D2, and D3 = the level of the respective Data Inputs  
 Z = high impedance

# MC54/74HC253

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	2.0	±0.1	±1.0	±1.0	μA
			4.5				
			6.0				
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	2.0	±0.5	±5.0	±10.0	μA
			4.5				
			6.0				
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	2.0	8	80	160	μA
			4.5				
			6.0				

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC253

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Data to Output Y (Figures 1 and 3)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Address to Output Y (Figures 1 and 3)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Multiplexer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		31	

## SWITCHING WAVEFORMS

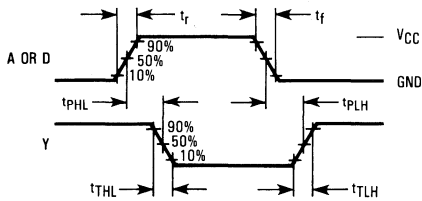


Figure 1.

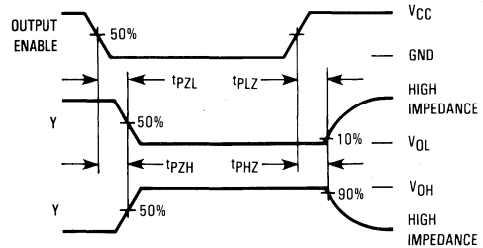
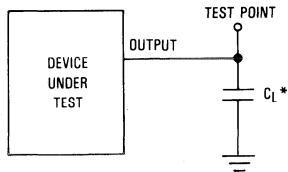


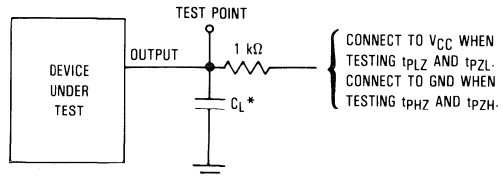
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.



\*Includes all probe and jig capacitance.

Figure 4.

# MC54/74HC253

## PIN DESCRIPTIONS

### DATA INPUTS

**D0<sub>a</sub>-D3<sub>a</sub>, D0<sub>b</sub>-D3<sub>b</sub> (PINS 3, 4, 5, 6, 10, 11, 12, 13)** — Data inputs. When one of these pairs of inputs is selected and the outputs are enabled, the outputs assume the state of the respective inputs.

### CONTROL INPUTS

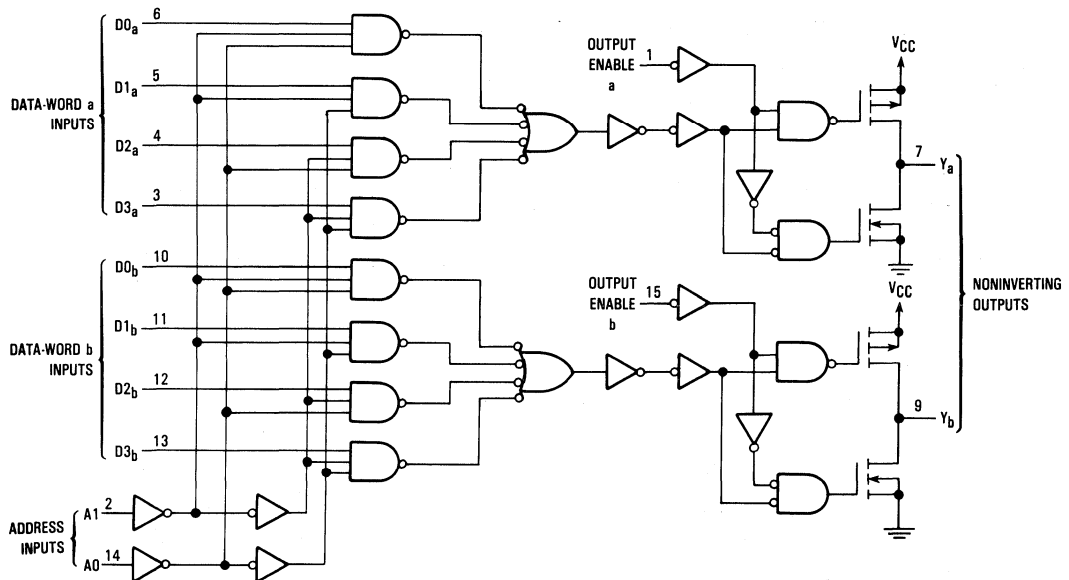
**A0, A1 (PINS 2, 14)** — Address inputs. These inputs select the pair of Data inputs to appear at the corresponding outputs.

**OUTPUT ENABLE (PINS 1, 15)** — Active-low three-state Output Enable. When a low level is applied to these inputs, the corresponding outputs are enabled. When a high level is applied, the outputs assume the high-impedance state.

### OUTPUTS

**Y<sub>a</sub>, Y<sub>b</sub> (PINS 7, 9)** — Noninverting three-state outputs.

### LOGIC DETAIL



**MC54/74HC257**

**Quad 2-Input Data Selector/  
 Multiplexer with 3-State Outputs**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC257 is identical in pinout to the LS257. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects a (4-bit) nibble from either the A or B inputs as determined by the Select input. The nibble is presented at the outputs in noninverted form when the Output Enable pin is at a low level. A high level on the Output Enable pin switches the outputs into the high-impedance state.

The HC257 is similar in function to the HC157 which do not have 3-state outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



**N SUFFIX  
 PLASTIC  
 CASE 648-08**

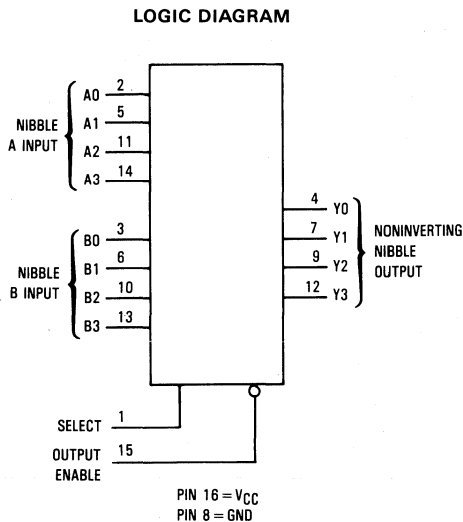


**D SUFFIX  
 SOIC  
 CASE 751B-04**

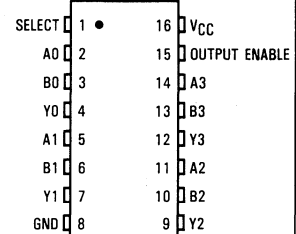
**ORDERING INFORMATION**

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs		Outputs
Output Enable	Select	Y0-Y3
H	X	Z
L	L	A0-A3
L	H	B0-B3

X = don't care  
 Z = high-impedance state  
 A0-A3, B0-B3 = the levels of the respective Nibble Inputs.

# MC54/74HC257

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HC257

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Nibble A or B to Output Y (Figures 1 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Select to Output Y (Figures 2 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		39	

## PIN DESCRIPTIONS

### INPUTS

**A0, A1, A2, A3 (PINS 2, 5, 11, 14)** — Nibble A input. The data present on these pins is transferred to the output when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

**B0, B1, B2, B3 (PINS 3, 6, 10, 13)** — Nibble B input. The logic data present on these pins is transferred to the output when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

### OUTPUTS

**Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12)** — Nibble output. The selected nibble input is presented at these outputs when the

Output Enable input is at a low level. For the Output Enable input at a high level, the outputs are switched to the high impedance state.

### CONTROL INPUTS

**SELECT (PIN 1)** — Nibble select. This input determines the nibble to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

**OUTPUT ENABLE (PIN 15)** — Output Enable. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input forces the outputs into the high-impedance state.

# MC54/74HC257

## SWITCHING WAVEFORMS

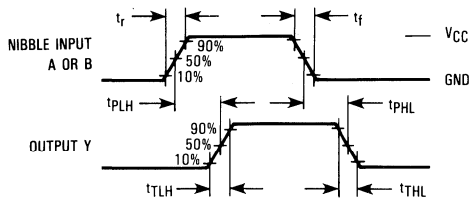


Figure 1.

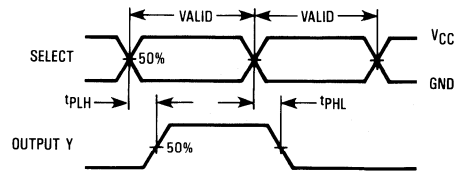


Figure 2.

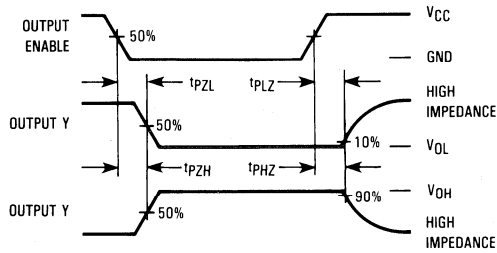
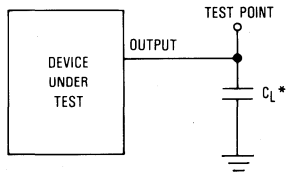


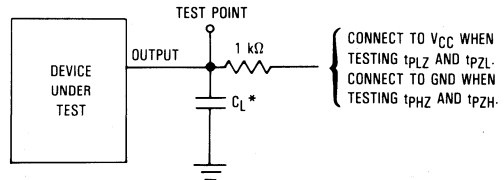
Figure 3.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 4.

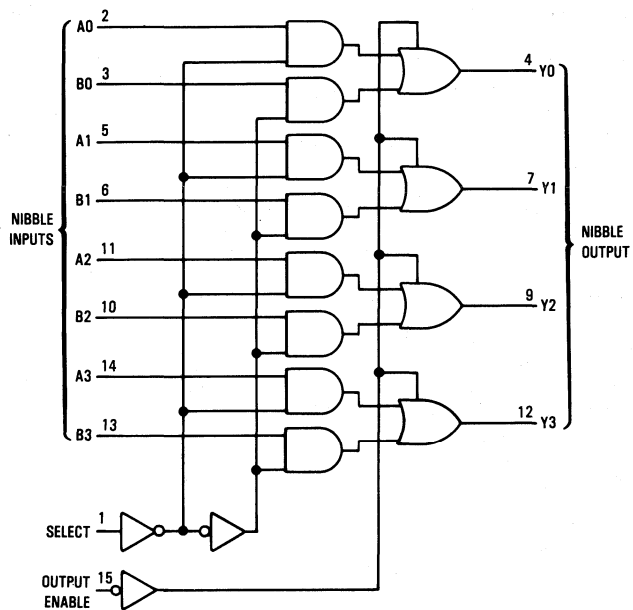


\*Includes all probe and jig capacitance.

Figure 5.

# MC54/74HC257

## EXPANDED LOGIC DIAGRAM



## 8-Bit Addressable Latch 1-of-8 Decoder

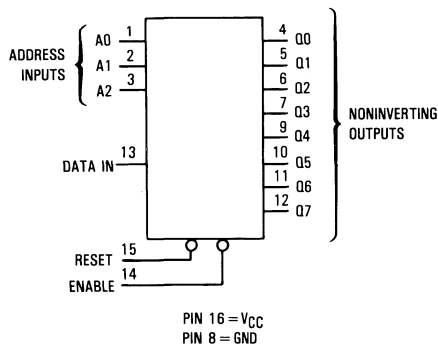
### High-Performance Silicon-Gate CMOS

The MC54/74HC259 is identical in pinout to the LS259. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

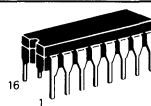
The HC259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode all outputs are LOW and unaffected by the address and data inputs. When operating the HC259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates

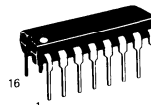
**LOGIC DIAGRAM**



## MC54/74HC259



J SUFFIX  
 CERAMIC  
 CASE 620-09



N SUFFIX  
 PLASTIC  
 CASE 648-08



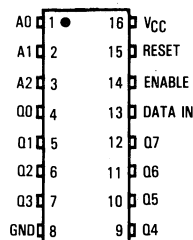
D SUFFIX  
 SOIC  
 CASE 751B-04

### ORDERING INFORMATION

MC74HCXXXN Plastic  
 MC54HCXXXJ Ceramic  
 MC74HCXXXD SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8-Line Demultiplexer
H	L	Reset

### LATCH SELECTION TABLE

Address Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

# MC54/74HC259

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC259

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Data to Output (Figures 1 and 6)	2.0	185	230	280	ns
		4.5	37	46	56	
		6.0	31	39	48	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Address Select to Output (Figures 2 and 6)	2.0	215	270	325	ns
		4.5	43	54	65	
		6.0	37	46	55	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Enable to Output (Figures 3 and 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Output (Figures 4 and 6)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		30	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Address or Data to Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Enable to Address or Data (Figure 5)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, Reset or Enable (Figure 3 or 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC259

## SWITCHING WAVEFORMS

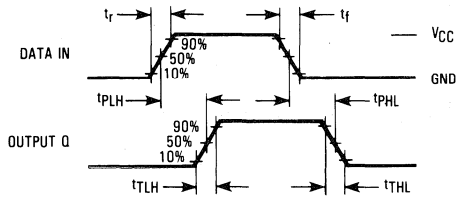


Figure 1

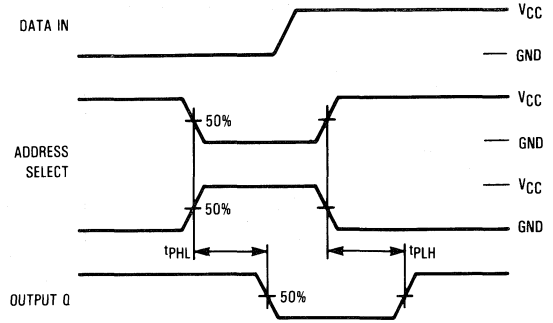


Figure 2

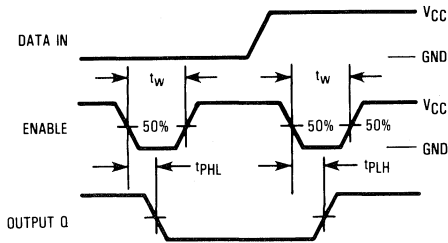


Figure 3

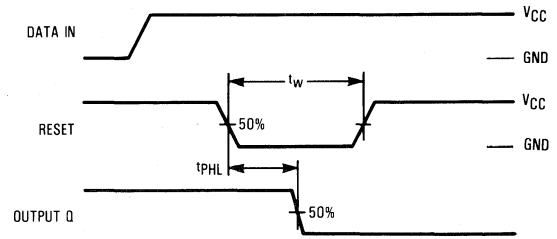


Figure 4

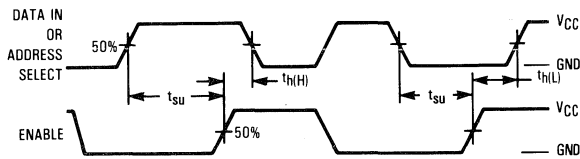
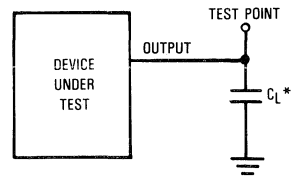


Figure 5

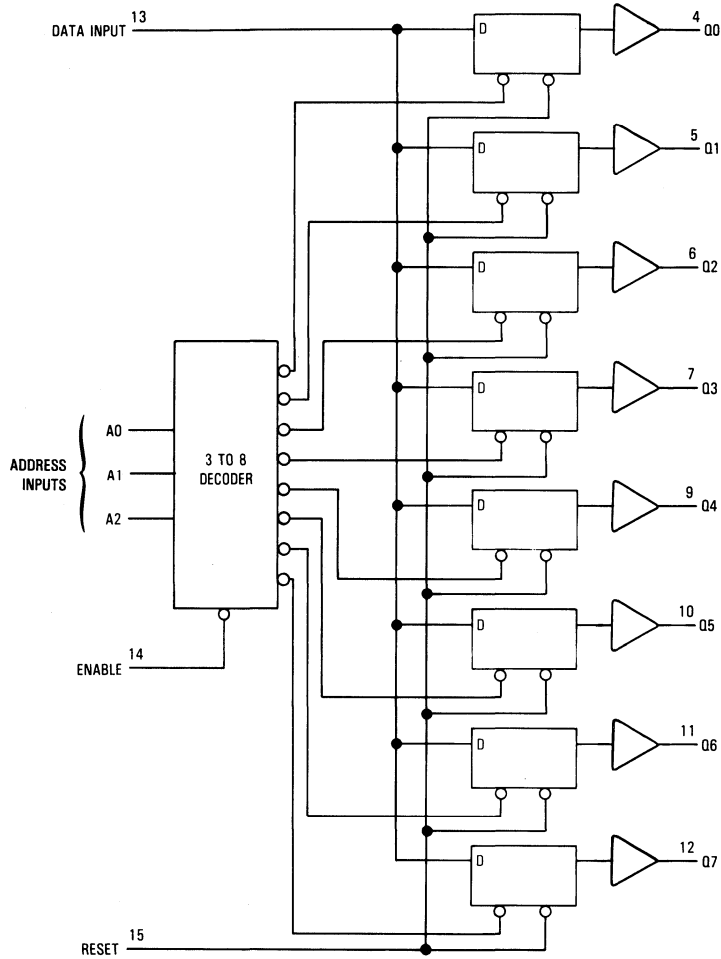


\*Includes all probe and jig capacitance.

Figure 6. Test Circuit

# MC54/74HC259

## EXPANDED LOGIC DIAGRAM



5

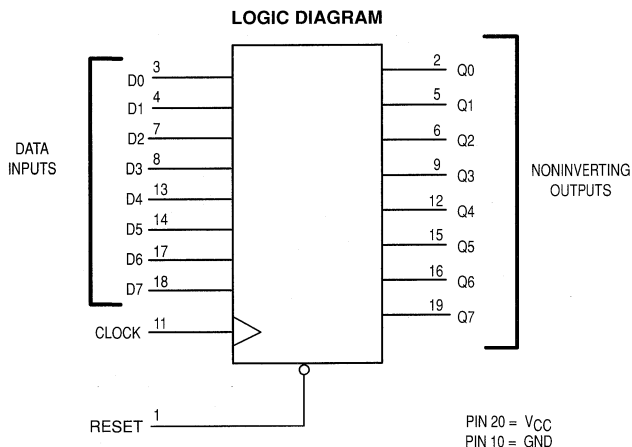


## Octal D Flip-Flop with Common Clock and Reset High-Performance Silicon-Gate CMOS

The MC54/74HC273A is identical in pinout to the LS273. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of eight D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active low.

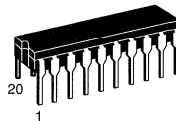
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates



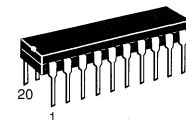
Design Criteria	Value	Unit
Internal Gate Count *	66	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	.0075	pJ

\*Equivalent to a two-input NAND gate.

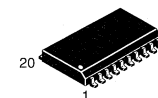
### MC54/74HC273A



**J SUFFIX  
CERAMIC  
CASE 732-03**



**N SUFFIX  
PLASTIC  
CASE 738-03**



**DW SUFFIX  
SOIC  
CASE 751D-03**

#### ORDERING INFORMATION

MC74HCXXAN	Plastic
MC54HCXXAJ	Ceramic
MC74HCXXADW	SOIC

#### PIN ASSIGNMENT

1	Reset	$V_{CC}$	20
2	Q0	Q7	19
3	D0	D7	18
4	D1	D6	17
5	Q1	Q6	16
6	Q2	Q5	15
7	D2	D5	14
8	D3	D4	13
9	Q3	Q4	12
10	GND	Clock	11

#### FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change

# MC54/74HC273A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C
		300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

†Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48		5.34	5.2			
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26		0.33	0.4			
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC273A

AC ELECTRICAL CHARACTERISTICS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)						
Symbol	Parameter	V <sub>CC</sub> Volts	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	5.0	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t <sub>TLH</sub> t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	

C <sub>in</sub>	Maximum Input Capacitance	10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
		48			

TIMING REQUIREMENTS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)										
Symbol	Parameter	Fig.	V <sub>CC</sub> Volts	Guaranteed Limit						Unit
				25°C to -55°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t <sub>su</sub>	Minimum Setup Time, Data to Clock	3	2.0	60		75		90		ns
			4.5	12		15		18		
			6.0	10		13		15		
t <sub>h</sub>	Minimum Hold Time, Clock to Data	3	2.0	3.0		3.0		3.0		ns
			4.5	3.0		3.0		3.0		
			6.0	3.0		3.0		3.0		
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock	2	2.0	5.0		5.0		5.0		ns
			4.5	5.0		5.0		5.0		
			6.0	5.0		5.0		5.0		
t <sub>w</sub>	Minimum Pulse Width, Clock	1	2.0	60		75		90		ns
			4.5	12		15		18		
			6.0	10		13		15		
t <sub>w</sub>	Minimum Pulse Width, Reset	2	2.0	60		75		90		ns
			4.5	12		15		18		
			6.0	10		13		15		
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1	2.0		1000		1000		1000	ns
			4.5		500		500		500	
			6.0		400		400		400	

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# MC54/74HC273A

## SWITCHING WAVEFORMS

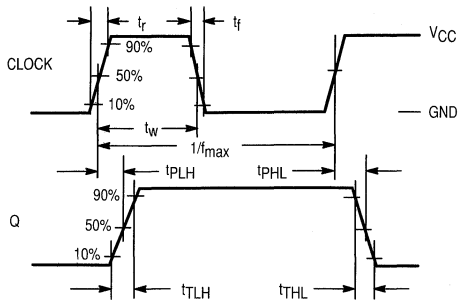


Figure 1.

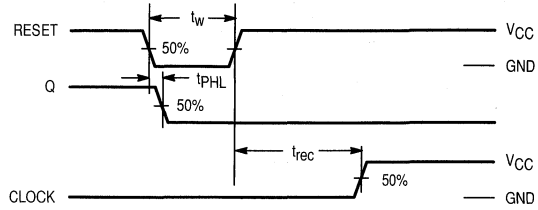


Figure 2.

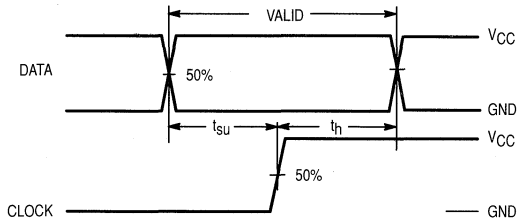
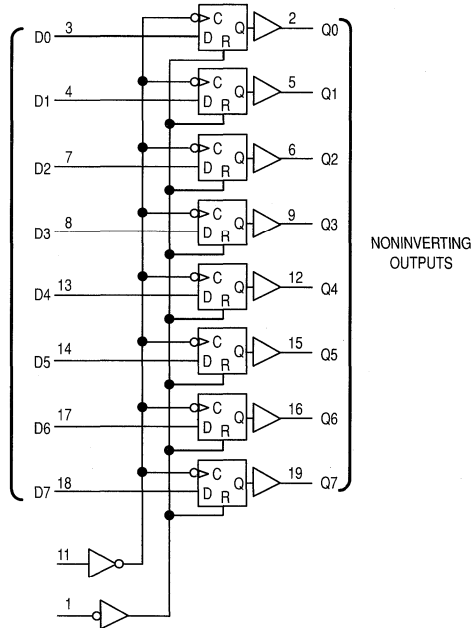


Figure 3.

## EXPANDED LOGIC DIAGRAM



5

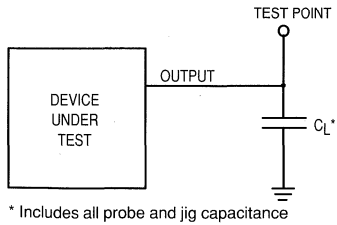


Figure 4. Test Circuit

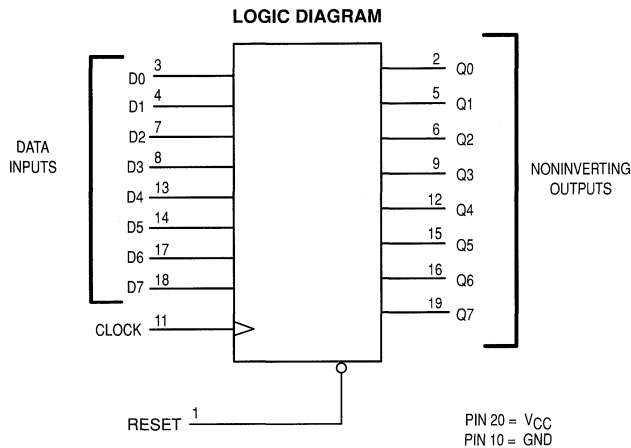
## Octal D Flip-Flop with Common Clock and Reset with LSTTL Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT273A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

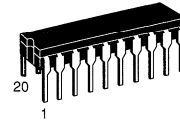
The HCT273A is identical in pinout to the LS273.

This device consists of eight D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active low.

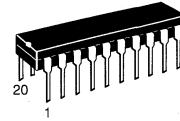
- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 284 FETs or 71 Equivalent Gates



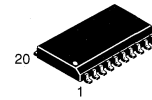
### MC54/74HCT273A



**J SUFFIX  
CERAMIC  
CASE 732-03**



**N SUFFIX  
PLASTIC  
CASE 738-03**

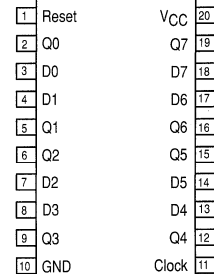


**DW SUFFIX  
SOIC  
CASE 751D-03**

**ORDERING INFORMATION**

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXADW	SOIC

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change

X = Don't Care  
Z = High Impedance

# MC54/74HCT273A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or Plastic DIP) (Ceramic DIP)	260 300	°C °C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS				
Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limits			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	3.98	3.84	3.7	V
			5.5	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	0.1	0.1	0.1	μA
			5.5	0.1	0.1	0.1	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	±0.1	±1.0	±1.0	μA
			5.5	4.0	40	160	

ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HCT273A

AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )						
Symbol	Parameter	Fig.	Guaranteed Limits			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle)	1, 4	30	24	20	MHz
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q	1, 4	25	28	35	ns
$t_{PHL}$	Maximum Propagation Delay, Reset to Q	2, 4	25	28	35	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output	1, 5	18	20	22	ns

$C_{PD}$	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$		pF
		30		

TIMING REQUIREMENTS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )									
Symbol	Parameter	Fig.	Guaranteed Limits						Unit
			25°C to -55°C		< 85°C		< 125°C		
			Min	Max	Min	Max	Min	Max	
$t_{SU}$	Minimum Setup Time, Data to Clock	3	10		12		15		ns
$t_H$	Minimum Hold Time, Clock to Data	3	3.0		3.0		3.0		ns
$t_{REC}$	Minimum Recovery Time, Set or Reset Inactive to Clock	2	5.0		5.0		5.0		ns
$t_W$	Minimum Pulse Width, Clock	1	12		15		18		ns
$t_W$	Minimum Pulse Width, Set or Reset	2	12		15		18		ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Times	1		500		500		500	ns

# MC54/74HCT273A

## SWITCHING WAVEFORMS

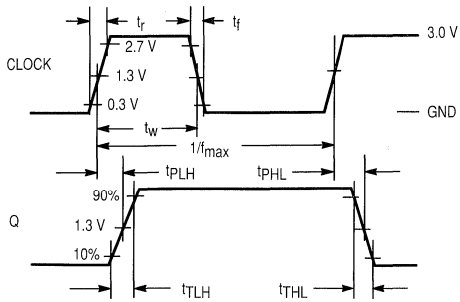


Figure 1.

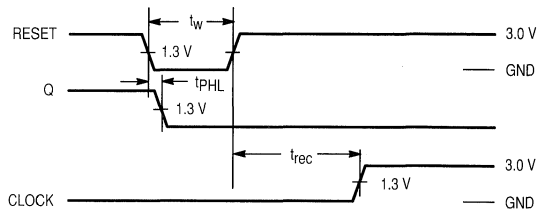


Figure 2.

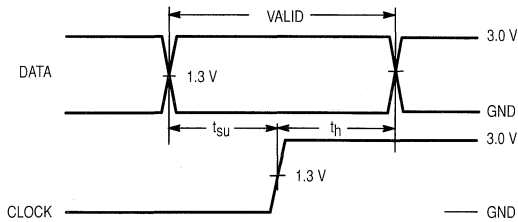
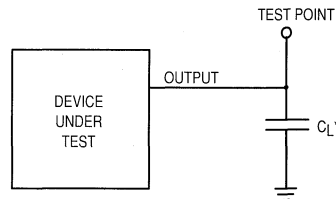


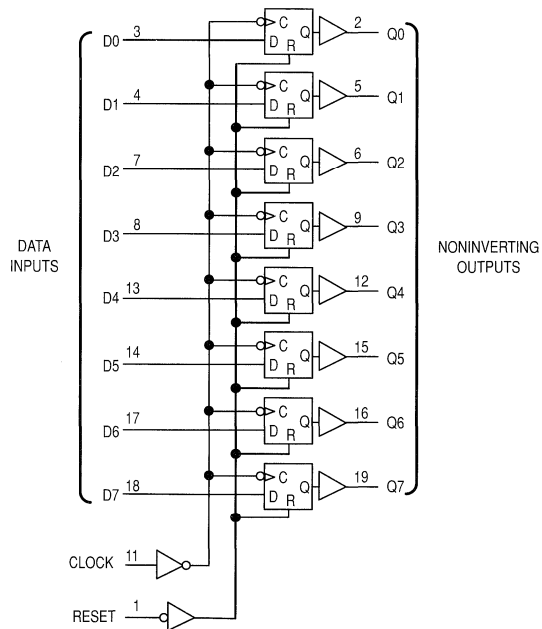
Figure 3.



\* Includes all probe and jig capacitance

Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM





# 9-Bit Odd/Even Parity Generator/Checker

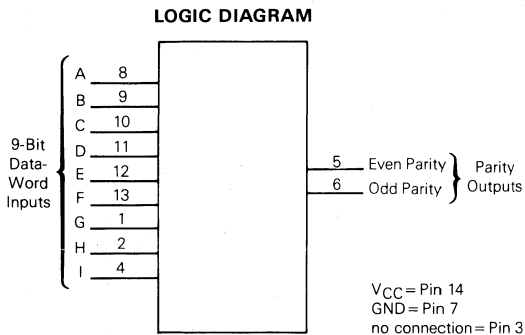
## High-Performance Silicon-Gate CMOS

The MC54/74HC280 is identical in pinout to the LS280. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

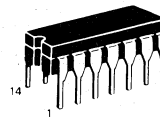
This circuit consists of 9 data-bit inputs (A through I) and 2 outputs (Even Parity and Odd Parity) to allow both odd and even parity applications. Words greater than 9-bits can be accommodated by cascading other HC280 devices.

This device can be used in systems utilizing the LS180 parity generator/checker. Although the HC280 does not have expander inputs, the corresponding function is provided by an input at pin 4 and the absence of any connection at pin 3. This permits the HC280 to be substituted for the LS180 to produce a similar function, even if the HC280s are mixed with existing LS180s. NOTE: Pullup resistors must be used on the LS180 outputs to interface with the HC280.

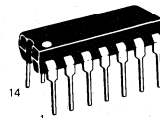
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 226 FETs or 56.5 Equivalent Gates



### MC54/74HC280



**J SUFFIX  
 CERAMIC  
 CASE 632-08**



**N SUFFIX  
 PLASTIC  
 CASE 646-06**



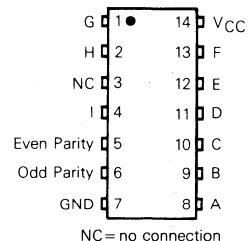
**D SUFFIX  
 SOIC  
 CASE 751A-02**

#### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Number of Inputs A through I that are high	Outputs	
	Even Parity	Odd Parity
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

# MC54/74HC280

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package‡	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC280

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Data Inputs to Parity Outputs (Figures 1 and 2)	2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		60	

## PIN DESCRIPTIONS

### INPUTS

A, B, C, D, E, F, G, H, I (Pins 8-13, 1, 2, 4) — Nine-bit data-word inputs. The data word placed on these pins is checked for even or odd parity.

### OUTPUTS

**Even Parity (Pin 5)** — Even-parity output. This pin goes high if the data word has even parity and low if the data word has odd parity.

**Odd Parity (Pin 6)** — Odd-parity output. This pin goes high if the data word has odd parity and low if the data word has even parity.

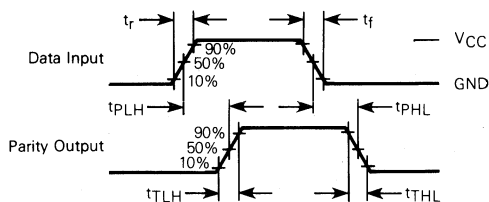
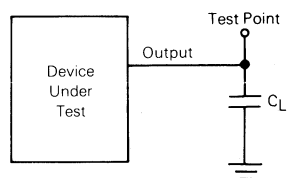


Figure 1. Switching Waveforms

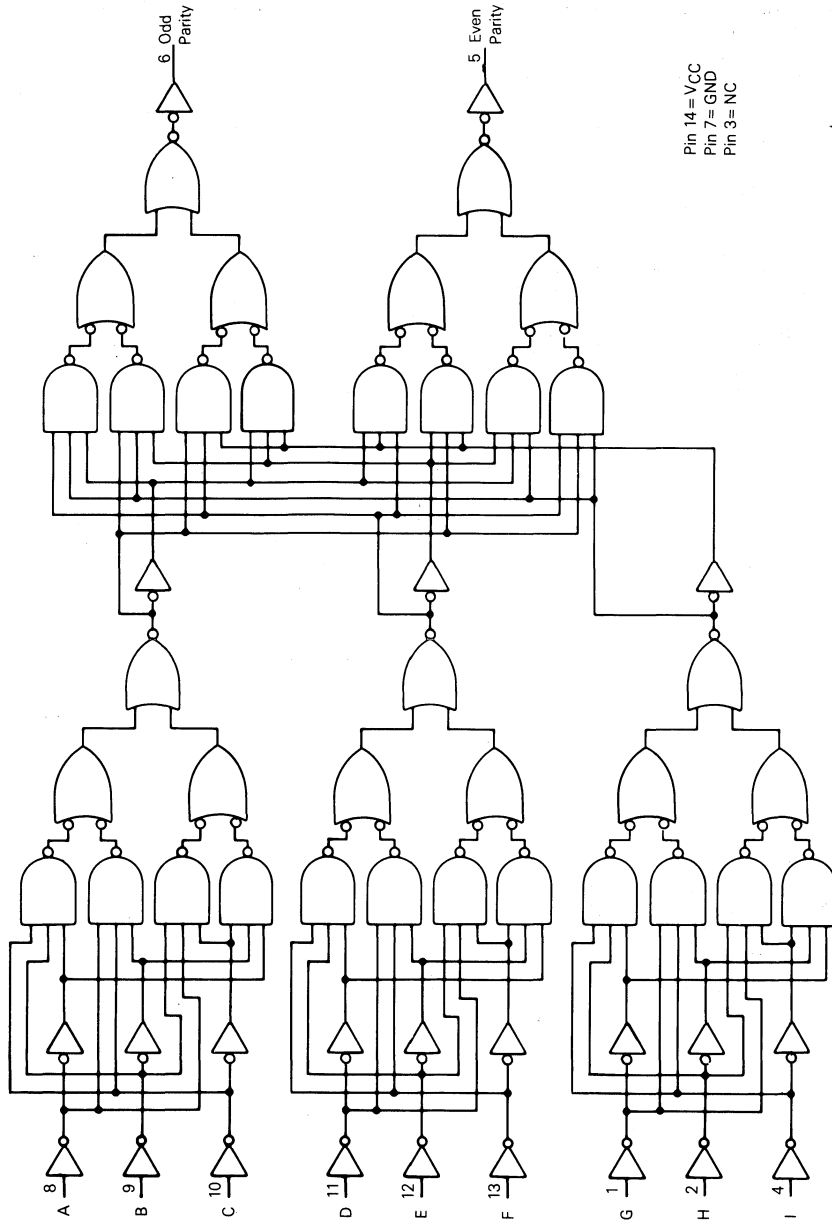


\* Includes all probe and jig capacitance.

Figure 2. Test Circuit

# MC54/74HC280

EXPANDED LOGIC DIAGRAM

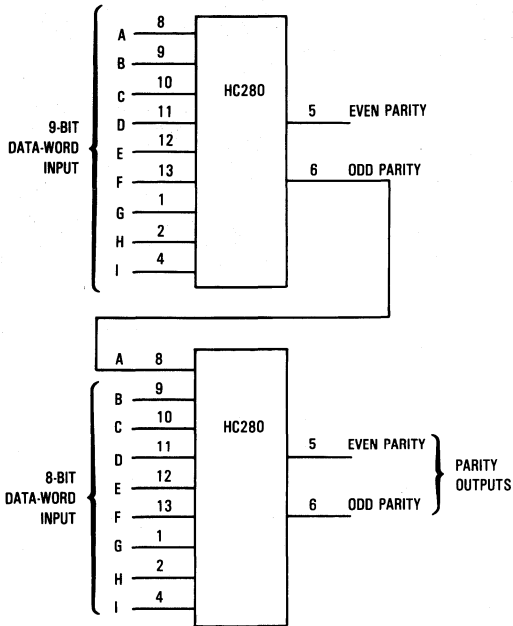


5

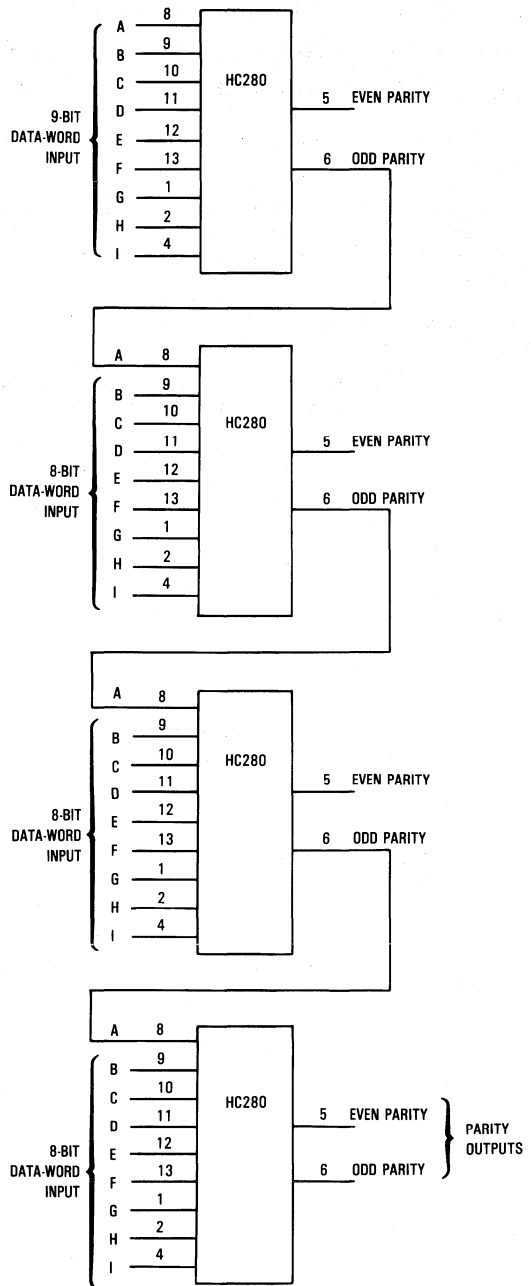
# MC54/74HC280

## TYPICAL APPLICATIONS

**CASCADED 17-BIT ODD/EVEN PARITY GENERATOR/CHECKER**



**CASCADED 33-BIT ODD/EVEN PARITY GENERATOR/CHECKER**



5

## 8-Bit Bidirectional Universal Shift Register with Parallel I/O High-Performance Silicon-Gate CMOS

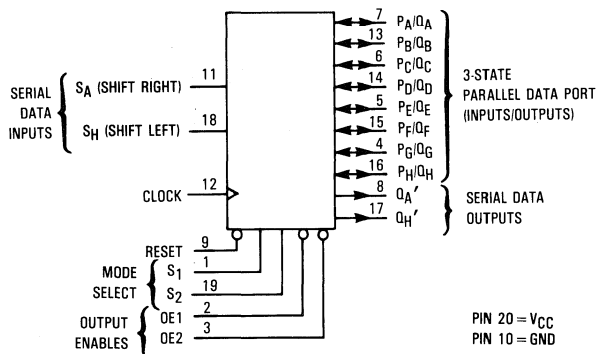
The MC54/74HC299 is identical in pinout to the LS299. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC299 features a multiplexed parallel input/output data port to achieve full 8-bit handling in a 20 pin package. Due to the large output drive capability and the 3-state feature, this device is ideally suited for interface with bus lines in a bus-oriented system.

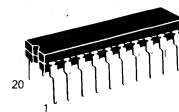
Two Mode-Select inputs and two Output Enable inputs are used to choose the mode of operation as listed in the Function Table. Synchronous parallel loading is accomplished by taking both Mode-Select lines, S<sub>1</sub> and S<sub>2</sub>, high. This places the outputs in the high-impedance state, which permits data applied to the data port to be clocked into the register. Reading out of the register can be accomplished when the outputs are enabled. The active-low asynchronous Reset overrides all other inputs.

- Output Drive Capability: 15 LSTTL Loads for Q<sub>A</sub> through Q<sub>H</sub>  
 10 LSTTL Loads for Q<sub>A</sub>' and Q<sub>H</sub>'
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates

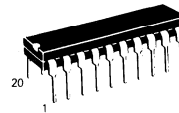
LOGIC DIAGRAM



### MC54/74HC299



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03



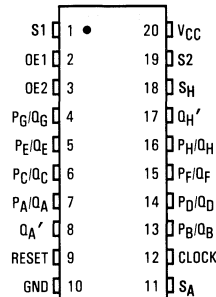
DW SUFFIX  
 SOIC  
 CASE 751D-03

#### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



# MC54/74HC299

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA (P/Q)  I <sub>out</sub>   ≤ 7.8 mA (P/Q)	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA (Q')  I <sub>out</sub>   ≤ 5.2 mA (Q')	4.5	3.98	3.84	
6.0	5.48	5.34		5.20			
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA		2.0	0.1	0.1	0.1
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA (P/Q)  I <sub>out</sub>   ≤ 7.8 mA (P/Q)	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA (Q')  I <sub>out</sub>   ≤ 5.2 mA (Q')	4.5	0.26	0.33	0.40
6.0	0.26	0.33		0.40			
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND		6.0	±0.1	±1.0	±1.0
I <sub>OZ</sub>	Maximum Three-State Leakage Current (Q <sub>A</sub> thru Q <sub>H</sub> )	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC299

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0	5.0	4.0	3.4	MHz
		4.5	25	20	17	
		6.0	29	24	20	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q <sub>A</sub> ' or Q <sub>H</sub> ' (Figures 1 and 5)	2.0	170	215	255	ns
		4.5	34	43	51	
		6.0	29	37	43	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q <sub>A</sub> thru Q <sub>H</sub> (Figures 1 and 5)	2.0	160	200	240	ns
		4.5	32	40	48	
		6.0	27	34	41	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q <sub>A</sub> ' or Q <sub>H</sub> ' (Figures 2 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q <sub>A</sub> thru Q <sub>H</sub> (Figures 2 and 5)	2.0	190	240	285	ns
		4.5	38	48	57	
		6.0	32	41	48	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, OE1, OE2, S1, or S2 to Q <sub>A</sub> thru Q <sub>H</sub> (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, OE1, OE2, S1, or S2 to Q <sub>A</sub> thru Q <sub>H</sub> (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>T LH</sub> , t <sub>T HL</sub>	Maximum Output Transition Time, Q <sub>A</sub> thru Q <sub>H</sub> (Figures 1 and 5)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t <sub>T LH</sub> , t <sub>T HL</sub>	Maximum Output Transition Time, Q <sub>A</sub> ' or Q <sub>H</sub> ' (Figures 1 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q <sub>A</sub> thru Q <sub>H</sub>	—	15	15	15	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

5

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package), Outputs Enabled Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		240	



# MC54/74HC299

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{su}$	Minimum Setup Time, Mode Select S1 or S2 to Clock (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_{su}$	Minimum Setup Time, Data Inputs S <sub>A</sub> , S <sub>H</sub> , P <sub>A</sub> thru P <sub>H</sub> to Clock (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_h$	Minimum Hold Time, Clock to Mode Select S1 or S2 (Figure 4)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
$t_h$	Minimum Hold Time, Clock to Data Inputs, S <sub>A</sub> , S <sub>H</sub> , P <sub>A</sub> thru P <sub>H</sub> (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_w$	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC299

FUNCTION TABLE

Inputs									Response								
Mode	Reset	Mode Select		Output Enables		Clock	Serial Inputs		P <sub>A</sub> /Q <sub>A</sub>	P <sub>B</sub> /Q <sub>B</sub>	P <sub>C</sub> /Q <sub>C</sub>	P <sub>D</sub> /Q <sub>D</sub>	P <sub>E</sub> /Q <sub>E</sub>	P <sub>F</sub> /Q <sub>F</sub>	P <sub>G</sub> /Q <sub>G</sub>	P <sub>H</sub> /Q <sub>H</sub>	Q <sub>A</sub> ' Q <sub>H</sub> '
		S <sub>2</sub>	S <sub>1</sub>	OE1†	OE2†		D <sub>A</sub>	D <sub>H</sub>									
Reset	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L L
	L	H	H	X	X	X	X	X	Q <sub>A</sub> through Q <sub>H</sub> = Z								L L
Shift Right	H	L	H	H	X	↔	D	X	Shift Right: Q <sub>A</sub> through Q <sub>H</sub> = Z; D <sub>A</sub> → F <sub>A</sub> ; F <sub>A</sub> → F <sub>B</sub> ; etc.								D Q <sub>G</sub>
	H	L	H	X	H	↔	D	X	Shift Right: Q <sub>A</sub> through Q <sub>H</sub> = Z; D <sub>A</sub> → F <sub>A</sub> ; F <sub>A</sub> → F <sub>B</sub> ; etc.								D Q <sub>G</sub>
	H	H	L	L	L	↔	D	X	Shift Right: D <sub>A</sub> → F <sub>A</sub> = Q <sub>A</sub> ; F <sub>A</sub> → F <sub>B</sub> = Q <sub>B</sub> ; etc.								D Q <sub>G</sub>
Shift Left	H	H	L	H	X	↔	X	D	Shift Left: Q <sub>A</sub> through Q <sub>H</sub> = Z; D <sub>H</sub> → F <sub>H</sub> ; F <sub>H</sub> → F <sub>G</sub> ; etc.								Q <sub>B</sub> D
	H	H	L	X	H	↔	X	D	Shift Left: Q <sub>A</sub> through Q <sub>H</sub> = Z; D <sub>H</sub> → F <sub>H</sub> ; F <sub>H</sub> → F <sub>G</sub> ; etc.								Q <sub>B</sub> D
	H	H	L	L	L	↔	X	D	Shift Left: D <sub>H</sub> → F <sub>H</sub> = Q <sub>H</sub> ; F <sub>H</sub> → F <sub>G</sub> = Q <sub>G</sub> ; etc.								Q <sub>B</sub> D
Parallel Load	H	H	H	X	X	↔	X	X	Parallel Load: P <sub>N</sub> → F <sub>N</sub>								P <sub>A</sub> P <sub>H</sub>
Hold	H	L	L	H	X	X	X	X	Hold: Q <sub>A</sub> through Q <sub>H</sub> = Z; F <sub>N</sub> = F <sub>N</sub>								P <sub>A</sub> P <sub>H</sub>
	H	L	L	X	H	X	X	X	Hold: Q <sub>A</sub> through Q <sub>H</sub> = Z; F <sub>N</sub> = F <sub>N</sub>								P <sub>A</sub> P <sub>H</sub>
	H	L	L	L	L	X	X	X	Hold: Q <sub>N</sub> = Q <sub>N</sub>								P <sub>A</sub> P <sub>H</sub>

Z = high impedance

D = data on serial input

F = flip-flop (see Logic Diagram)

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

## PIN DESCRIPTIONS

### DATA INPUTS

**S<sub>A</sub> (PIN 11)** — Serial data input (Shift Right). Data on this input is shifted into the shift register on the rising edge of Clock when S<sub>2</sub> is low and S<sub>1</sub> is high (shift right mode).

**S<sub>H</sub> (PIN 18)** — Serial data input (Shift Left). Data on this input is shifted into the shift register on the rising edge of Clock when S<sub>2</sub> is high and S<sub>1</sub> is low (shift left mode).

**P<sub>A</sub> through P<sub>H</sub> (PINS 7, 13, 6, 14, 5, 15, 4, 16)** — Parallel data port inputs. Data on these pins can be parallel loaded into the shift register on the rising edge of Clock when both S<sub>1</sub> and S<sub>2</sub> are high. For any other combination of S<sub>1</sub> and S<sub>2</sub>, these pins serve as the outputs of the shift register.

### CONTROL INPUTS

**CLOCK (PIN 12)** — Clock input. A low-to-high transition on this pin shifts the data at each stage to the next stage (shift right or left mode) or loads the data at the parallel data inputs into the shift register (parallel load mode).

**OE1, OE2 (PINS 2, 3)** — Active-low output enables. When both OE1 and OE2 are low, the outputs Q<sub>A</sub> through Q<sub>H</sub> are enabled. When one or both output enables are high, the outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

**RESET (PIN 9)** — Active-low reset. A low on this pin resets all stages of the register to a low level. The reset operation is asynchronous.

**S<sub>1</sub>, S<sub>2</sub> (PINS 1, 19)** — Mode select inputs. The levels present at these pins determine the shift register's mode of operation:

S<sub>1</sub> = S<sub>2</sub> = Low. Hold.

S<sub>1</sub> = Low, S<sub>2</sub> = High. Shift left.

S<sub>1</sub> = High, S<sub>2</sub> = Low. Shift right.

S<sub>1</sub> = S<sub>2</sub> = High. Parallel load.

### OUTPUTS

**Q<sub>A</sub>' , Q<sub>H</sub>' (PINS 8, 17)** — Serial data outputs. These are the outputs of the first and last stages of the shift register, respectively. These outputs are not 3-state outputs and have standard drive capabilities.

**Q<sub>A</sub> through Q<sub>H</sub> (PINS 7, 13, 6, 14, 5, 15, 4, 16)** — Parallel data port outputs. Shifted data is present at these pins when OE1 and OE2 are low. For all other combinations of OE1 and OE2 these outputs are in the high-impedance state.

# MC54/74HC299

## SWITCHING WAVEFORMS

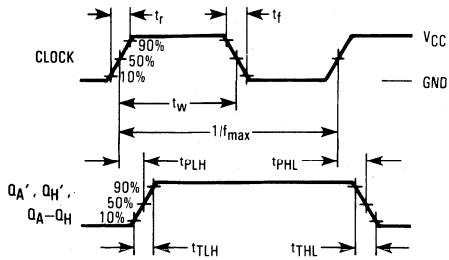


Figure 1

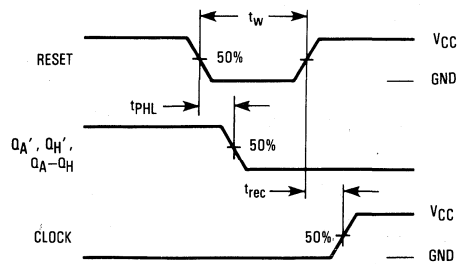


Figure 2

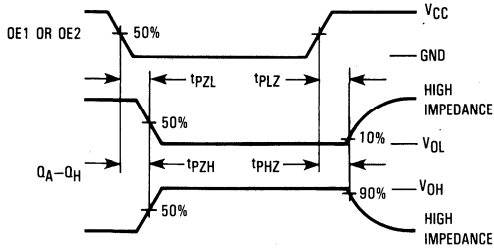


Figure 3a

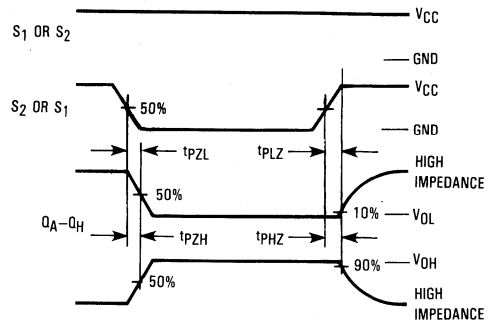


Figure 3b

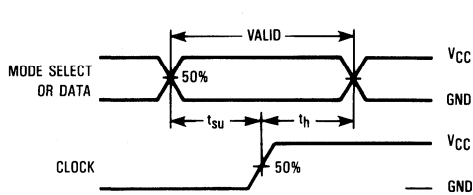
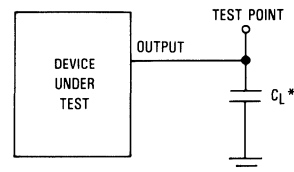
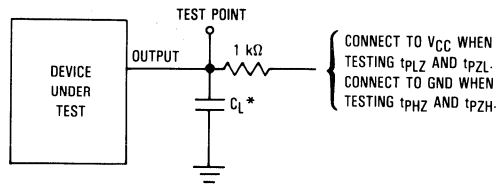


Figure 4



\*Includes all probe and jig capacitance.

Figure 5. Test Circuit

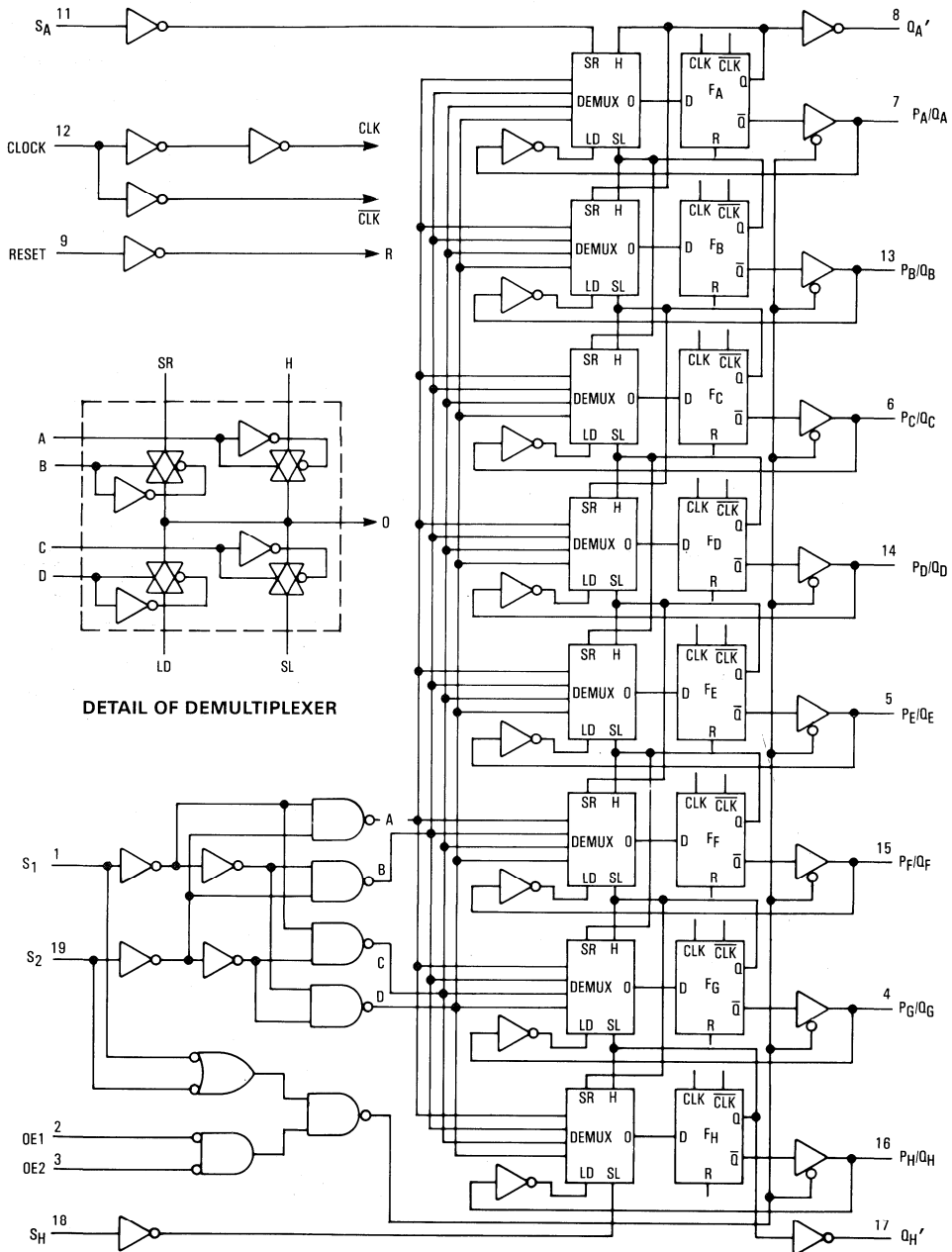


\*Includes all probe and jig capacitance.

Figure 6. Test Circuit

# MC54/74HC299

## EXPANDED LOGIC DIAGRAM



5

# Hex 3-State Noninverting Buffer with Common Enables

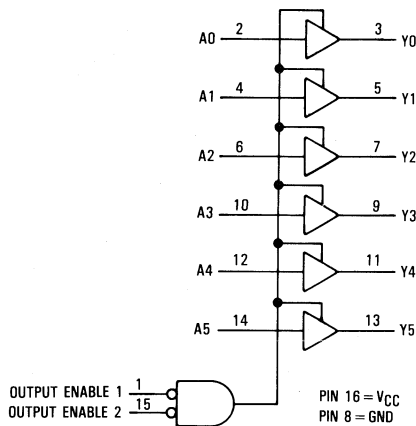
## High-Performance Silicon-Gate CMOS

The MC54/74HC365 is identical in pinout to the LS365. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC365 has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates

### LOGIC DIAGRAM



## MC54/74HC365



**J SUFFIX**  
**CERAMIC**  
 CASE 620-09



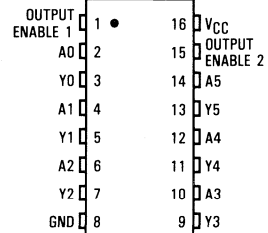
**N SUFFIX**  
**PLASTIC**  
 CASE 648-08

### ORDERING INFORMATION

MC74HCXXXN Plastic  
 MC54HCXXXJ Ceramic

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output	
Enable 1	Enable 2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

X = don't care  
 Z = high impedance

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## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	6.0	5.9	5.9	5.9	
			6.0	3.98	3.84	3.70	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC365

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	220	275	330	ns
		4.5	44	55	66	
		6.0	37	47	56	
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	220	275	330	ns
		4.5	44	55	66	
		6.0	37	47	56	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

$C_{PD}$	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		40	

## SWITCHING WAVEFORMS

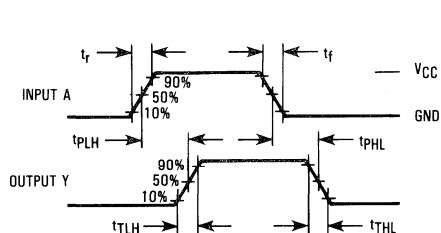


Figure 1.

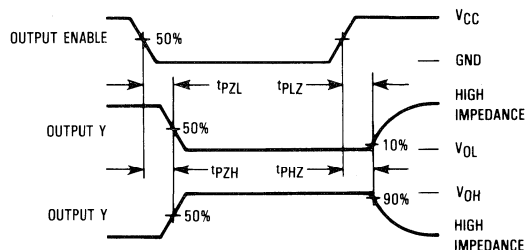
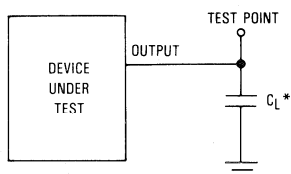


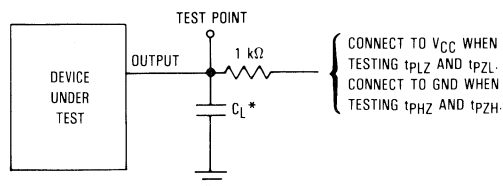
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.

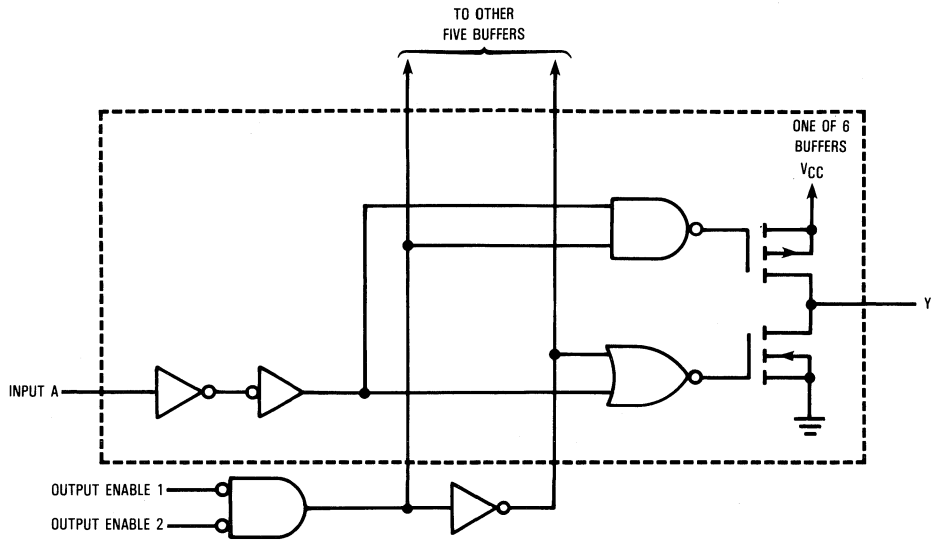


\*Includes all probe and jig capacitance.

Figure 4.

# MC54/74HC365

## LOGIC DETAIL





## Hex 3-State Inverting Buffer with Common Enables

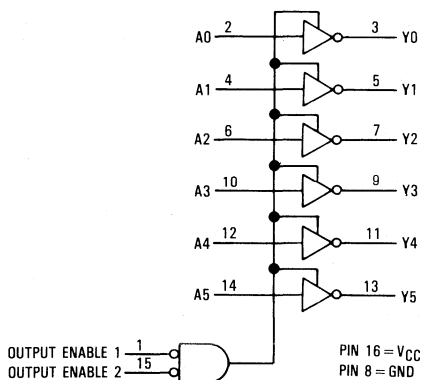
### High-Performance Silicon-Gate CMOS

The MC54/74HC366 is identical in pinout to the LS366. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

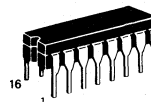
This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC366 has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 78 FETs or 19.5 Equivalent Gates

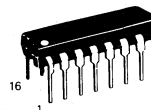
#### LOGIC DIAGRAM



## MC54/74HC366



J SUFFIX  
 CERAMIC  
 CASE 620-09



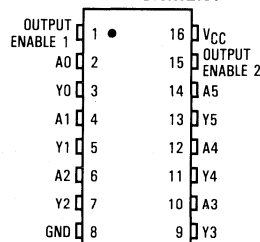
N SUFFIX  
 PLASTIC  
 CASE 648-08

#### ORDERING INFORMATION

MC74HCXXXN Plastic  
 MC54HCXXXJ Ceramic

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs			Output
Enable 1	Enable 2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

X = don't care  
 Z = high impedance

# MC54/74HC366

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260	°C
		300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	0.1	0.1	0.1	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	±0.5	±5.0	±10.0	μA
			6.0	8	80	160	
			6.0	±0.1	±1.0	±1.0	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC366

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		40	

## SWITCHING WAVEFORMS

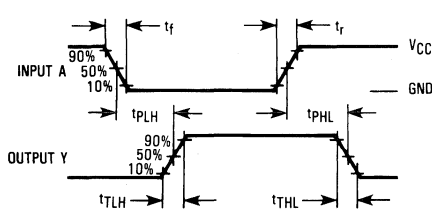


Figure 1.

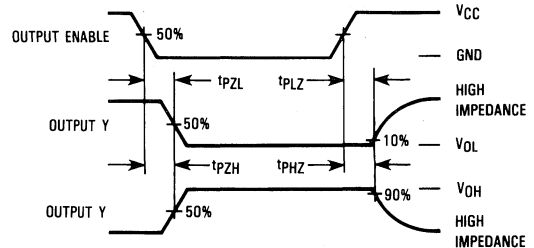
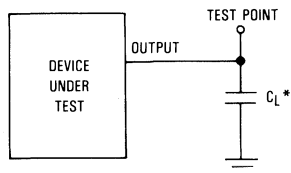


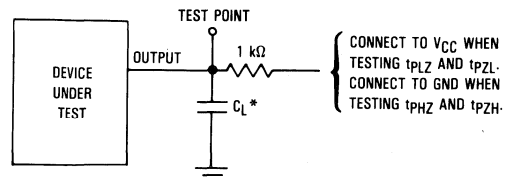
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.

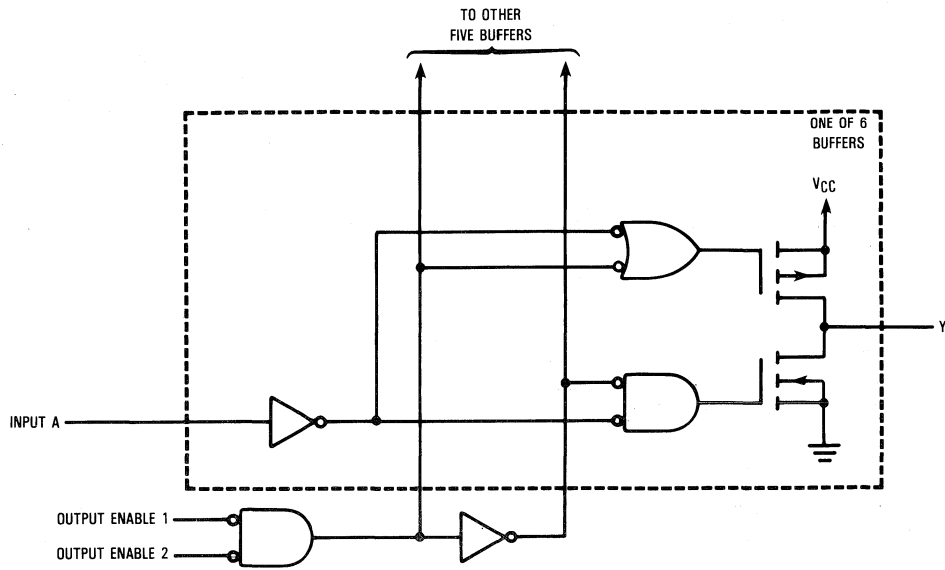


\*Includes all probe and jig capacitance.

Figure 4.

# MC54/74HC366

## LOGIC DETAIL



5

# Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections

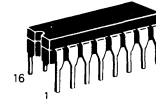
## High-Performance Silicon-Gate CMOS

The MC54/74HC367 is identical in pinout to the LS367. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs.

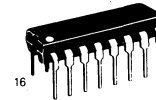
This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC367 has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates

### MC54/74HC367



**J SUFFIX**  
**CERAMIC**  
 CASE 620-09



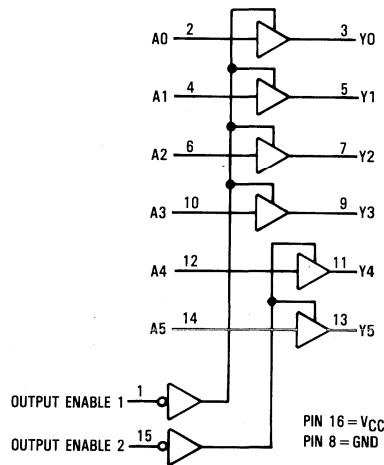
**N SUFFIX**  
**PLASTIC**  
 CASE 648-08

#### ORDERING INFORMATION

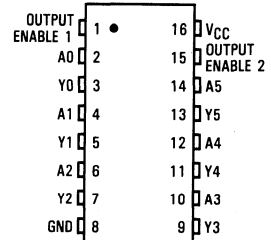
MC74HCXXXN Plastic  
 MC54HCXXXJ Ceramic

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs		Output
Enable 1, Enable 2	A	Y
L	L	L
L	H	H
H	X	Z

X = don't care  
 Z = high-impedance

# MC54/74HC367

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 35$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			4.5	3.98	3.84	3.70	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \leq 7.8 \text{ mA}$	4.5	3.98	3.84	3.70	V
			6.0	5.48	5.34	5.20	
			2.0	0.1	0.1	0.1	
			4.5	0.1	0.1	0.1	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	6.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			2.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
			6.0	±0.5	±5.0	±10.0	
$I_{OZ}$	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10.0	μA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC367

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	190	240	285	ns
		4.5	38	48	57	
		6.0	32	41	48	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0$ V	
			40

## SWITCHING WAVEFORMS

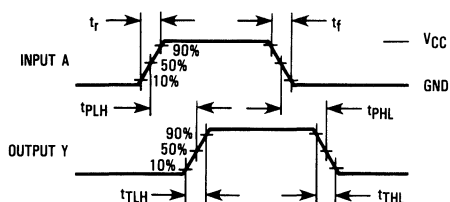


Figure 1.

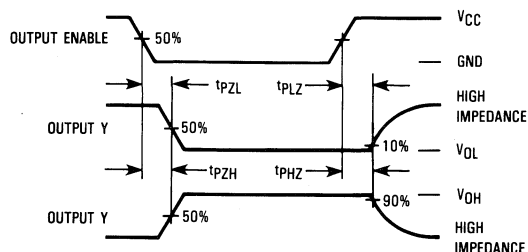
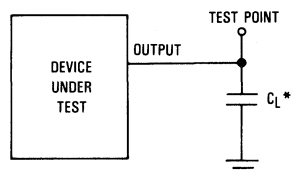


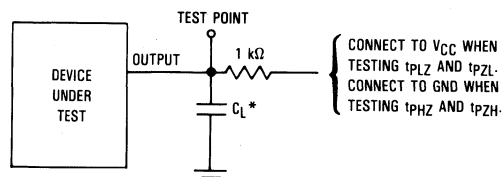
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.



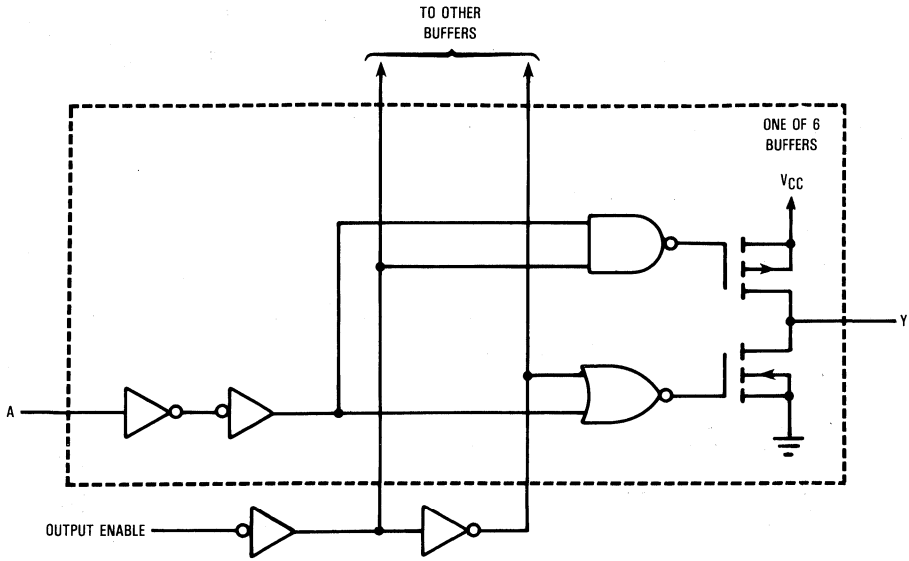
\*Includes all probe and jig capacitance.

Figure 4.

5

# MC54/74HC367

## LOGIC DETAIL



5



# Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections

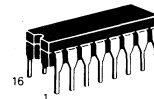
## High-Performance Silicon-Gate CMOS

The MC54/74HC368 is identical in pinout to the LS368. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs.

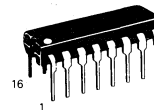
This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC368 has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 80 FETs or 20 Equivalent Gates

### MC54/74HC368



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



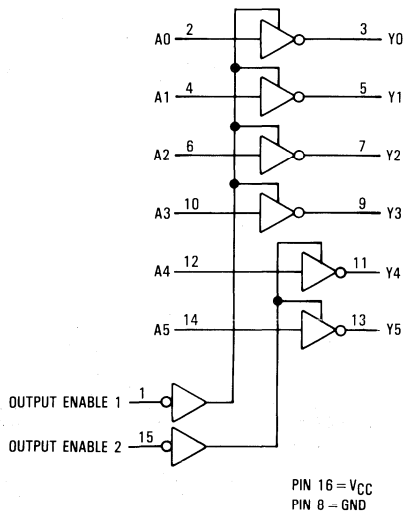
**N SUFFIX  
 PLASTIC  
 CASE 648-08**

#### ORDERING INFORMATION

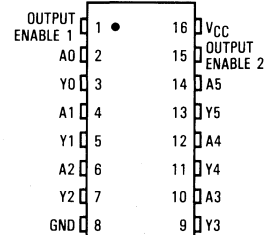
MC74HCXXXN Plastic  
 MC54HCXXXJ Ceramic

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT



**5**

#### FUNCTION TABLE

Inputs		Output
Enable 1, Enable 2	A	Y
L	L	H
L	H	L
H	X	Z

X = don't care  
 Z = high-impedance

# MC54/74HC368

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC368

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0	95	120	145	ns
		4.5	19	24	29	
		6.0	16	20	25	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	190	240	285	ns
		4.5	38	48	57	
		6.0	32	41	48	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		40	

## SWITCHING WAVEFORMS

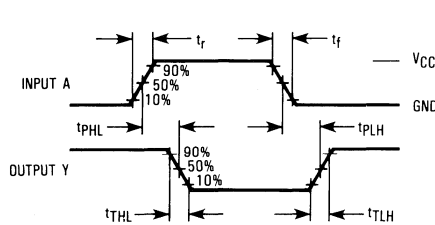


Figure 1.

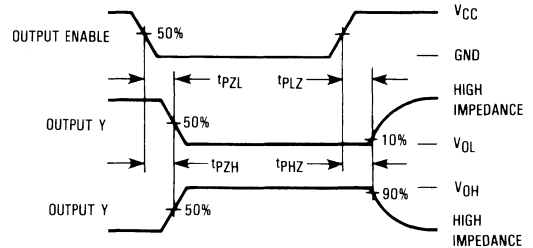
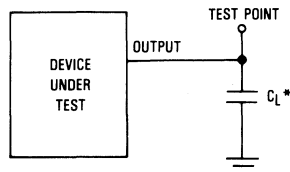


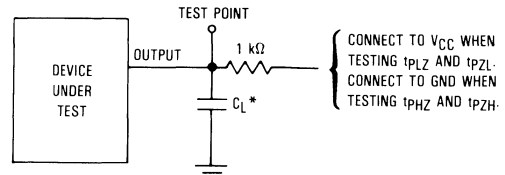
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.



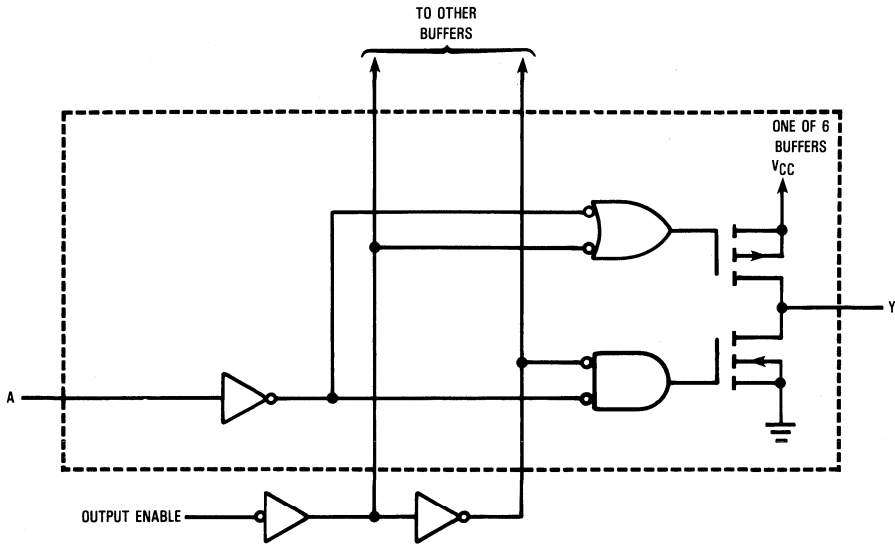
\*Includes all probe and jig capacitance.

Figure 4.

5

# MC54/74HC368

## LOGIC DETAIL



5

# Octal 3-State Non-Inverting Transparent Latch

## High-Performance Silicon-Gate CMOS

The MC54/74HC373A is identical in pinout to the LS373. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

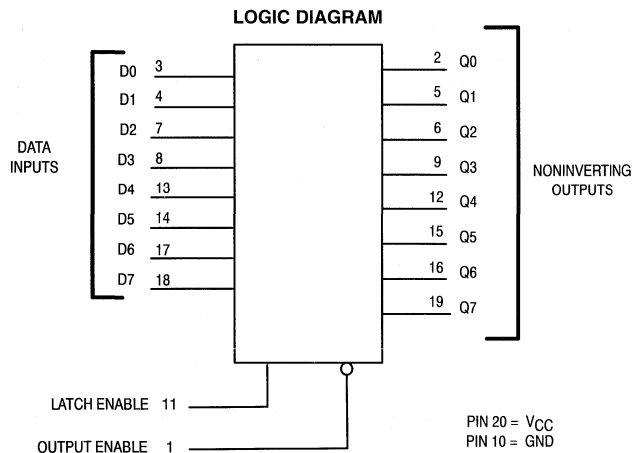
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC373A is identical in function to the HC573A which has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC373A is the non-inverting version of the HC533A.

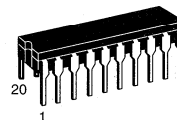
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates



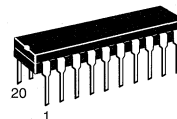
Design Criteria	Value	Unit
Internal Gate Count *	46.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	0.0075	pJ

\*Equivalent to a two-input NAND gate.

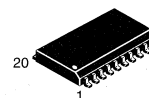
## MC54/74HC373A



**J SUFFIX**  
**CERAMIC**  
**CASE 732-03**



**N SUFFIX**  
**PLASTIC**  
**CASE 738-03**

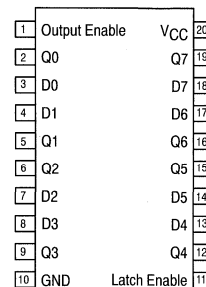


**DW SUFFIX**  
**SOIC**  
**CASE 751D-03**

### ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXADW	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care  
Z = High Impedance

# MC54/74HC373A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC) (Ceramic DIP)	260 300	°C °C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			4.5	3.98	3.84	3.7	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.4	
6.0	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	0.26	0.33	0.4			
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC373A

AC ELECTRICAL CHARACTERISTICS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)						
Symbol	Parameter	V <sub>CC</sub> (V)	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> t <sub>PHL</sub>	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t <sub>TLH</sub> t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns

C <sub>in</sub>	Maximum Input Capacitance	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
					36

TIMING REQUIREMENTS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)										
Symbol	Parameter	Fig.	V <sub>CC</sub> (V)	Guaranteed Limit						Unit
				25°C to -55°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t <sub>su</sub>	Minimum Setup Time, Input D to Latch Enable	4	2.0 4.5 6.0	25 5.0 5.0		30 6.0 6.0		40 8.0 7.0		ns
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input D	4	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t <sub>w</sub>	Minimum Pulse Width, Latch Enable	2	2.0 4.5 6.0	60 12 10		75 15 13		90 18 15		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns

5

# MC54/74HC373A

## SWITCHING WAVEFORMS

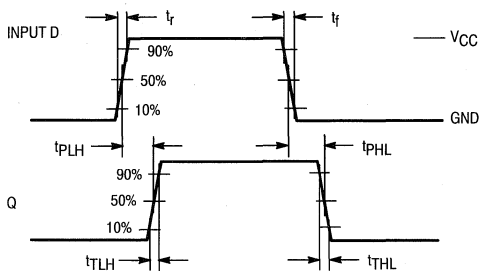


Figure 1.

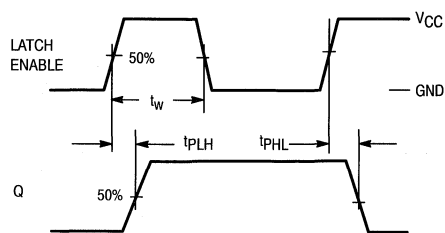


Figure 2.

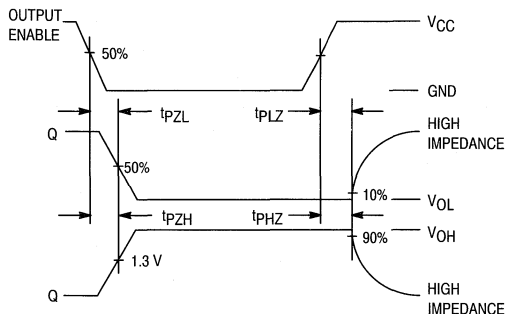


Figure 3.

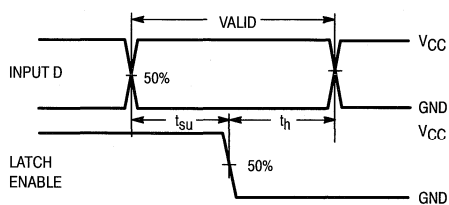
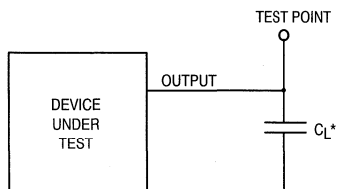


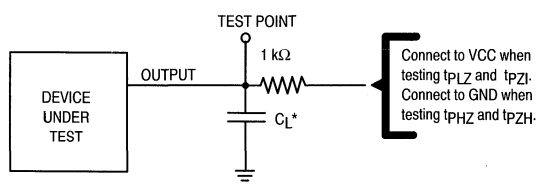
Figure 4.

## TEST CIRCUITS



\* Includes all probe and jig capacitance

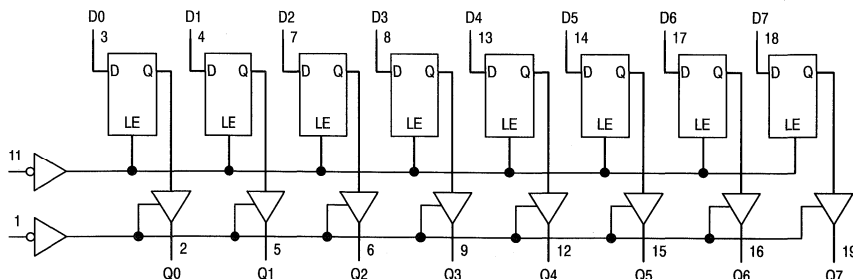
Figure 5.



\* Includes all probe and jig capacitance

Figure 6.

## EXPANDED LOGIC DIAGRAM





## Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT373A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

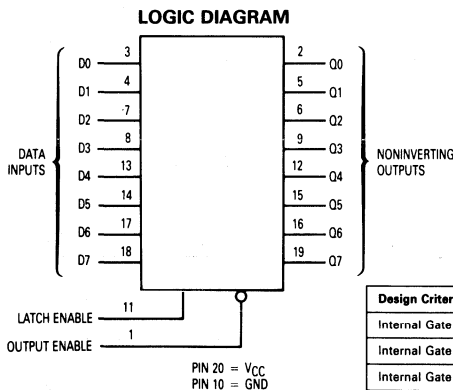
The HCT373A is identical in pinout to the LS373.

The eight latches of the HCT373A are transparent D-type latches. While the Latch Enable is high the Q outputs follow the Data Inputs. When Latch Enable is taken low, data meeting the setup and hold times becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT373A is identical in function to the HCT573A, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT533A, which has inverting outputs.

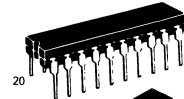
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 196 FETs or 49 Equivalent Gates



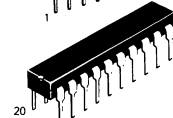
Design Criteria	Value	Units
Internal Gate Count*	49	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	.0075	pJ

\*Equivalent to a two-input NAND gate.

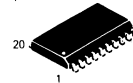
### MC54/74HCT373A



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03



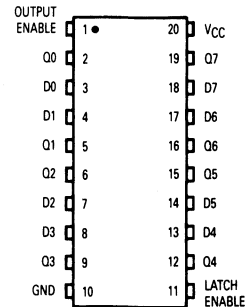
DW SUFFIX  
 SOIC  
 CASE 751D-03

#### ORDERING INFORMATION

MC74HCTXXXN Plastic  
 MC54HCTXXXJ Ceramic  
 MC74HCTXXXDW SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care  
 Z = high impedance

# MC54/74HCT373A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA	4.5	0.26	0.33	0.4	μA
			5.5	±0.1	±1.0	±1.0	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4.0	40	160	μA

ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTE 1. Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.  
 NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HCT373A

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6.0 \text{ ns}$ )

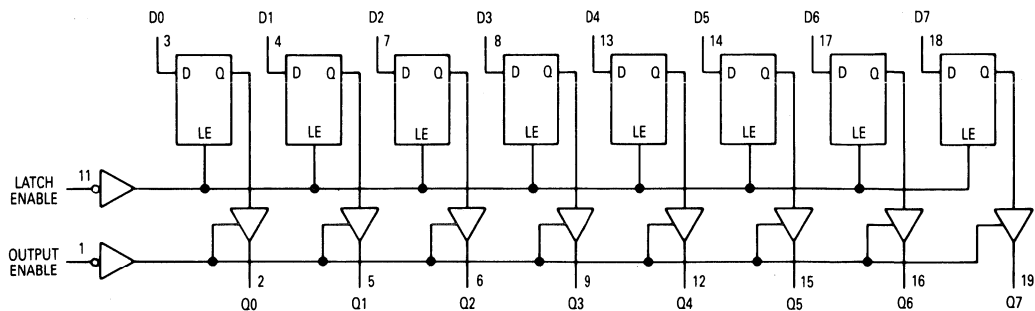
Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	28	35	42	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	32	40	48	ns
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	30	38	45	ns
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 5)	12	15	18	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

CPD	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		65	

**TIMING REQUIREMENTS** ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , Input  $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$t_{su}$	Minimum Setup Time, Input D to Latch Enable (Figure 4)	10	13	15	ns
$t_h$	Minimum Hold Time, Latch Enable to Input D (Figure 4)	10	13	15	ns
$t_w$	Minimum Pulse Width, Latch Enable (Figure 2)	12	15	18	ns
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

## EXPANDED LOGIC DIAGRAM



5

# MC54/74HCT373A

## SWITCHING WAVEFORMS

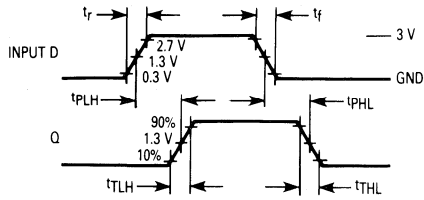


Figure 1.

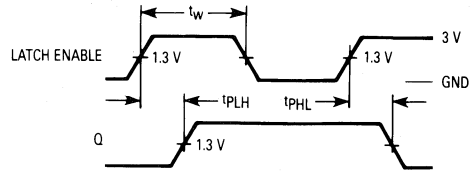


Figure 2.

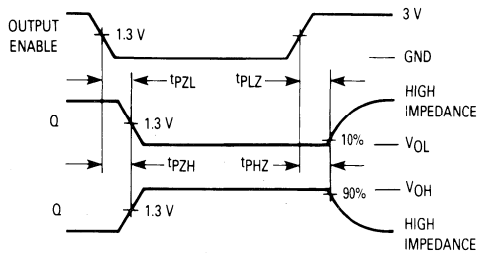


Figure 3.

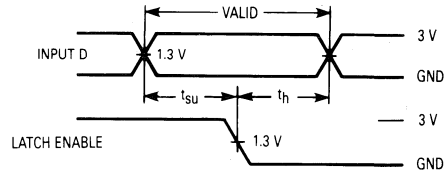
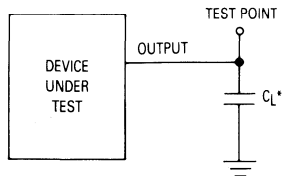


Figure 4.

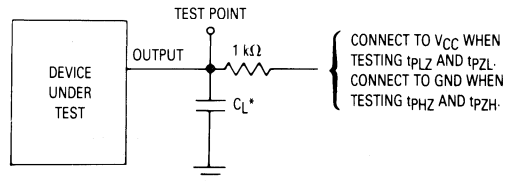
## TEST CIRCUITS

5



\*Includes all probe and jig capacitance.

Figure 5.



\*Includes all probe and jig capacitance.

Figure 6.

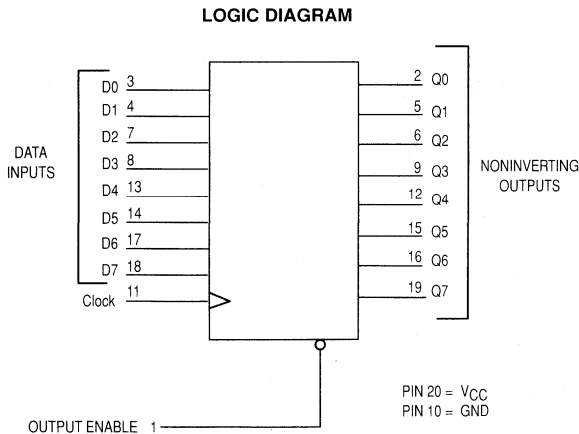
## Octal 3-State Noninverting D Flip-Flop High-Performance Silicon-Gate CMOS

The MC54/74HC374A is identical in pinout to the LS374. This device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

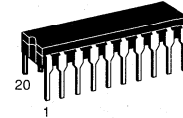
Data meeting the setup time is clocked to the outputs with the rising edge of the clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state; thus, data may be stored even when the outputs are not enabled.

The HC374A is identical in function to the HC574A which has the input pins on the opposite side of the package from the output. This device is similar in function to the HC534A which has inverting outputs.

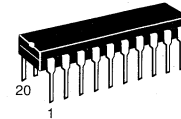
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates



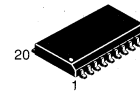
### MC54/74HC374A



**J SUFFIX  
CERAMIC  
CASE 732-03**



**N SUFFIX  
PLASTIC  
CASE 738-03**

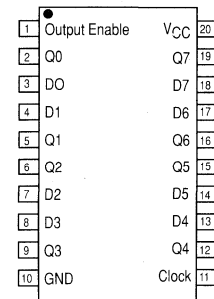


**DW SUFFIX  
SOIC  
CASE 751D-03**

#### ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXADW	SOIC

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Output Enable	Inputs		Output	
	Clock	D	Q	
L		H	H	
L		L	L	
L		X	no change	
H	X	X	Z	

X = don't care  
Z = high impedance

# MC54/74HC374A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	+75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C °C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND < (V<sub>in</sub> or V<sub>out</sub>) < V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating – Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns ns ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limits			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.50	1.50	1.50	V
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.50	0.50	0.50	V
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.90	1.90	1.90	V
			4.5	4.40	4.40	4.40	
			6.0	5.90	5.90	5.90	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.10	0.10	0.10	V
			4.5	0.10	0.10	0.10	
			6.0	0.10	0.10	0.10	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	0.26	0.33	0.40	V
			6.0	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.00	±1.00	μA
I <sub>OZ</sub>	Maximum Three State Leakage Current	Output in Hi-Impedance State V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.50	±5.00	±10.00	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> ≤ 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

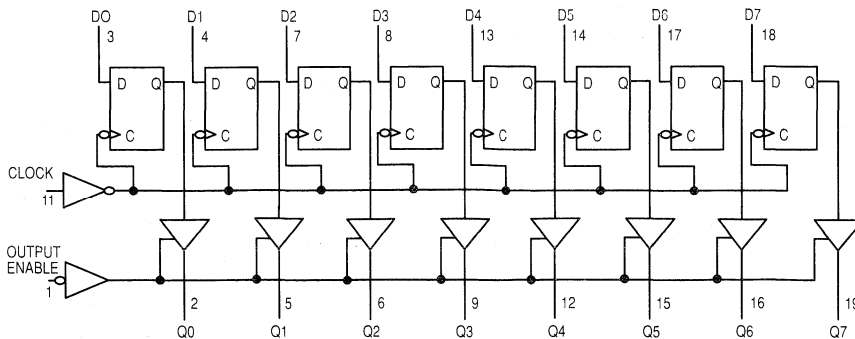
5

# MC54/74HC374A

AC ELECTRICAL CHARACTERISTICS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6 ns)							
Symbol	Parameter	Fig.	V <sub>CC</sub> Volts	Guaranteed Limits			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)	1, 4	2.0 4.5 6.0	6 30 35	5 24 28	4 20 24	MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q	1, 4	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay Time, Output Enable to Q	2, 5	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Propagation Delay, Output Enable to Q	2, 5	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, any Output	1, 4	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance			10	10	10	pF
C <sub>out</sub>	Maximum Tri-State Output Capacitance (Output in Hi-Impedance State)			15	15	15	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>			Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
				34			

TIMING REQUIREMENTS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)											
Symbol	Parameter	Fig.	V <sub>CC</sub> Volts	Guaranteed Limits						Unit	
				25°C to -55°C		≤ 85°C		≤ 125°C			
				Min	Max	Min	Max	Min	Max		
t <sub>su</sub>	Minimum Setup Time, Data to Clock	3	2.0 4.5 6.0	50 10 9		65 13 11		75 15 13		ns	
t <sub>h</sub>	Minimum Hold Time, Clock to Data	3	2.0 4.5 6.0	5 5 5		5 5 5		5 5 5		ns	
t <sub>w</sub>	Minimum Pulse Width, Clock	1	2.0 4.5 6.0	60 12 10		75 15 3		90 18 15		ns	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400		ns

## EXPANDED LOGIC DIAGRAM



# MC54/74HC374A

## SWITCHING WAVEFORMS

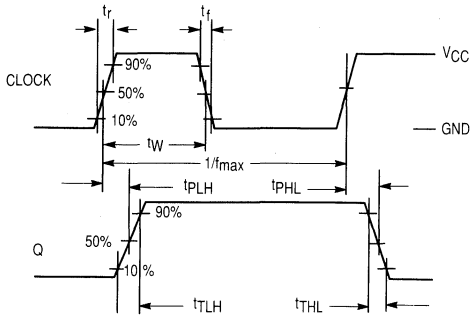


Figure 1.

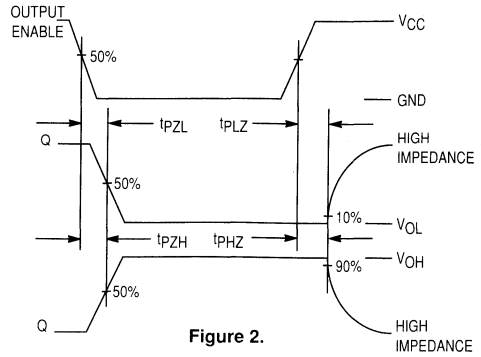


Figure 2.

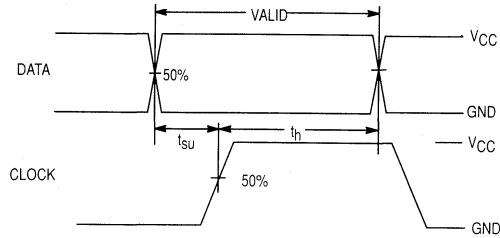
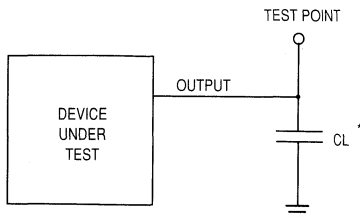


Figure 3.

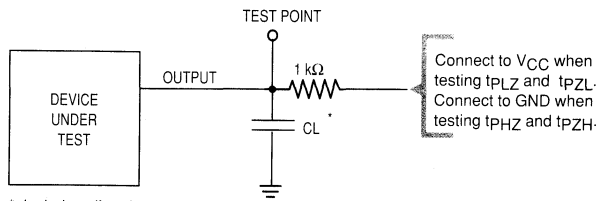
5

## TEST CIRCUITS



\* Includes all probe and jig capacitance

Figure 4.



\* Includes all probe and jig capacitance

Figure 5.



## Octal 3-State Noninverting D Flip-Flop with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT374A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

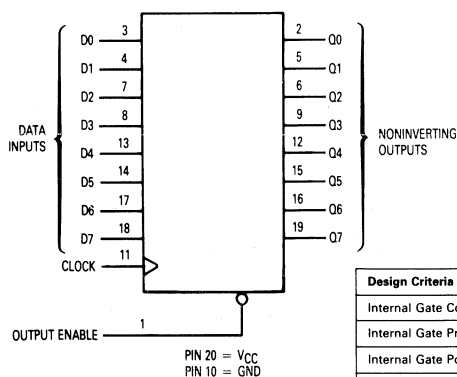
The HCT374A is identical in pinout to the LS374.

Data meeting the setup and hold time is clocked to the outputs with the rising edge of Clock. The Output Enable does not affect the state of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HCT374A is identical in function to the HCT574A, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT534A, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 276 FETs or 69 Equivalent Gates
- Improvements over HCT374
  - Improved Propagation Delays
  - 50% Lower Quiescent Power
  - Improved Input Noise and Latchup Immunity

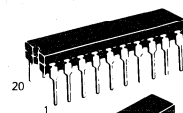
### LOGIC DIAGRAM



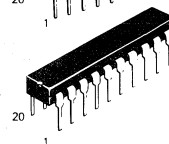
Design Criteria	Value	Units
Internal Gate Count*	69	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	.0075	pJ

\*Equivalent to a two-input NAND gate.

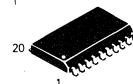
## MC54/74HCT374A



J SUFFIX  
CERAMIC  
CASE 732-03



N SUFFIX  
PLASTIC  
CASE 738-03



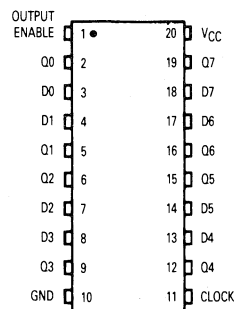
DW SUFFIX  
SOIC  
CASE 751D-03

### ORDERING INFORMATION

MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A$  = -55° to 125°C for all packages.  
Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output	
Output Enable	Clock	D	Q
L		H	H
L		L	L
L	L,H	X	no change
H	X	X	Z

X = don't care  
Z = high impedance

# MC54/74HCT374A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA	4.5	3.98	3.84	3.7	μA
			5.5	0.26	0.33	0.4	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4.0	40	160	μA

ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTE 1. Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HCT374A

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , $C_L = 50\text{ pF}$ , Input $t_r = t_f = 6.0\text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	31	39	47	ns
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	30	38	45	ns
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	30	38	45	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	12	15	18	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

$C_{PD}$	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$	pF
		65	

## TIMING REQUIREMENTS ( $V_{CC} = 5.0\text{ V} \pm 10\%$ , Input $t_r = t_f = 6.0\text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$t_{su}$	Minimum Setup Time, Data to Clock (Figure 3)	12	15	18	ns
$t_h$	Minimum Hold Time, Clock to Data (Figure 3)	5.0	5.0	5.0	ns
$t_w$	Minimum Pulse Width, Clock (Figure 1)	12	15	18	ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

# MC54/74HCT374A

## SWITCHING WAVEFORMS

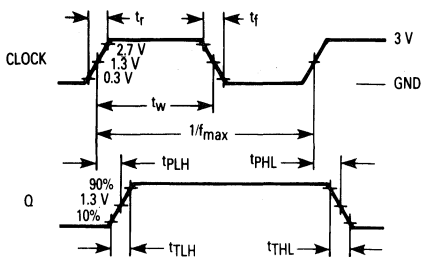


Figure 1.

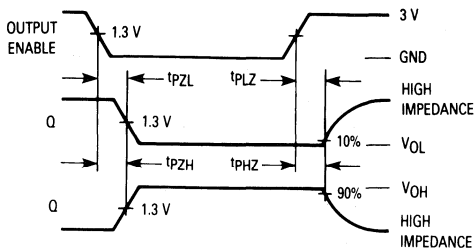


Figure 2.

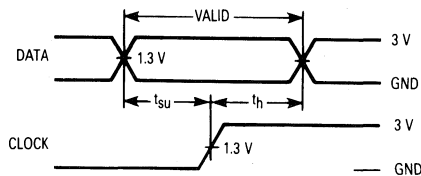
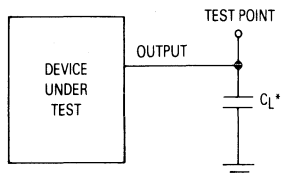


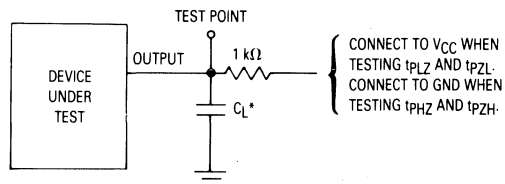
Figure 3.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

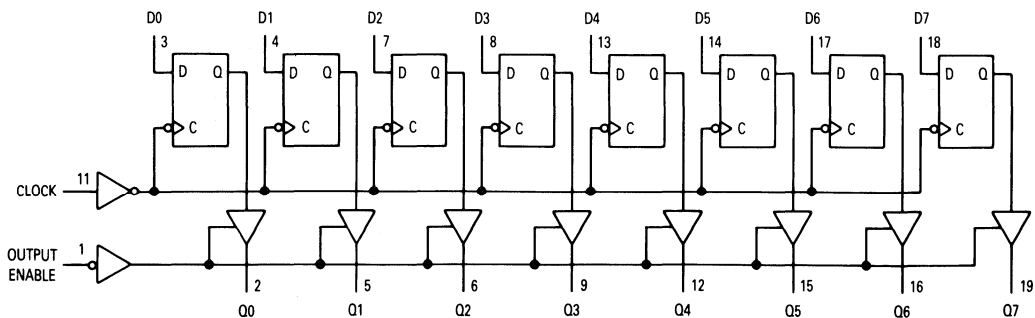
Figure 4.



\*Includes all probe and jig capacitance.

Figure 5.

## EXPANDED LOGIC DIAGRAM



# Dual 4-Stage Binary Ripple Counter with $\div 2$ and $\div 5$ Sections

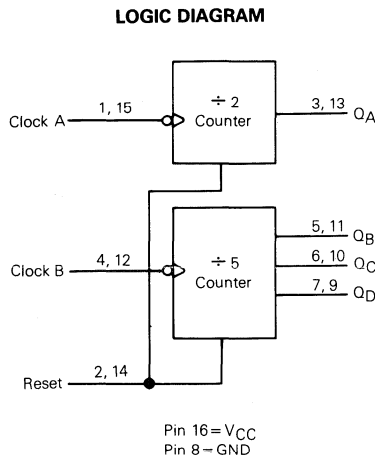
## High-Performance Silicon-Gate CMOS

The MC54/74HC390 is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

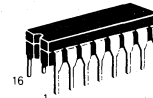
This device consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five section. The divide-by-two and divide-by-five counters have separate clock inputs, and can be cascaded to implement various combinations of  $\div 2$  and/or  $\div 5$  up to a  $\div 100$  counter.

Flip-flops internal to the counters are triggered by high-to-low transitions of the clock input. A separate, asynchronous reset is provided for each 4-bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390.

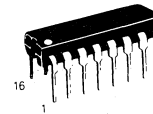
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates



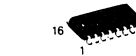
## MC54/74HC390



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



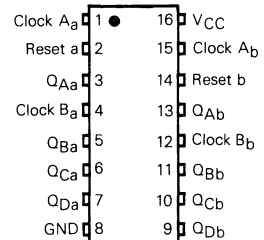
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXXD SOIC  
 MC74HCXXXN Plastic  
 MC54HCXXXJ Ceramic

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Clock A	Clock B	Reset	Action
X	X	H	Reset $\div 2$ and $\div 5$
	X	L	Increment $\div 2$
X		L	Increment $\div 5$

# MC54/74HC390

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit				
				25°C to -55°C	≤85°C	≤125°C					
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V				
			4.5	3.15	3.15	3.15					
			6.0	4.2	4.2	4.2					
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V				
			4.5	0.9	0.9	0.9					
			6.0	1.2	1.2	1.2					
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V				
			4.5	4.4	4.4	4.4					
			6.0	5.9	5.9	5.9					
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V				
			4.5	0.1	0.1	0.1					
			6.0	0.1	0.1	0.1					
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA				
			I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0		8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC390

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	5.4	4.4	3.6	MHz
		4.5	27	22	18	
		6.0	32	26	21	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock A to QA (Figures 1 and 3)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock A to QC (QA connected to Clock B) (Figures 1 and 3)	2.0	290	365	435	ns
		4.5	58	73	87	
		6.0	49	62	74	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock B to QB (Figures 1 and 3)	2.0	130	165	195	ns
		4.5	26	33	39	
		6.0	22	28	33	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock B to QC (Figures 1 and 3)	2.0	185	230	280	ns
		4.5	37	46	56	
		6.0	31	39	48	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock B to QD (Figures 1 and 3)	2.0	130	165	195	ns
		4.5	26	33	39	
		6.0	22	28	33	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Counter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock A or Clock B (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t <sub>w</sub>	Minimum Pulse Width, Clock A, Clock B (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC390

## PIN DESCRIPTIONS

### INPUTS

**CLOCK A (PINS 1, 15) and CLOCK B (PINS 4, 15)** — Clock A is the clock input to the ÷ 2 counter; Clock B is the clock input to the ÷ 5 counter. The internal flip-flops are toggled by high-to-low transitions of the clock input.

### CONTROL INPUTS

**RESET (PINS 2, 14)** — Asynchronous reset. A high at the Reset input prevents counting, resets the internal flip-flops, and forces  $Q_A$  through  $Q_D$  low.

### OUTPUTS

**$Q_A$  (PINS 3, 13)** — Output of the ÷ 2 counter.

**$Q_B, Q_C, Q_D$  (PINS 5, 6, 7, 9, 10, 11)** — Outputs of the ÷ 5 counter.  $Q_D$  is the most significant bit.  $Q_A$  is the least significant bit when the counter is connected for BCD output as in Figure 4.  $Q_B$  is the least significant bit when the counter is operating in the bi-quinary mode as in Figure 5.

## SWITCHING WAVEFORMS

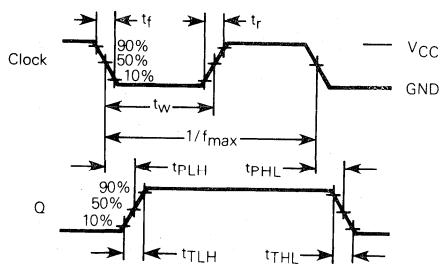


Figure 1.

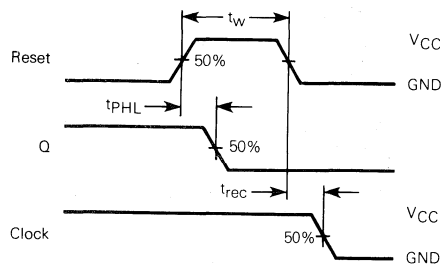
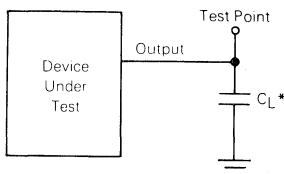


Figure 2.

## TEST CIRCUIT



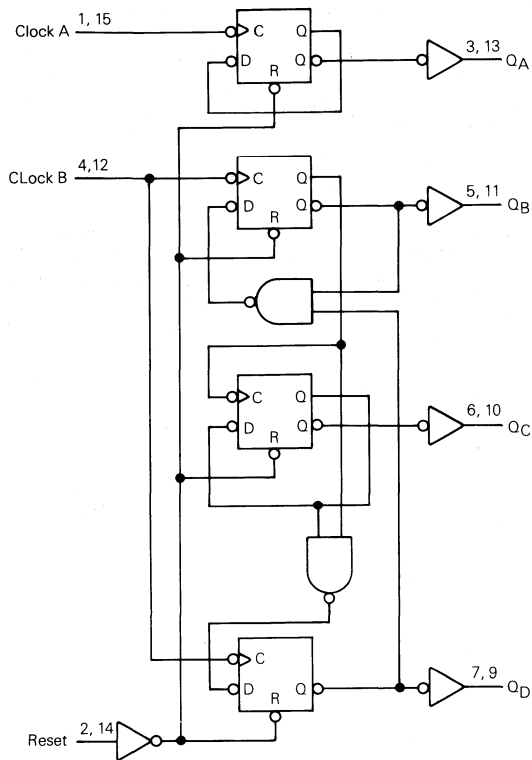
\*Includes all probe and jig capacitance.

Figure 3.

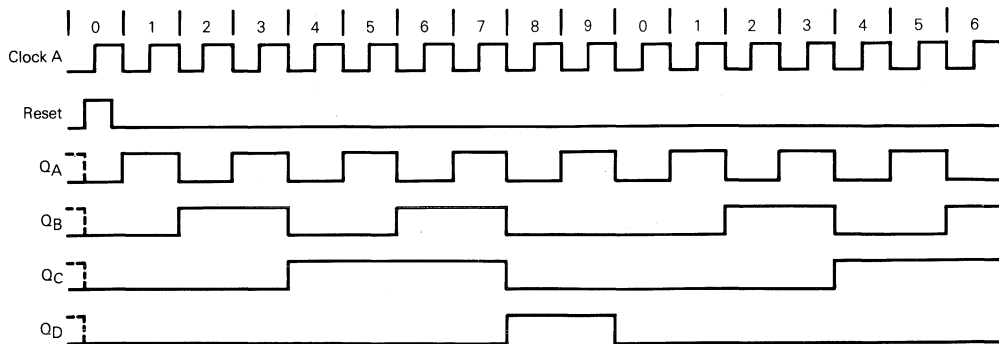


# MC54/74HC390

## EXPANDED LOGIC DIAGRAM



**TIMING DIAGRAM**  
(Q<sub>A</sub> Connected to Clock B)



# MC54/74HC390

## APPLICATIONS INFORMATION

Each half of the MC54/74HC390 has independent  $\div 2$  and  $\div 5$  sections (except for the Reset function). The  $\div 2$  and  $\div 5$  counters can be connected to give BCD or bi-quinary (2-5) count sequences. If output  $Q_A$  is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The function table for the BCD count sequence is given in Table 1.

To obtain a bi-quinary count sequence, the input signal is connected to the Clock B input, and output  $Q_D$  is connected to the Clock A input (Figure 5).  $Q_A$  provides a 50% duty cycle output. The bi-quinary count sequence function table is given in Table 2.

**Table 1.**  
**BCD Count Sequence\***

Count	Output			
	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

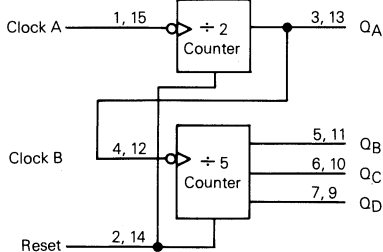
\* $Q_A$  connected to Clock B input.

**Table 2.**  
**Bi-Quinary Count Sequence\*\***

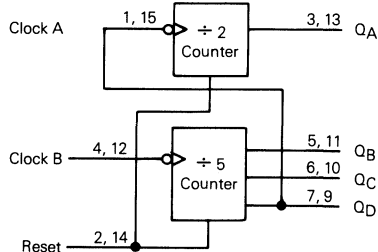
Count	Output			
	$Q_A$	$Q_D$	$Q_C$	$Q_B$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L

\*\* $Q_D$  connected to Clock A input.

## CONNECTION DIAGRAMS



**Figure 4. BCD Count**



**Figure 5. Bi-Quinary Count**

5

## Dual 4-Stage Binary Ripple Counter

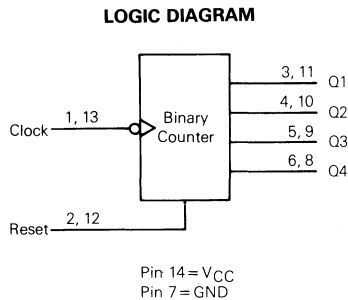
### High-Performance Silicon-Gate CMOS

The MC54/74HC393 is identical in pinout to the LS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

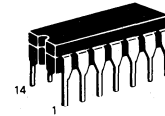
This device consists of two independent 4-bit binary ripple counters with parallel outputs from each counter stage. A  $\pm 256$  counter can be obtained by cascading the two binary counters.

Internal flip-flops are triggered by high-to-low transitions of the clock input. Reset for the counters is asynchronous and active-high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC393.

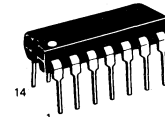
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 236 FETs or 59 Equivalent Gates



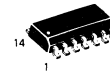
## MC54/74HC393



**J SUFFIX  
 CERAMIC  
 CASE 632-08**



**N SUFFIX  
 PLASTIC  
 CASE 646-06**



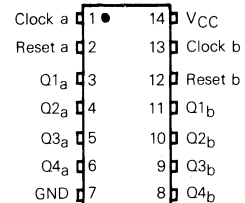
**D SUFFIX  
 SOIC  
 CASE 751A-02**

### ORDERING INFORMATION

MC74HCXXXD	SOIC
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Outputs
Clock	Reset	
X	H	L
H	L	No Change
L	L	No Change
	L	No Change
	L	Advance to Next State

# MC54/74HC393

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC393

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	5.4	4.4	3.6	MHz
		4.5	27	22	18	
		6.0	32	26	21	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q2 (Figures 1 and 3)	2.0	190	240	285	ns
		4.5	38	48	57	
		6.0	32	41	48	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q3 (Figures 1 and 3)	2.0	240	300	360	ns
		4.5	48	60	72	
		6.0	41	51	61	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q4 (Figures 1 and 3)	2.0	290	365	435	ns
		4.5	58	73	87	
		6.0	49	62	74	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Counter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		40	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC393

## PIN DESCRIPTIONS

### INPUTS

**CLOCK (PINS 1, 13)** — Clock input. The internal flip-flops are toggled and the counter state advances on high-to-low transitions of the clock input.

### CONTROL INPUTS

**RESET (PINS 2, 12)** — Active-high, asynchronous reset. A

separate reset is provided for each counter. A high at the Reset input prevents counting and forces all four outputs low.

### OUTPUTS

**Q1, Q2, Q3, Q4 (PINS 3, 4, 5, 6, 8, 9, 10, 11)** — Parallel binary outputs. Q4 is the most significant bit.

## SWITCHING WAVEFORMS

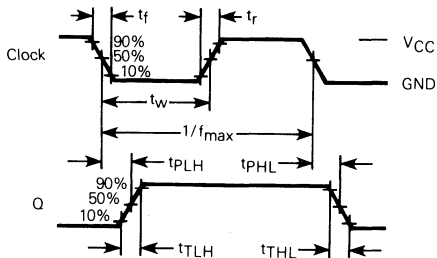


Figure 1.

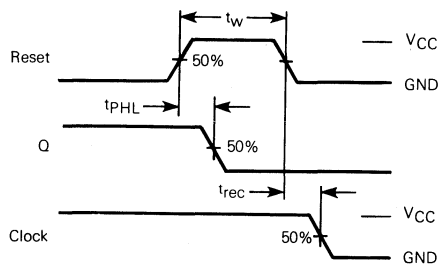
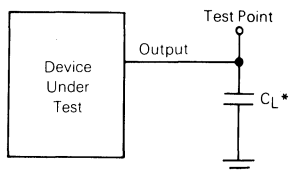


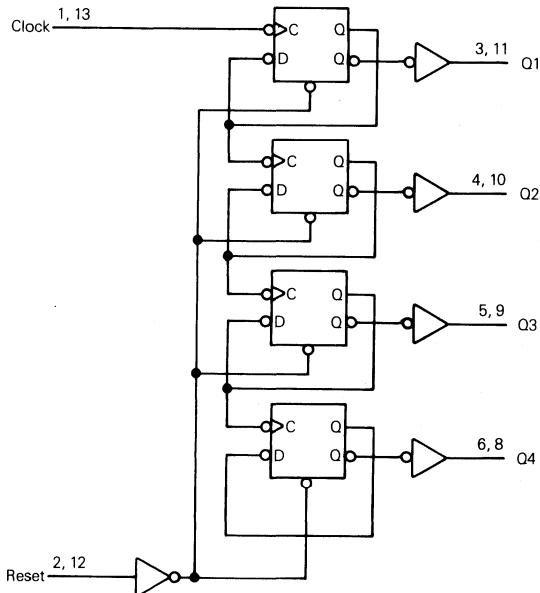
Figure 2.



\* Includes all probe and jig capacitance.

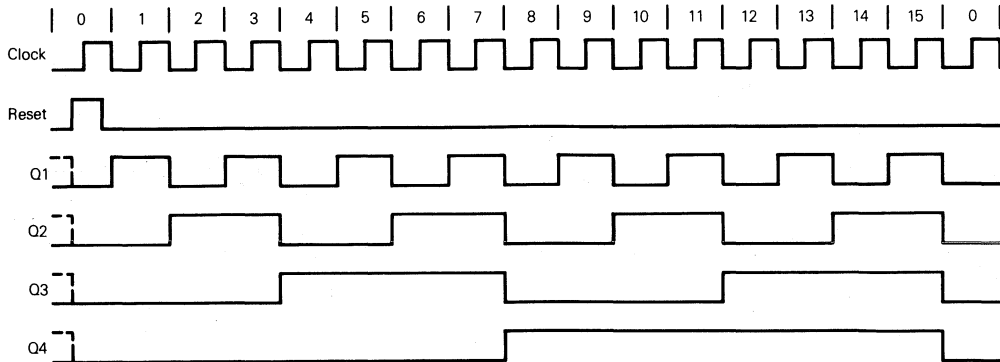
Figure 3. Test Circuit

## EXPANDED LOGIC DIAGRAM



# MC54/74HC393

## TIMING DIAGRAM



## COUNT SEQUENCE

Count	Outputs			
	Q4	Q3	Q2	Q1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

## Octal 3-State Inverting D Flip-Flop

### High-Performance Silicon-Gate CMOS

The MC54/74HC534A is identical in pinout to the LS534. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

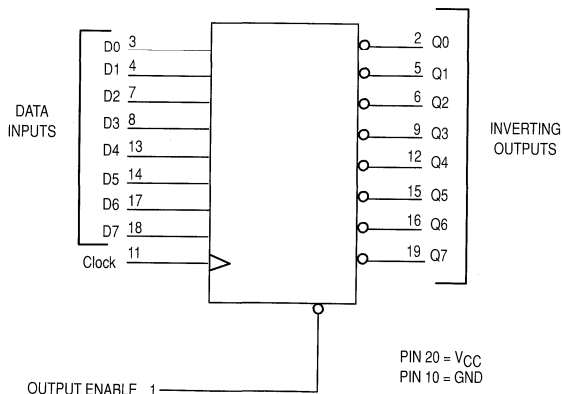
Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC534A is identical in function to the HC564 which has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

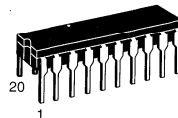
This device is similar in function to the HC374A, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 282 FETs or 68.5 Equivalent Gates

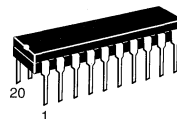
**LOGIC DIAGRAM**



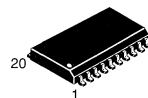
## MC54/74HC534A



**J SUFFIX**  
**CERAMIC**  
**CASE 732-03**



**N SUFFIX**  
**PLASTIC**  
**CASE 738-03**

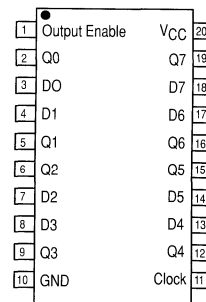


**DW SUFFIX**  
**SOIC**  
**CASE 751D-03**

### ORDERING INFORMATION

MC74HCXXAN	Plastic
MC54HCXXAJ	Ceramic
MC74HCXXADW	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Output Enable	Inputs		Output
	Clock	D	Q
L		H	L
L		L	H
L	L, H,	X	no change
H	X	X	Z

X = Don't Care  
 Z = High Impedance



# MC54/74HC534A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C °C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limits			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	2.0	0.1	0.1	0.1	μA
			4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC534A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limits			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   = 0 μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)							
Symbol	Parameter	Fig.	V <sub>CC</sub> V	Guaranteed Limits			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)	1, 4	2.0 4.5 6.0	6.0 30 35	5.0 24 28	4.0 20 24	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q	1, 4	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q	2, 5	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q	2, 5	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t <sub>TLH</sub> t <sub>THL</sub>	Maximum Output Transition Time, Any Output	1, 4	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns

C <sub>in</sub>	Maximum Input Capacitance		10	10	10	pF	
C <sub>OUT</sub>	Maximum Tri-State Output Capacitance, (Output in Hi-Impedance State)		15	15	15	pF	
C <sub>PD</sub>	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>		Typical @ 25°C, V <sub>CC</sub> = 5.0 V			34	pF

5

TIMING REQUIREMENTS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)										
Symbol	Parameter	Fig.	V <sub>CC</sub> V	Guaranteed Limits						Unit
				25°C to -55°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t <sub>su</sub>	Minimum Setup Time, Data to Clock	3	2.0 4.5 6.0	50 10 9.0		65 13 11		75 15 13		ns
t <sub>h</sub>	Minimum Hold Time, Clock to Data	3	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t <sub>w</sub>	Minimum Pulse Width, Clock	1	2.0 4.5 6.0	60 12 10		75 15 13		90 18 15		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns

# MC54/74HC534A

## SWITCHING WAVEFORMS

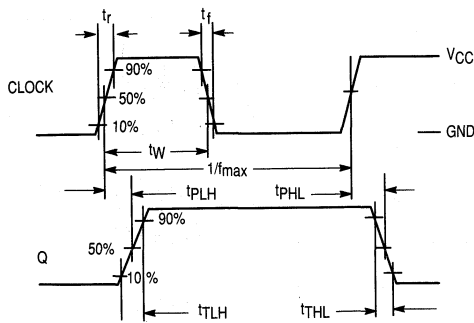


Figure 1.

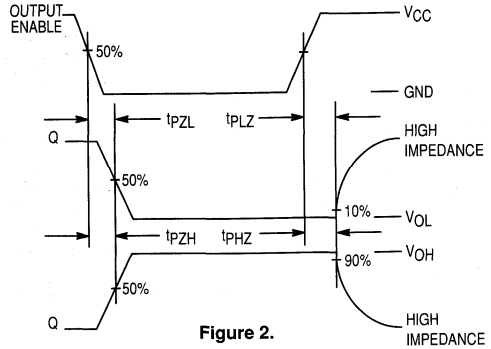


Figure 2.

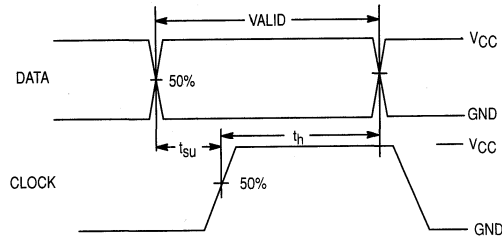
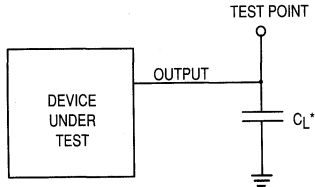


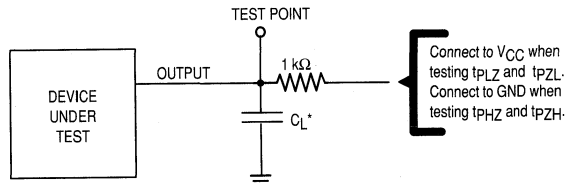
Figure 3.

## TEST CIRCUITS



\* Includes all probe and jig capacitance

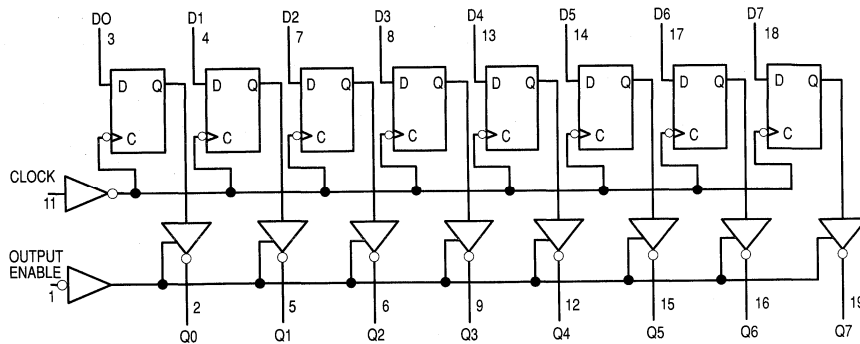
Figure 4.



\* Includes all probe and jig capacitance

Figure 5.

## EXPANDED LOGIC DIAGRAM



# Octal 3-State Inverting Buffer/Line Driver/Line Receiver

## High-Performance Silicon-Gate CMOS

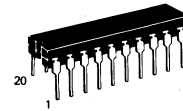
The MC54/74HC540 is identical in pinout to the LS540. The device inputs are compatible with standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

The HC540 is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

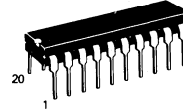
The HC540 is similar in function to the HC541, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 124 FETs or 31 Equivalent Gates

### MC54/74HC540



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03



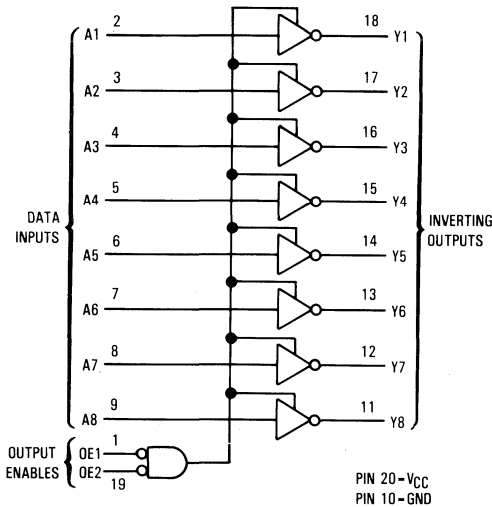
DW SUFFIX  
 SOIC  
 CASE 751D-03

#### ORDERING INFORMATION

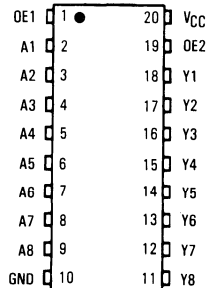
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENTS



#### FUNCTION TABLE

Inputs			Output
OE1	OE2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = high impedance  
 X = don't care

# MC54/74HC540

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	3.98 5.48	3.84 5.34	3.70 5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	0.26 0.26	0.33 0.33	0.40 0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC540

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

**NOTES:**

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

## SWITCHING WAVEFORMS

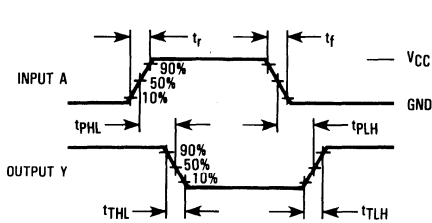


Figure 1.

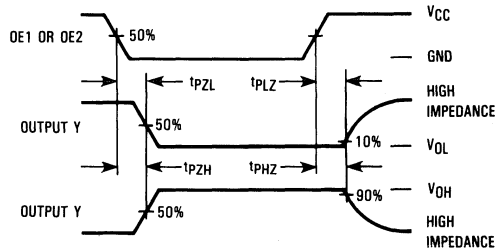
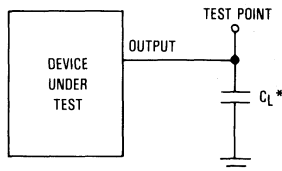


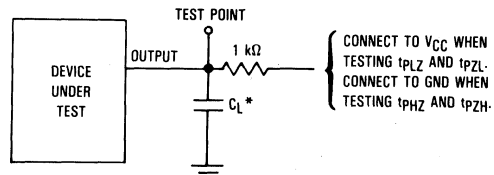
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.



\*Includes all probe and jig capacitance.

Figure 4.

# MC54/74HC540

## PIN DESCRIPTIONS

### INPUTS

**A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9)** — Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROLS

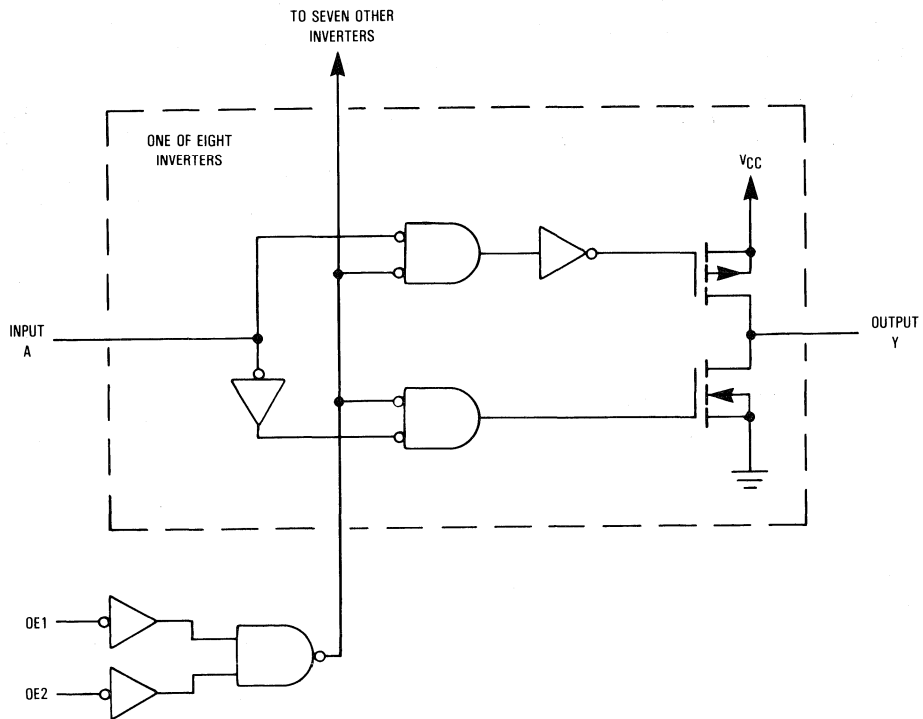
**OE1, OE2 (PINS 1, 19)** — Output enables (active-low). When a low voltage is applied to both of these pins, the outputs

are enabled and the device functions as an inverter. When a high voltage is applied to either input, the outputs assume the high impedance state.

### OUTPUTS

**Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11)** — Device outputs. Depending upon the state of the output enable pins, these outputs are either inverting outputs or high-impedance outputs.

## LOGIC DETAIL



# Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

## High-Performance Silicon-Gate CMOS

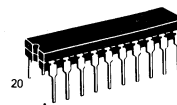
The MC54/74HC541 is identical in pinout to the LS541. The device inputs are compatible with standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

The HC541 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

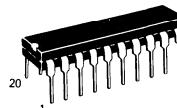
The HC541 is similar in function to the HC540, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 140 FETs or 35 Equivalent Gates

### MC54/74HC541



**J SUFFIX**  
**CERAMIC**  
**CASE 732-03**



**N SUFFIX**  
**PLASTIC**  
**CASE 738-03**



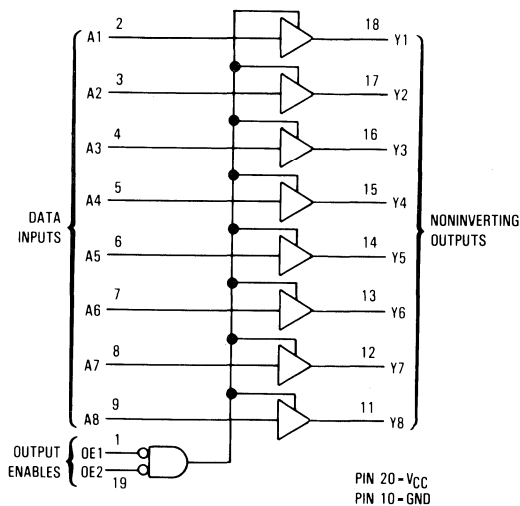
**DW SUFFIX**  
**SOIC**  
**CASE 751D-03**

#### ORDERING INFORMATION

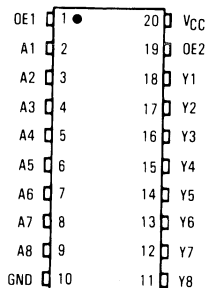
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs		Output	
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = high impedance  
 X = don't care



# MC54/74HC541

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit	
				25°C to -55°C	≤85°C	≤125°C		
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V	
			4.5	3.15	3.15	3.15		
			6.0	4.2	4.2	4.2		
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V	
			4.5	0.9	0.9	0.9		
			6.0	1.2	1.2	1.2		
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V	
			4.5	4.4	4.4	4.4		
			6.0	5.9	5.9	5.9		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V	
			4.5	0.1	0.1	0.1		
			6.0	0.1	0.1	0.1		
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA	
			Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0		±10.0
				6.0	8	80		160
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC541

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

## SWITCHING WAVEFORMS

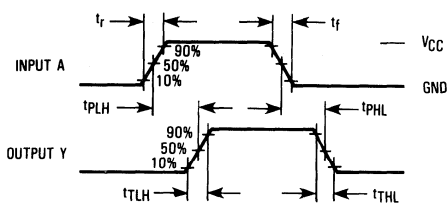


Figure 1.

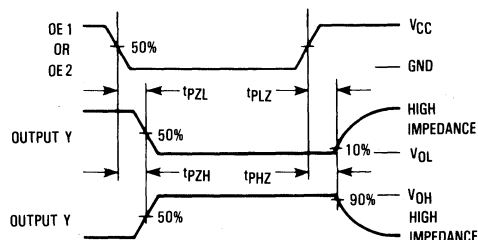
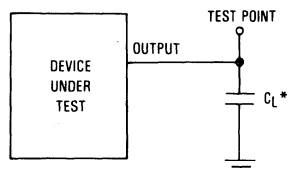


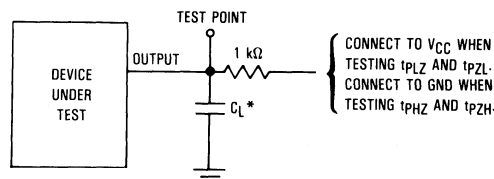
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.



\*Includes all probe and jig capacitance.

Figure 4.

# MC54/74HC541

## PIN DESCRIPTIONS

### INPUTS

**A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9)** — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROLS

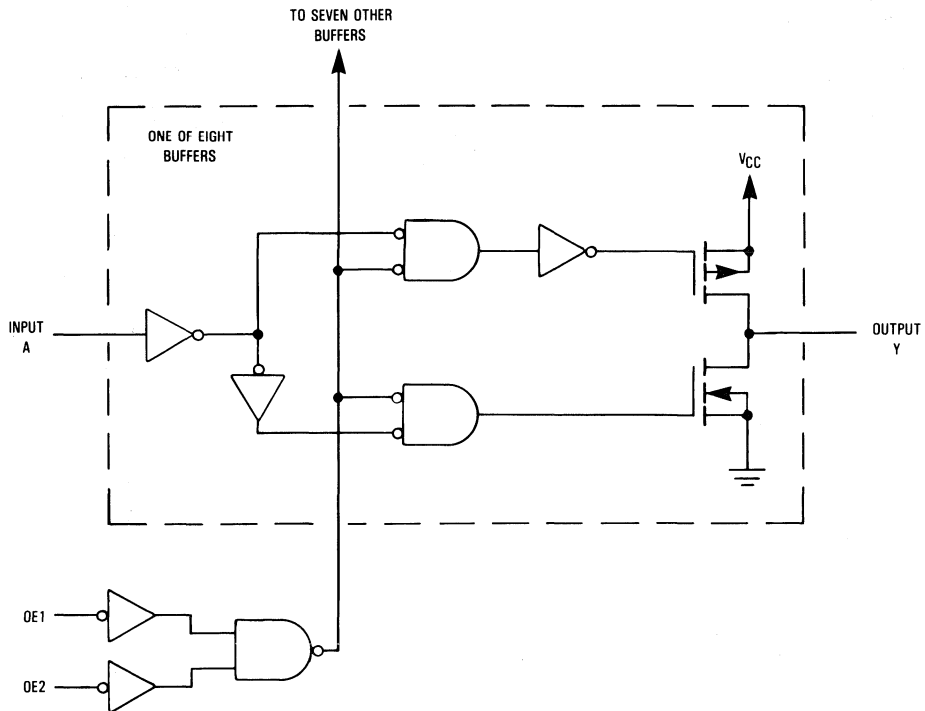
**OE1, OE2 (PINS 1, 19)** — Output enables (active-low). When a low level is applied to both of these pins, the outputs

are enabled and the device functions as a noninverting buffer. When a high level is applied to either input, the outputs assume the high impedance state.

### OUTPUTS

**Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11)** — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high impedance outputs.

## LOGIC DETAIL



**MC54/74HCT541**

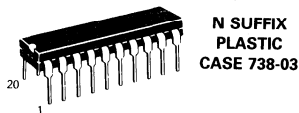
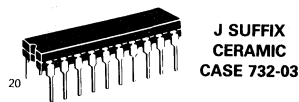
**Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS**

The MC54/74HCT541 is identical in pinout to the LS541. The device may be used as a level converter for interfacing TTL or NMOS to High-Speed CMOS inputs.

The HCT541 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HCT541 is similar in function to the HCT540, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 180 FETs or 45 Equivalent Gates

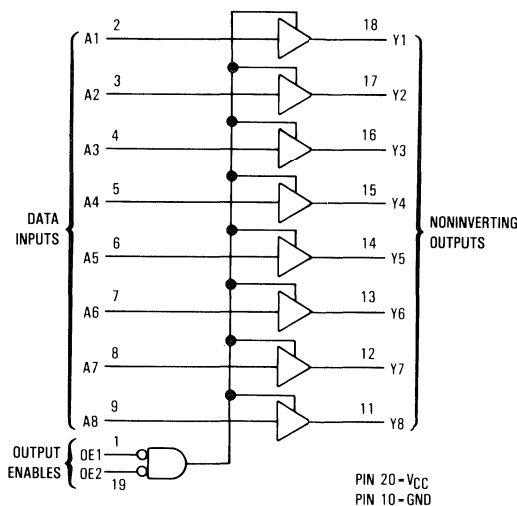


**ORDERING INFORMATION**

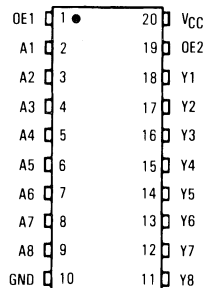
MC74HCTXXXN Plastic  
 MC54HCTXXXJ Ceramic  
 MC74HCTXXXDW SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

**LOGIC DIAGRAM**



**PIN ASSIGNMENTS**



**FUNCTION TABLE**

Inputs			Output
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = high impedance  
 X = don't care

# MC54/74HCT541

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
		5.5	5.4	5.4	5.4		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA	4.5	3.98	3.84	3.70	V
		5.5	0.1	0.1	0.1		
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	4.5	0.1	0.1	0.1	μA
			5.5	0.1	0.1	0.1	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	4.5	0.26	0.33	0.40	μA
			5.5	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	4.5	±0.5	±5.0	±10.0	μA
			5.5	8	80	160	

ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	Guaranteed Limit		mA
			≥ -55°C	25°C to 125°C	
			5.5	2.9	2.4

### NOTES:

- Information on typical parametric values can be found in Chapter 4.
- Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

5

# MC54/74HCT541

AC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5.0\text{ V} \pm 10\%$ ,  $C_L=50\text{ pF}$ , Input  $t_r=t_f=6\text{ ns}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	30	38	45	ns
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	35	44	53	ns
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	45	56	68	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

**NOTES:**

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

$C_{PD}$	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	pF
		50	

## SWITCHING WAVEFORMS

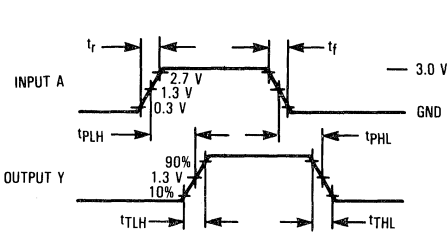


Figure 1.

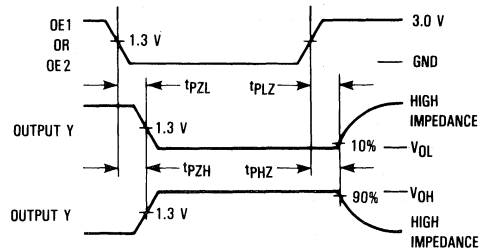
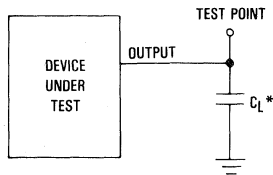


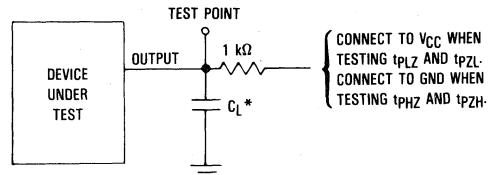
Figure 2.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 3.



\*Includes all probe and jig capacitance.

Figure 4.

# MC54/74HCT541

## PIN DESCRIPTIONS

### INPUTS

**A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9)** — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROLS

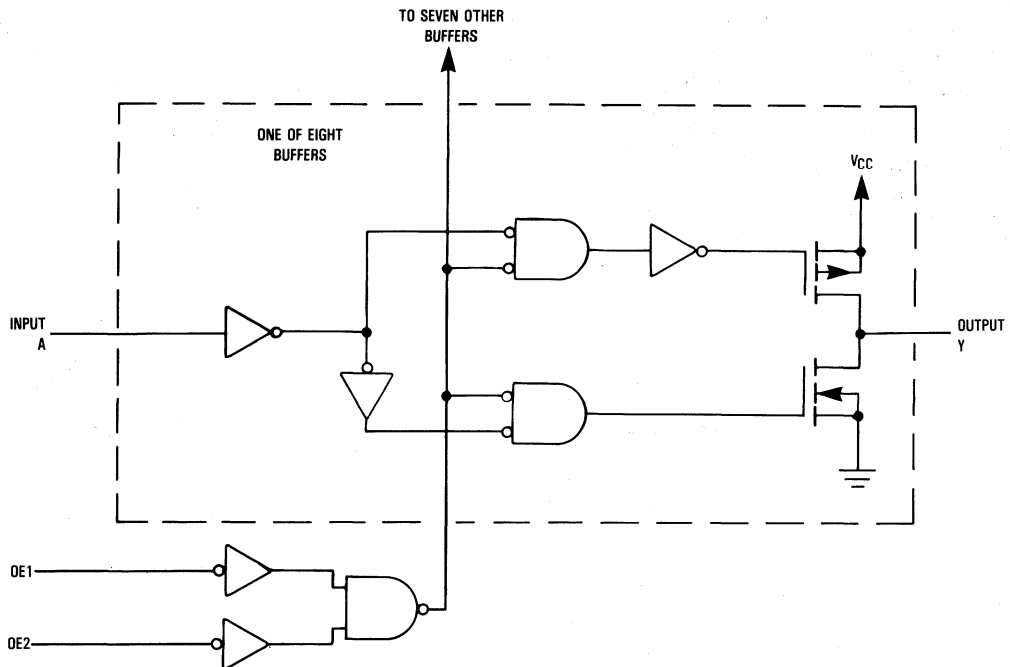
**OE1, OE2 (PINS 1, 19)** — Output enables (active low). When a low level is applied to both of these pins, the outputs

are enabled and the device functions as a noninverting buffer. When a high level is applied to either input, the outputs assume the high impedance state.

### OUTPUTS

**Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11)** — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high impedance outputs.

## LOGIC DETAIL



## Octal 3-State Inverting Transparent Latch

### High-Performance Silicon-Gate CMOS

The MC54/74HC563 is identical in pinout to the LS563. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

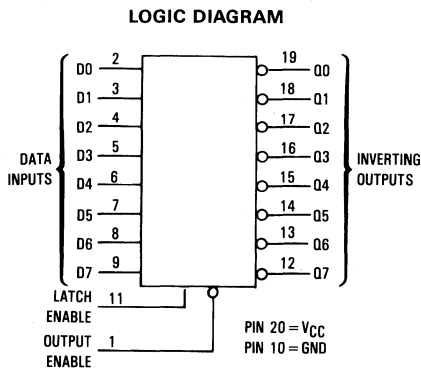
This device is identical in function to the HC533 but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. The data appears at the outputs in inverted form. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

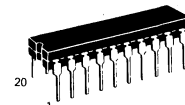
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC573 is the noninverting version of this function.

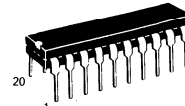
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates



## MC54/74HC563



**J SUFFIX  
CERAMIC  
CASE 732-03**



**N SUFFIX  
PLASTIC  
CASE 738-03**



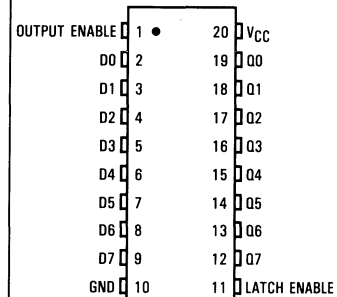
**DW SUFFIX  
SOIC  
CASE 751D-03**

### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output	
Output Enable	Latch Enable	D	Q
L	H	H	L
L	H	L	H
L	L	X	no change
H	X	X	Z

X = don't care  
 Z = high impedance



# MC54/74HC563

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
Ceramic DIP: - 10 mW/°C from 100° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to - 55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC563

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		37	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC563

## SWITCHING WAVEFORMS

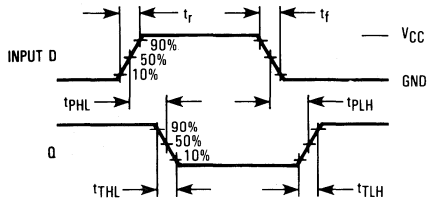


Figure 1.

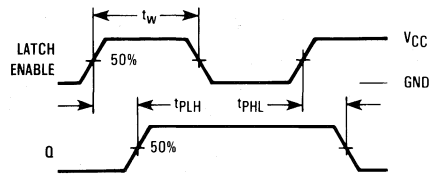


Figure 2.

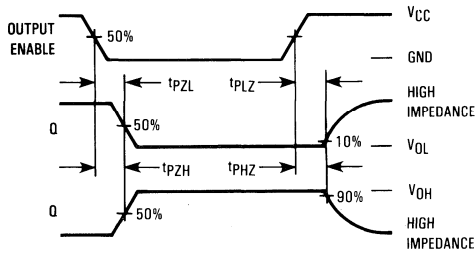


Figure 3.

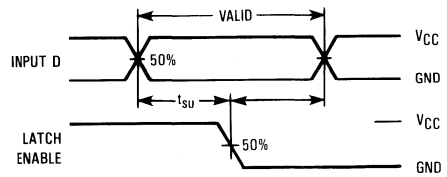
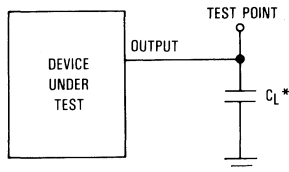


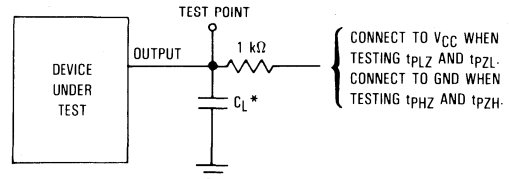
Figure 4.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 5.

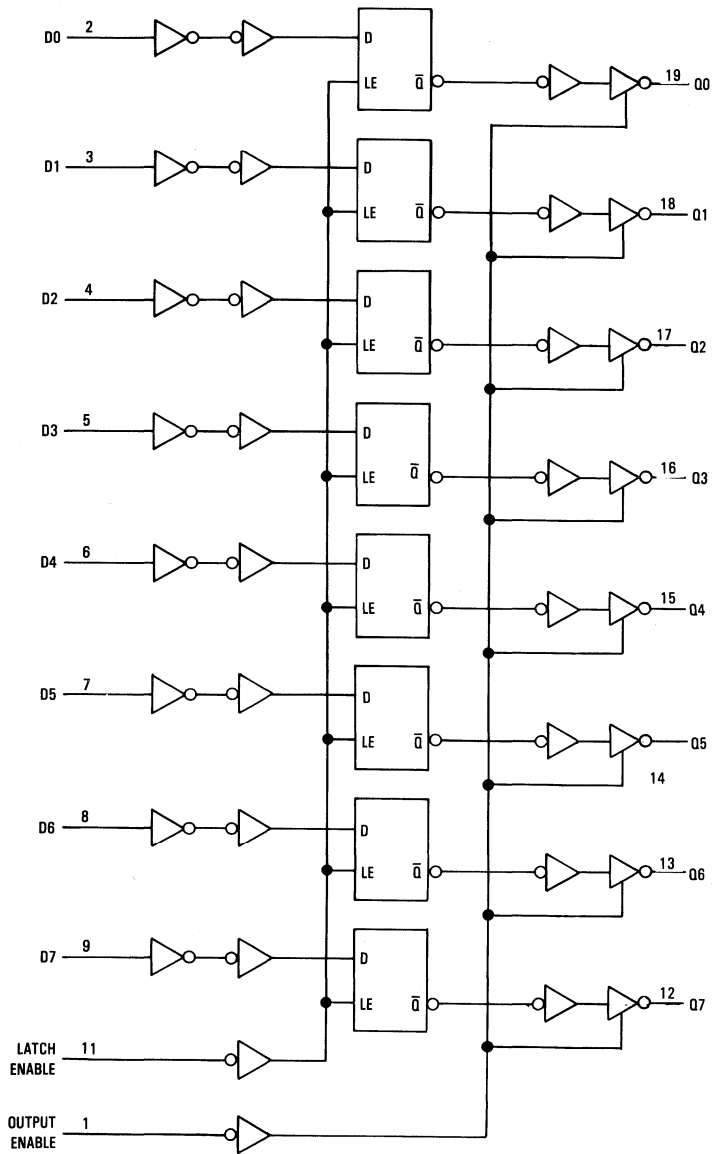


\*Includes all probe and jig capacitance.

Figure 6.

# MC54/74HC563

## EXPANDED LOGIC DIAGRAM



5

**MC54/74HC564**

**Octal 3-State  
 Inverting D Flip-Flop  
 High-Performance Silicon-Gate CMOS**

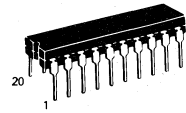
The MC54/74HC564 is identical in pinout to the LS564. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs.

This device is identical in function to the HC534A but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

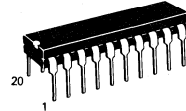
Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC564 is the inverting version of the HC574A.

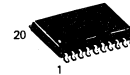
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 282 FETs or 70.5 Equivalent Gates



**J SUFFIX  
 CERAMIC  
 CASE 732-03**



**N SUFFIX  
 PLASTIC  
 CASE 738-03**



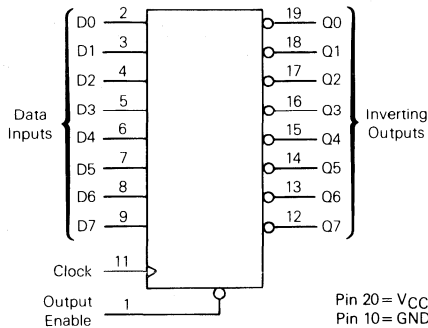
**DW SUFFIX  
 SOIC  
 CASE 751D-03**

**ORDERING INFORMATION**

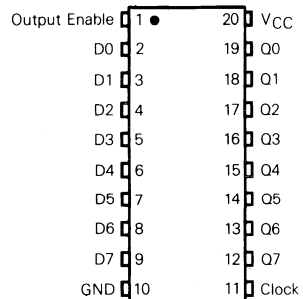
- |             |         |
|-------------|---------|
| MC74HCXXXN  | Plastic |
| MC54HCXXXJ  | Ceramic |
| MC74HCXXXDW | SOIC    |

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs		Output	
Output Enable	Clock	D	Q
L		H	L
L		L	H
L	L, H,	X	no change
H	X	X	Z

X = don't care  
 Z = high impedance

# MC54/74HC564

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	2.0	0.26	0.33	0.40	μA
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND Output in High-Impedance State V <sub>in</sub> =V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> =V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC564

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		38	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Clock to Data (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC564

## SWITCHING WAVEFORMS

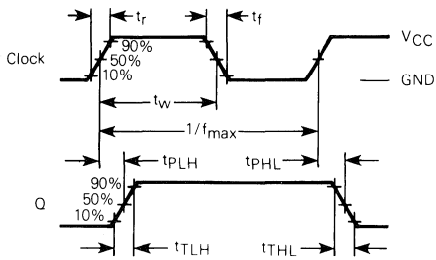


Figure 1.

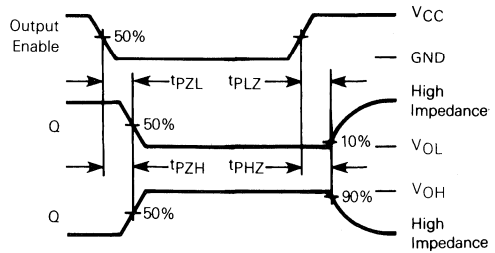


Figure 2.

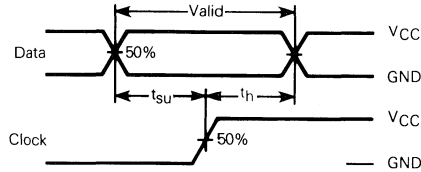
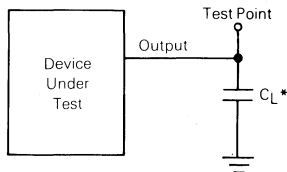


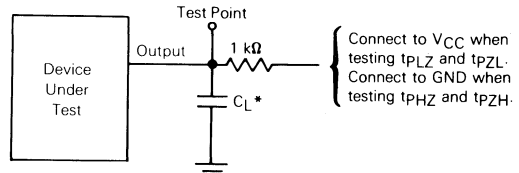
Figure 3.

## TEST CIRCUITS



\* Includes all probe and jig capacitance.

Figure 4.



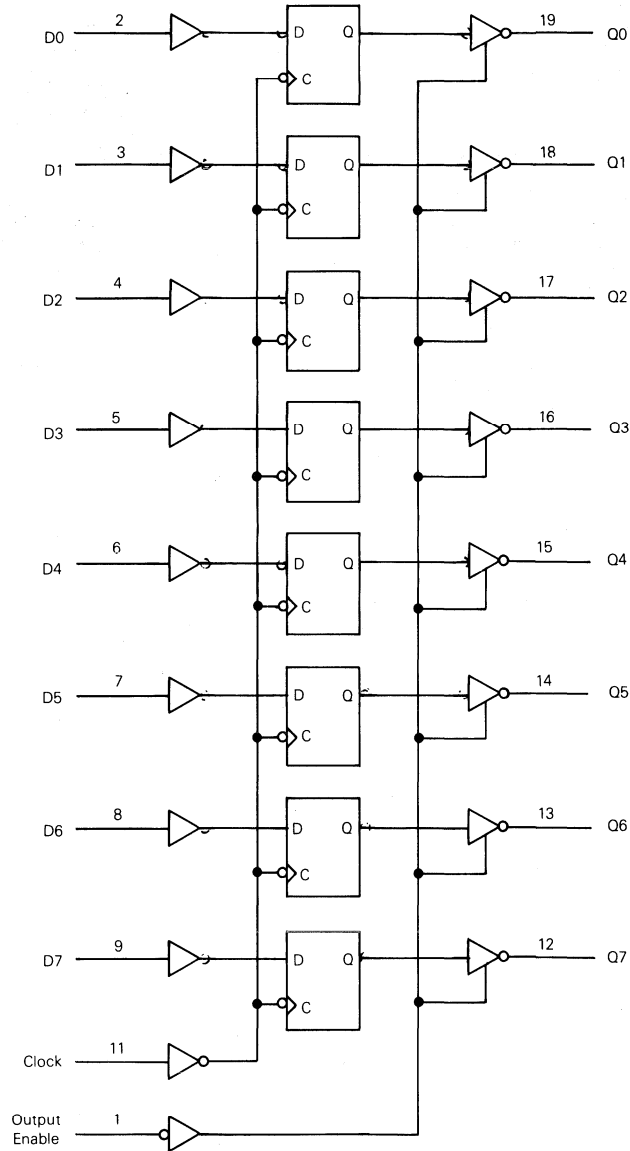
\* Includes all probe and jig capacitance.

Figure 5.



# MC54/74HC564

## EXPANDED LOGIC DIAGRAM



## Octal 3-State Noninverting Transparent Latch High-Performance Silicon-Gate CMOS

The MC54/74HC573A is identical in pinout to the LS573. The devices are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

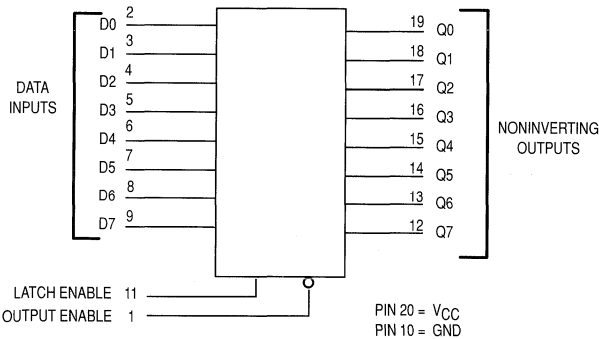
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The HC573A is identical in function to the HCT373A but has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC573A is the noninverting version of the HC563.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates

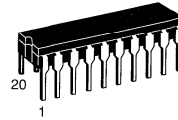
### LOGIC DIAGRAM



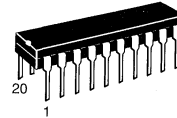
Design Criteria	Value	Unit
Internal Gate Count *	54.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	0.0075	pJ

\*Equivalent to a two-input NAND gate.

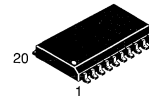
## MC54/74HC573A



J SUFFIX  
CERAMIC  
CASE 732-03



N SUFFIX  
PLASTIC  
CASE 738-03

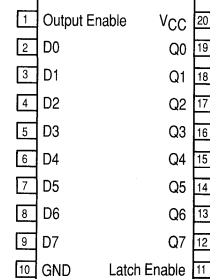


DW SUFFIX  
SOIC  
CASE 751D-03

### ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXADW	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = Don't Care

Z = High Impedance

# MC54/74HC573A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating – Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.7	V
			6.0	5.48	5.34	5.2	
			2.0	0.1	0.1	0.1	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			6.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	6.0	0.26	0.33	0.4	V
			2.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.10	±1.0	±1.0	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC573A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	-0.5	-5.0	-10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   = 0 μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)							
Symbol	Parameter	V <sub>CC</sub> Volts	Guaranteed Limit			Unit	
			25°C to -55°C	≤85°C	≤125°C		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns	
C <sub>in</sub>	Maximum Input Capacitance		10	10	10	pF	
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)		15	15	15	pF	
C <sub>PD</sub>	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>		Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF	
						23	

5

TIMING REQUIREMENTS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)										
Symbol	Parameter	Fig.	V <sub>CC</sub> Volts	Guaranteed Limit						Unit
				25°C to -55°C		≤85°C		≤125°C		
				Min	Max	Min	Max	Min	Max	
t <sub>SU</sub>	Minimum Setup Time, Input D to Latch Enable	4	2.0 4.5 6.0	50 10 9.0		65 13 11		75 15 13		ns
t <sub>H</sub>	Minimum Hold Time, Latch Enable to Input D	4	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t <sub>w</sub>	Minimum Pulse Width, Latch Enable	2	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns

# MC54/74HC573A

## SWITCHING WAVEFORMS

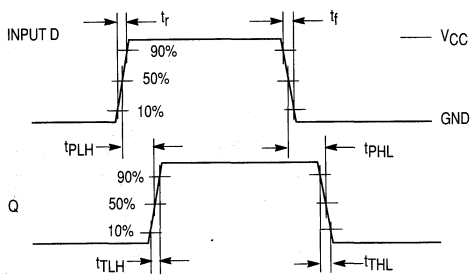


Figure 1.

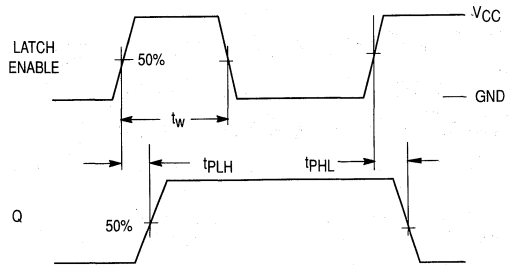


Figure 2.

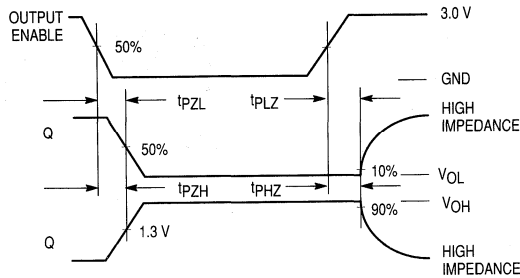


Figure 3.

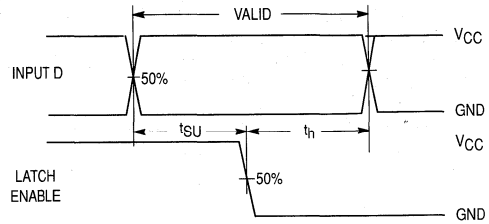
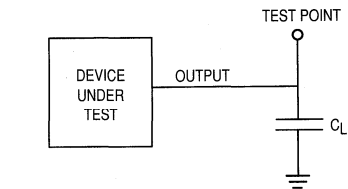
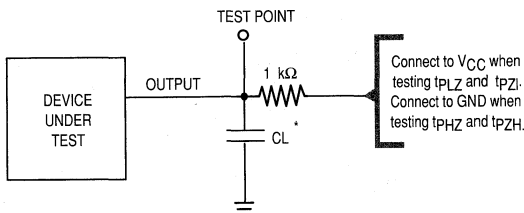


Figure 4.



\* Includes all probe and jig capacitance

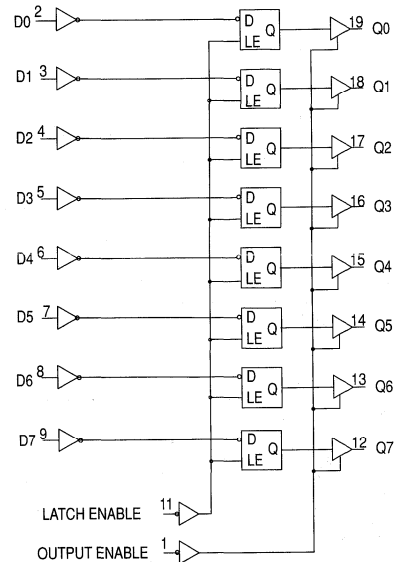
Figure 5. Test Circuit



\* Includes all probe and jig capacitance

Figure 6. Test Circuit

### EXPANDED LOGIC DIAGRAM



## Octal 3-State Noninverting Transparent Latch with LSTTL Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT573A is identical in pinout to the LS573. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

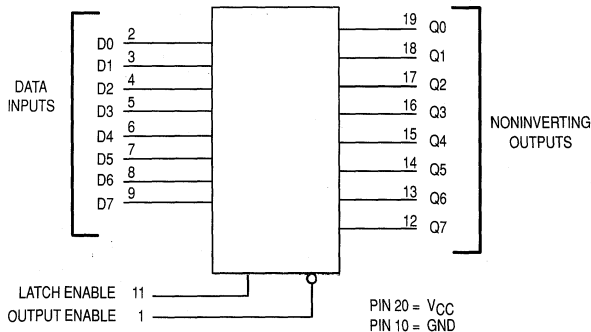
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT573A is identical in function to the HCT373A but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HCT573A is the noninverting version of the HC563.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 10  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
  - Improved Propagation Delays
  - 50% Lower Quiescent Power

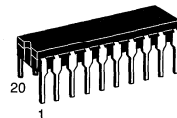
### LOGIC DIAGRAM



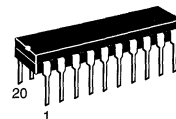
Design Criteria	Value	Unit
Internal Gate Count *	58.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	0.0075	pJ

\*Equivalent to a two-input NAND gate.

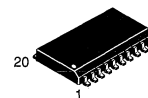
## MC54/74HCT573A



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03

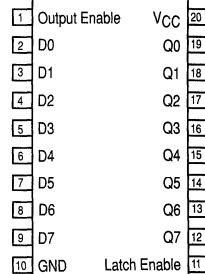


DW SUFFIX  
 SOIC  
 CASE 751D-03

### ORDERING INFORMATION

MC74HCTXXXAN	Plastic
MC54HCTXXXAJ	Ceramic
MC74HCTXXXADW	SOIC

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output	
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = Don't Care  
 Z = High Impedance

# MC54/74HCT573A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C °C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS				
Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
			4.5	3.98	3.84	3.7	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
			4.5	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HCT573A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> ≤ 0 μA	5.5	4.0	40	160	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

AC ELECTRICAL CHARACTERISTICS (V <sub>CC</sub> = 5.0 V ±10%, C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)					
Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input D to Output Q (Figures 1 and 5)	30	38	45	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	30	38	45	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t <sub>TZL</sub> , t <sub>TZH</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, any Output (Figures 1 and 5)	12	15	18	ns
C <sub>in</sub>	Maximum Input Capacitance	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF
CPD	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = CPD V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
		48			

5

TIMING REQUIREMENTS (V <sub>CC</sub> = 5.0 V ±10%, C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)									
Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			25°C to -55°C		≤85°C		≤125°C		
			Min	Max	Min	Max	Min	Max	
t <sub>su</sub>	Minimum Setup Time, Input D to Latch Enable	4	10		13		15		ns
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input D	4	5.0		5.0		5.0		ns
t <sub>w</sub>	Minimum Pulse Width, Latch Enable	2	15		19		22		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1		500		500		500	ns



# MC54/74HCT573A

## SWITCHING WAVEFORMS

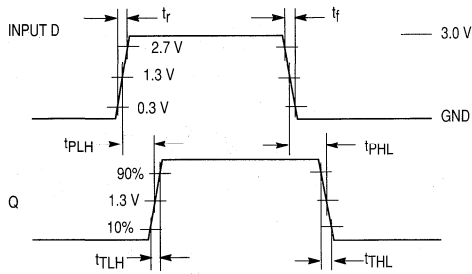


Figure 1.

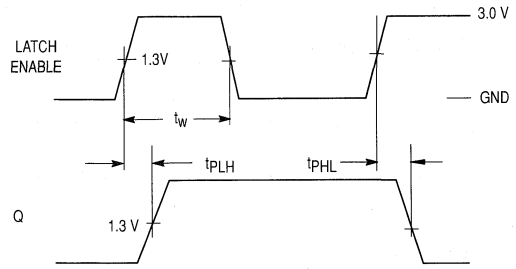


Figure 2.

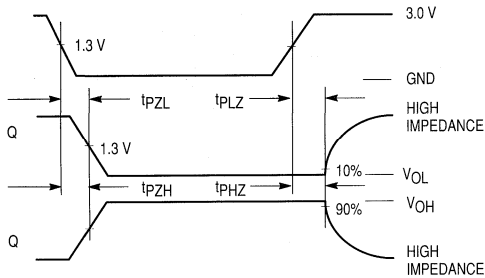


Figure 3.

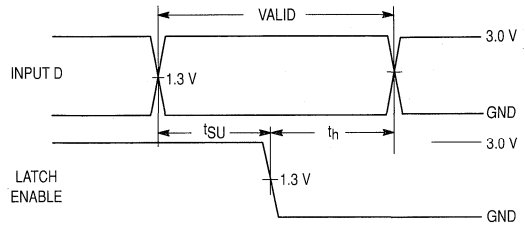
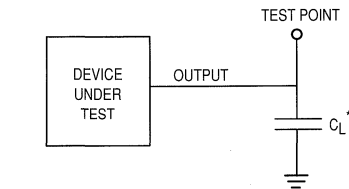
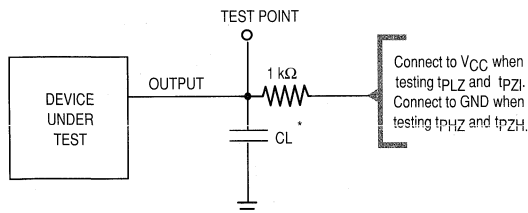


Figure 4.



\* Includes all probe and jig capacitance

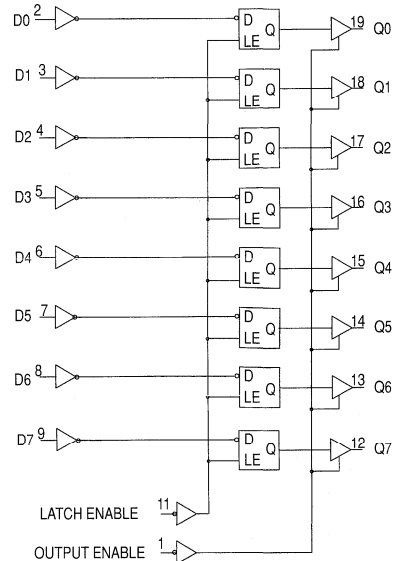
Figure 5. Test Circuit



\* Includes all probe and jig capacitance

Figure 6. Test Circuit

### EXPANDED LOGIC DIAGRAM



## Octal 3-State Noninverting D Flip-Flop High-Performance Silicon-Gate CMOS

The MC54/74HC574A is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

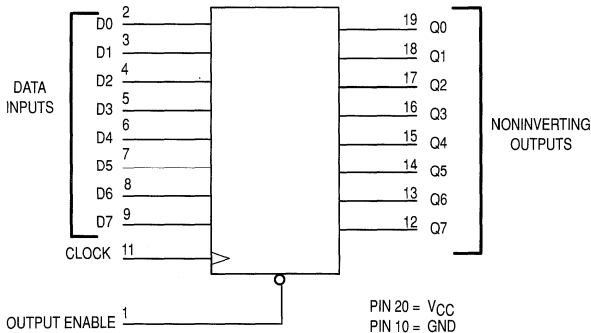
Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574A is identical in function to the HCT374A but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC574A is the noninverting version of the HC564.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates

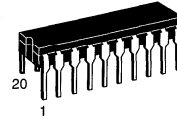
**LOGIC DIAGRAM**



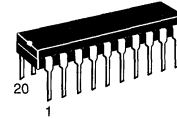
Design Criteria	Value	Unit
Internal Gate Count *	66.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	0.0075	$\mu$ J

\*Equivalent to a two-input NAND gate.

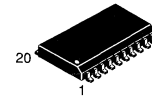
## MC54/74HC574A



**J SUFFIX  
 CERAMIC  
 CASE 732-03**



**N SUFFIX  
 PLASTIC  
 CASE 738-03**

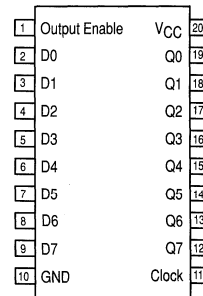


**DW SUFFIX  
 SOIC  
 CASE 751D-03**

**ORDERING INFORMATION**

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXADW	SOIC

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs			Output
Reset	Clock	D	Q
L		H	H
L		L	L
L		X	no change
H	X	X	Z

X = Don't Care  
 Z = High Impedance

# MC54/74HC574A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C
		300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC574A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   = 0 μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)							
Symbol	Parameter	V <sub>CC</sub> Volts	Guaranteed Limit			Unit	
			25°C to -55°C	≤85°C	≤125°C		
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns	

C <sub>in</sub>	Maximum Input Capacitance		10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance, Output in High-Impedance State		15	15	15	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	pF	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
			24			

5

TIMING REQUIREMENTS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)										
Symbol	Parameter	Fig.	V <sub>CC</sub> Volts	Guaranteed Limit						Unit
				25°C to -55°C		≤85°C		≤125°C		
				Min	Max	Min	Max	Min	Max	
t <sub>su</sub>	Minimum Setup Time, Data to Clock	3	2.0	50		65		75		ns
			4.5	10		13		15		
			6.0	9.0		11		13		
t <sub>h</sub>	Minimum Hold Time, Clock to Data	3	2.0	5.0		5.0		5.0		ns
			4.5	5.0		5.0		5.0		
			6.0	5.0		5.0		5.0		
t <sub>w</sub>	Minimum Pulse Width, Clock	1	2.0	75		95		110		ns
			4.5	15		19		22		
			6.0	13		16		19		
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1	2.0		1000		1000		1000	ns
			4.5		500		500		500	
			6.0		400		400		400	

# MC54/74HC574A

## SWITCHING WAVEFORMS

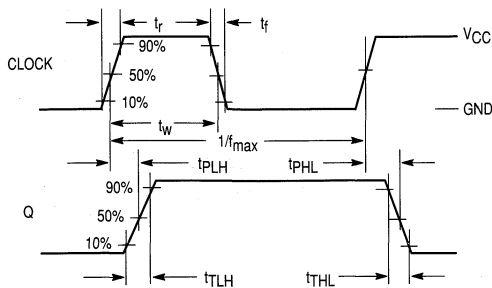


Figure 1.

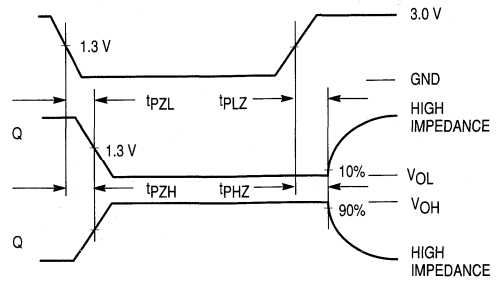


Figure 2.

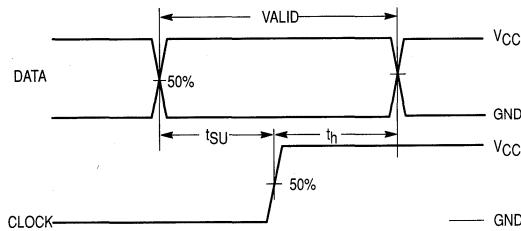


Figure 3.

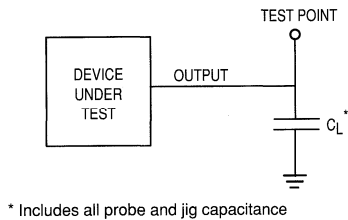
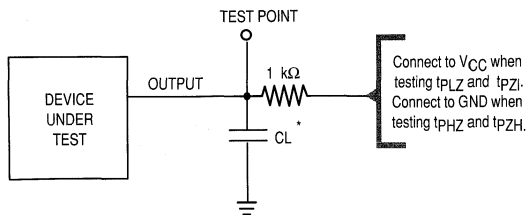


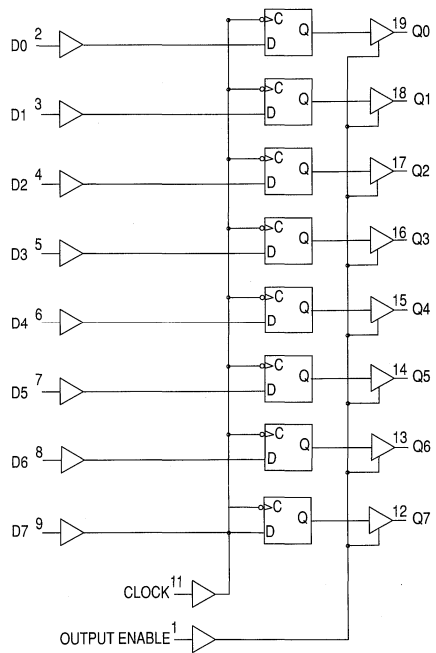
Figure 4. Test Circuit



\*Includes all probe and jig capacitance

Figure 5. Test Circuit

## EXPANDED LOGIC DIAGRAM



## Octal 3-State Noninverting D Flip-Flop with LSTTL Compatible Inputs High-Performance Silicon-Gate CMOS

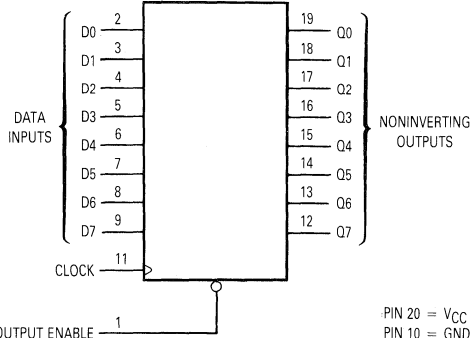
The MC54/74HCT574A is identical in pinout to the LS574. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HCT574A is identical in function to the HCT374A but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates

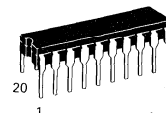
**LOGIC DIAGRAM**



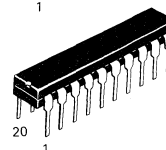
Design Criteria	Value	Unit
Internal Gate Count*	71.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	$\mu$ W
Speed Power Product	0.0075	pJ

\*Equivalent to a two-input NAND gate.

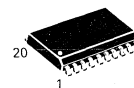
### MC54/74HCT574A



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03

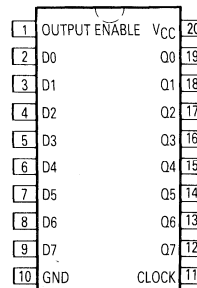


DW SUFFIX  
 SOIC  
 CASE 751D-03

#### ORDERING INFORMATION

MC74HCTXXXAN	Plastic
MC54HCTXXXAJ	Ceramic
MC74HCTXXXADW	SOIC

#### PIN ASSIGNMENT



#### FUNCTION TABLE

Inputs		Output	
Reset	Clock	D	Q
L		H	H
L		L	L
L		L,H,	no change
H	X	X	Z

X = don't care Z = High impedance

# MC54/74HCT574A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	4.5	0.26	0.33	0.4	μA
			5.5	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	4.5	4.0	40	160	μA
			5.5	4.0	40	160	

1. Output in high-impedance state.  
 NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HCT574A

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
I <sub>OZ</sub>	Maximum Three-State Leakage Current	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Note 1) V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	-0.5	-5.0	-10	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

1. Output in high-impedance state.

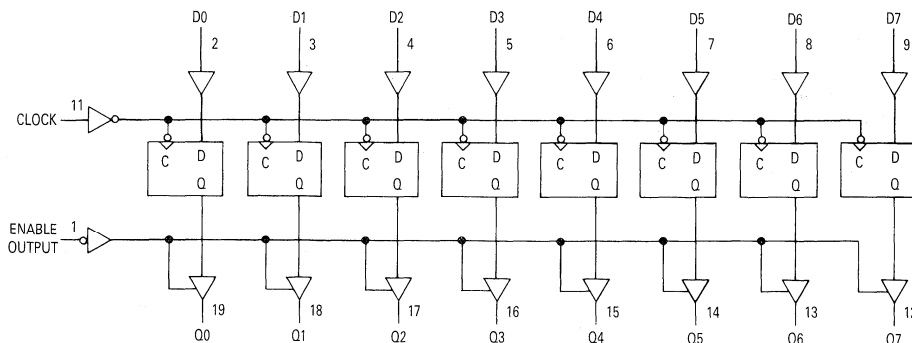
## AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0 V ± 10%, C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
f <sub>MAX</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	30	38	45	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	28	35	42	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Propagation Delay Time, Output Enable to Q (Figures 2 and 5)	28	35	42	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1, 2 and 4)	12	15	18	ns
C <sub>in</sub>	Maximum Input Capacitance	10	10	10	PF
C <sub>PD</sub>	Power Dissipation Capacitance (Flip-Flop) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
		58			

## TIMING REQUIREMENTS (V<sub>CC</sub> = 5.0 V ± 10%, C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			25°C to -55°C		≤85°C		≤125°C		
			Min	Max	Min	Max	Min	Max	
t <sub>SU</sub>	Minimum Setup Time, Data to Clock	3	10		13		15		ns
t <sub>H</sub>	Minimum Hold Time, Clock to Data	3	5.0		5.0		5.0		ns
t <sub>w</sub>	Minimum Pulse Width, Clock	1	15		19		22		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	1		500		500		500	ns

## EXPANDED LOGIC DIAGRAM





# MC54/74HCT574A

## SWITCHING WAVEFORMS

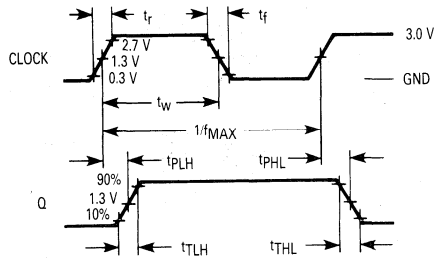


Figure 1.

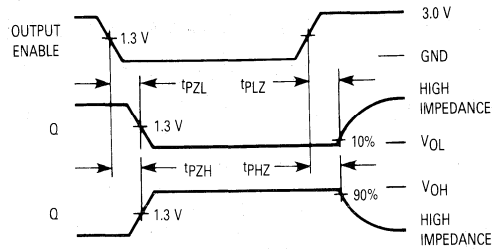


Figure 2.

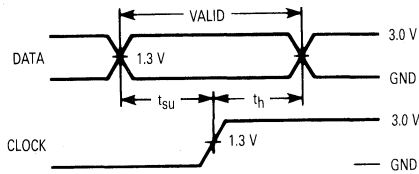
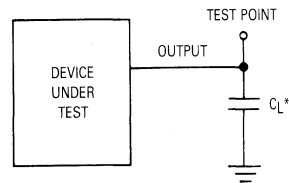
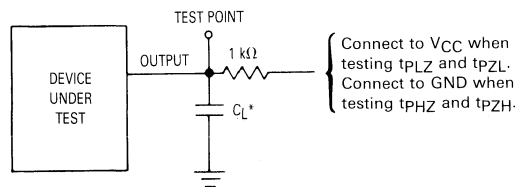


Figure 3.



\*Includes all probe and jig capacitance

Figure 4. Test Circuit



\*Includes all probe and jig capacitance

Figure 5. Test circuit

# 8-Bit Serial or Parallel-Input/ Serial-Output Shift Register with 3-State Output

## High-Performance Silicon-Gate CMOS

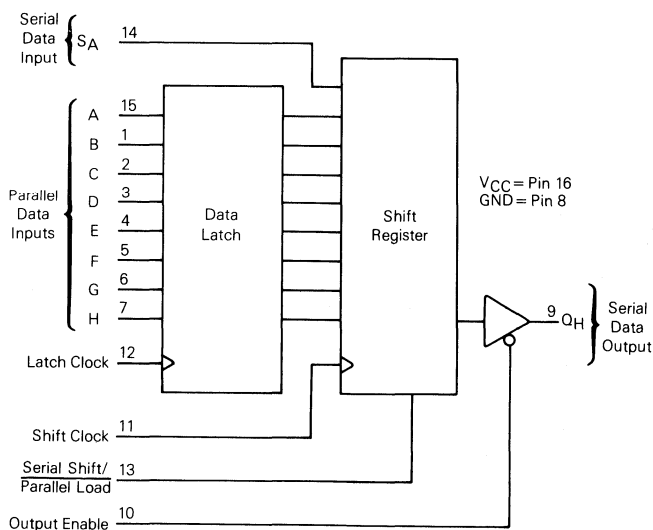
The MC54/74HC589 is similar in function to the HC597, which is not a 3-state device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table). The shift register output,  $Q_H$ , is a three-state output, allowing this device to be used in bus-oriented systems.

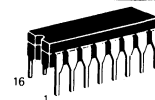
The HC589 directly interfaces with the Motorola SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current:  $1 \mu\text{A}$
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates

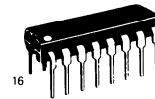
### LOGIC DIAGRAM



## MC54/74HC589



**J SUFFIX**  
**CERAMIC**  
 CASE 620-09



**N SUFFIX**  
**PLASTIC**  
 CASE 648-08



**D SUFFIX**  
**SOIC**  
 CASE 751B-04

### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT

B	1	16	VCC
C	2	15	A
D	3	14	SA
E	4	13	Serial Shift/ Parallel Load
F	5	12	Latch Clock
G	6	11	Shift Clock
H	7	10	Output Enable
GND	8	9	$Q_H$

# MC54/74HC589

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	6.0	5.9	5.9	5.9	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC589

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Clock to Q <sub>H</sub> (Figures 1 and 8)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Shift Clock to Q <sub>H</sub> (Figures 2 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Serial Shift/Parallel Load to Q <sub>H</sub> (Figures 4 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q <sub>H</sub> (Figures 3 and 9)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q <sub>H</sub> (Figures 3 and 9)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

**NOTES:**

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = CPD V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		50	

# MC54/74HC589

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>SU</sub>	Minimum Setup Time, A-H to Latch Clock (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>SU</sub>	Minimum Setup Time, Serial Data Input S <sub>A</sub> to Shift Clock (Figure 6)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>SU</sub>	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>H</sub>	Minimum Hold Time, Latch Clock to A-H (Figure 5)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t <sub>H</sub>	Minimum Hold Time, Shift Clock to Serial Data Input S <sub>A</sub> (Figure 6)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>W</sub>	Minimum Pulse Width, Shift Clock (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>W</sub>	Minimum Pulse Width, Latch Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>W</sub>	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

## FUNCTION TABLE

Operation	Inputs						Resulting Function			
	Output Enable	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S <sub>A</sub>	Parallel Inputs A-H	Data Latch Contents	Shift Register Contents	Output Q <sub>H</sub>	
Force output into high-impedance state	H	X	X	X	X	X	X	X	Z	
Load parallel data into data latch	L	H		L, H,	X	a-h	a-h	U	U	
Transfer latch contents to shift register	L	L	L, H,	X	X	X	U	LR <sub>N</sub> → SR <sub>N</sub>	LR <sub>H</sub>	
Contents of input latch and shift register are unchanged	L	H	L, H,	L, H,	X	X	U	U	U	
Load parallel data into data latch and shift register	L	L		X	X	a-h	a-h	a-h	h	
Shift serial data into shift register	L	H	X		D	X	*	SR <sub>A</sub> = D; SR <sub>N</sub> → SR <sub>N+1</sub>	SR <sub>G</sub> → SR <sub>H</sub>	
Load parallel data in data latch and shift serial data into shift register	L	H			D	a-h	a-h	SR <sub>A</sub> = D; SR <sub>N</sub> → SR <sub>N+1</sub>	SR <sub>G</sub> → SR <sub>H</sub>	

LR = latch register contents

SR = shift register contents

a-h = data at parallel data inputs A-H

D = data (L, H) at serial data input S<sub>A</sub>

U = remains unchanged

X = don't care

Z = high impedance

\* = depends on Latch Clock input

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# MC54/74HC589

## SWITCHING WAVEFORMS

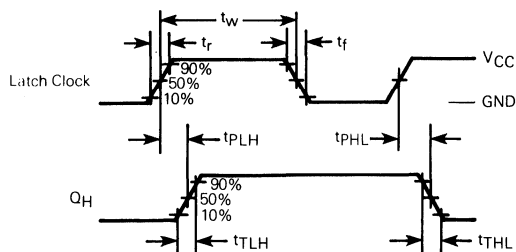


Figure 1. (Serial Shift/Parallel Load = L)

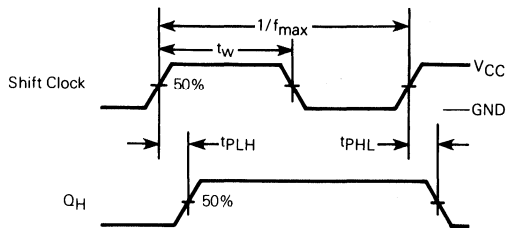


Figure 2. (Serial Shift/Parallel Load = H)

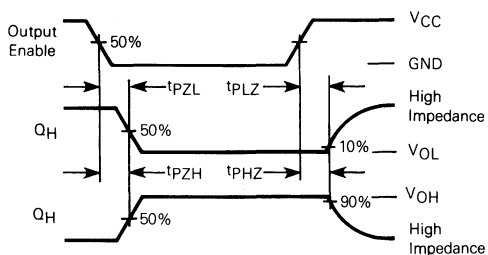


Figure 3.

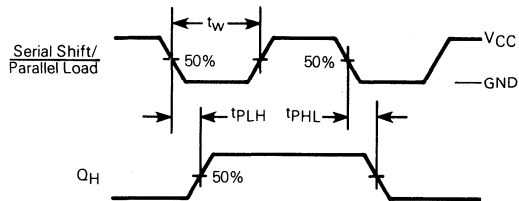


Figure 4.

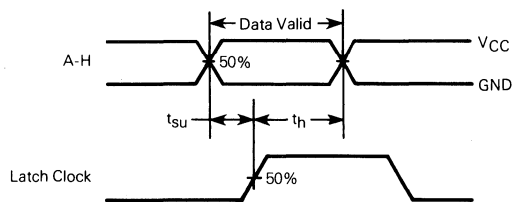


Figure 5.

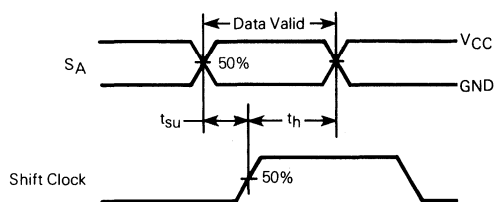


Figure 6.

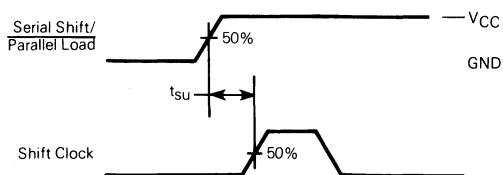
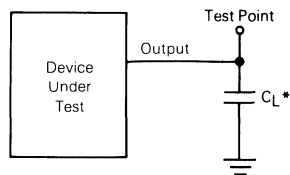


Figure 7.



\* Includes all probe and jig capacitance.

Figure 8. Test Circuit

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# MC54/74HC589

## TEST CIRCUIT

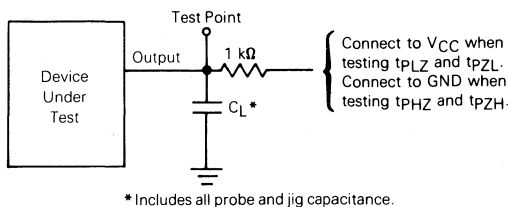


Figure 9.

## PIN DESCRIPTIONS

### DATA INPUTS

**A, B, C, D, E, F, G, H (PINS 15, 1, 2, 3, 4, 5, 6, 7)** — Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

**SA (PIN 14)** — Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

### CONTROL INPUTS

**SERIAL SHIFT/PARALLEL LOAD (PIN 13)** — Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

**SHIFT CLOCK (PIN 11)** — Serial shift clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and data in stage H is shifted out  $Q_H$ , being replaced by the data previously stored in stage G.

**LATCH CLOCK (PIN 12)** — Data latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the data latch.

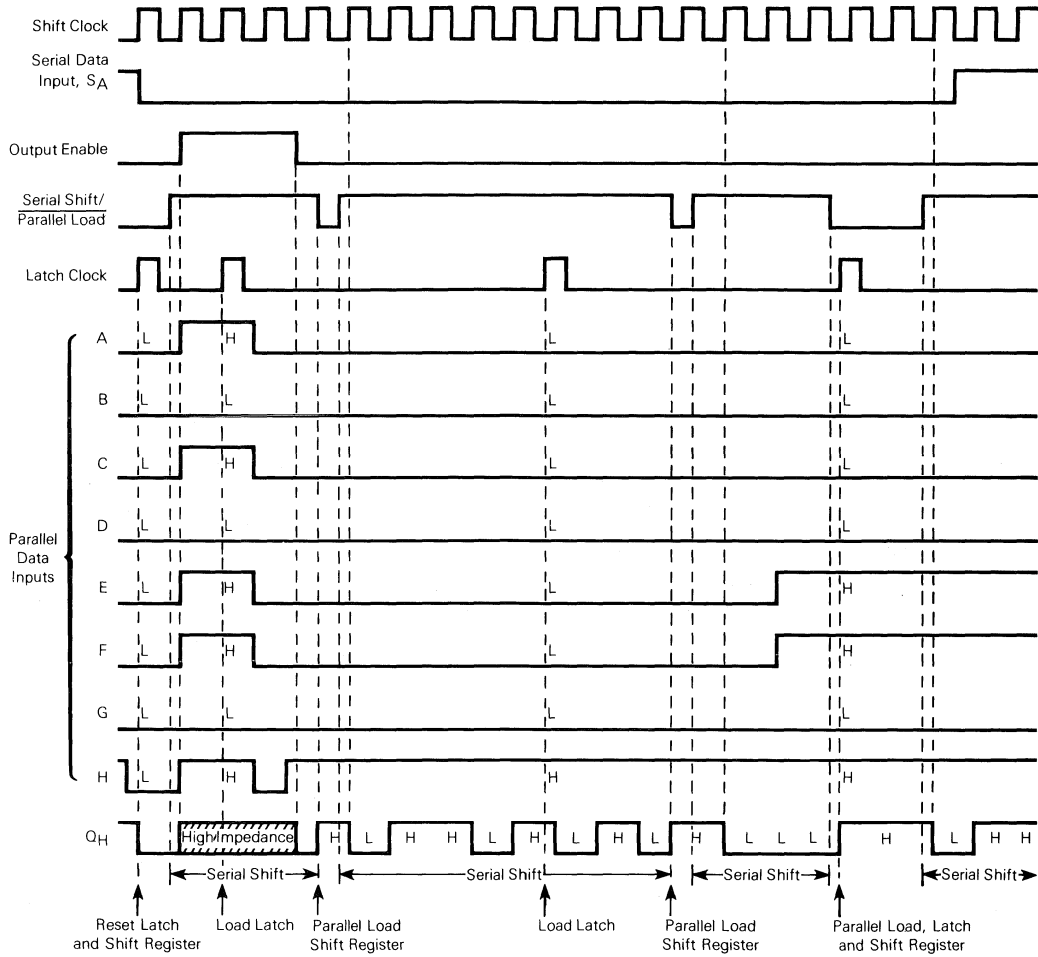
**OUTPUT ENABLE (PIN 10)** — Active-low output enable. A high level applied to this pin forces the  $Q_H$  output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

### OUTPUT

**$Q_H$  (PIN 9)** — Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.

# MC54/74HC589

## TIMING DIAGRAM

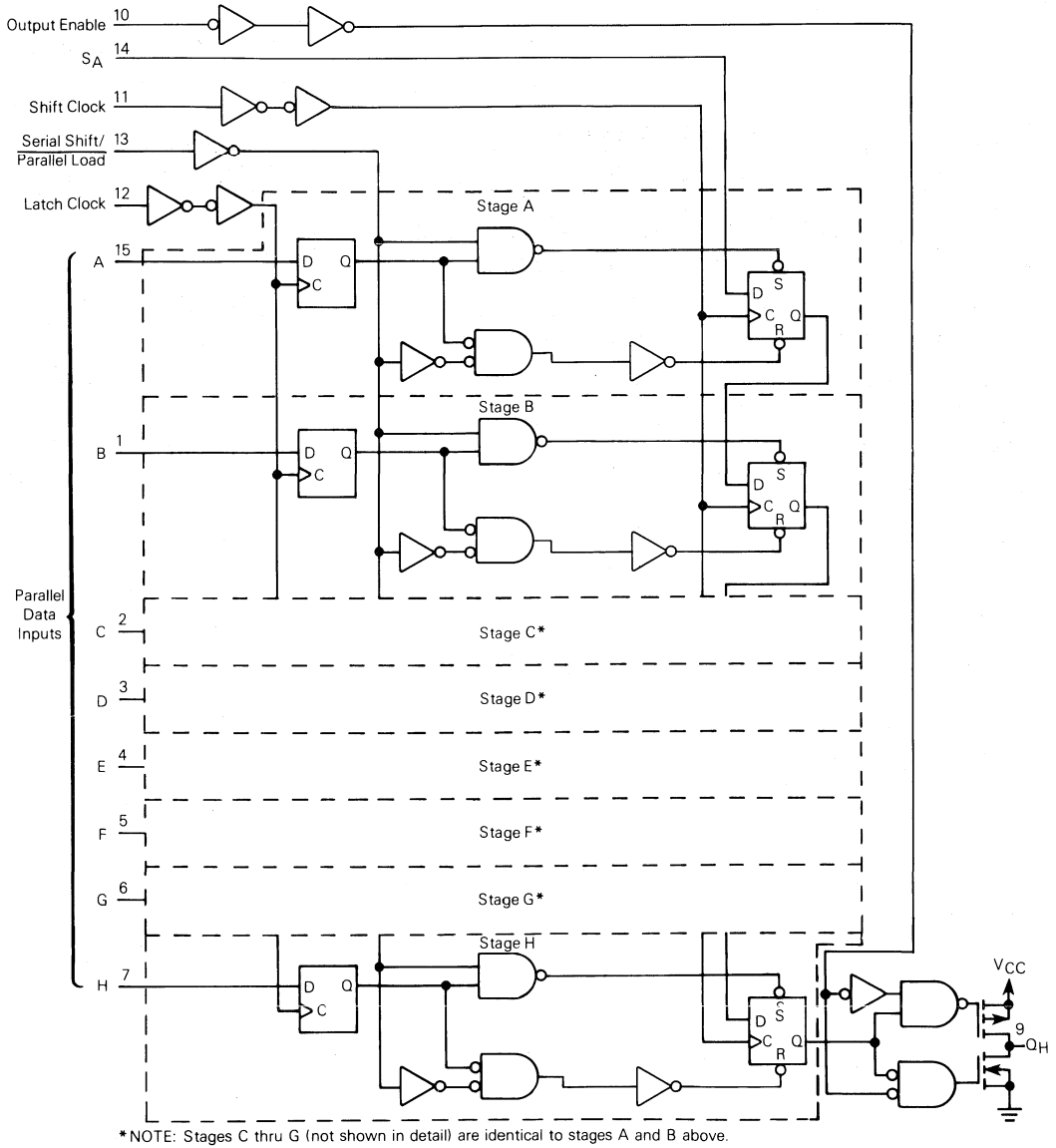


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# MC54/74HC589

## LOGIC DETAIL



## 8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs High-Performance Silicon-Gate CMOS

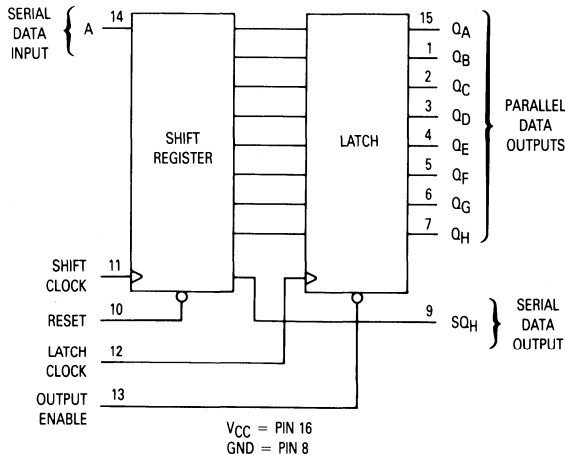
The MC54/74HC595A is identical in pinout to the LS595. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC595A consists of an 8-bit shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

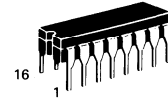
The HC595A directly interfaces with the Motorola SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
  - Improved Propagation Delays
  - 50% Lower Quiescent Power
  - Improved Input Noise and Latchup Immunity

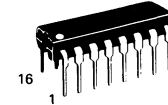
### LOGIC DIAGRAM



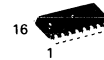
## MC54/74HC595A



J SUFFIX  
 CERAMIC  
 CASE 620-09



N SUFFIX  
 PLASTIC  
 CASE 648-08

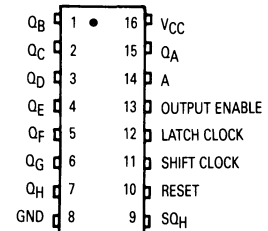


D SUFFIX  
 SOIC  
 CASE 751B-04

### ORDERING INFORMATION

MC74HCXXXAN	Plastic
MC54HCXXXAJ	Ceramic
MC74HCXXXAD	SOIC

### PIN ASSIGNMENT



# MC54/74HC595A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit	
				25°C to -55°C	≤85°C	≤125°C		
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V	
			4.5	3.15	3.15	3.15		
			6.0	4.2	4.2	4.2		
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V	
			4.5	1.35	1.35	1.35		
			6.0	1.8	1.8	1.8		
V <sub>OH</sub>	Minimum High-Level Output Voltage, Q <sub>A</sub> -Q <sub>H</sub>	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V	
			4.5	4.4	4.4	4.4		
			6.0	5.9	5.9	5.9		
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	3.98	3.84		3.7
				6.0	5.48	5.34		5.2
				6.0	5.48	5.34		5.2
V <sub>OL</sub>	Maximum Low-Level Output Voltage, Q <sub>A</sub> -Q <sub>H</sub>	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V	
			4.5	0.1	0.1	0.1		
			6.0	0.1	0.1	0.1		
			V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	0.26	0.33		0.4
				6.0	0.26	0.33		0.4
				6.0	0.26	0.33		0.4

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC595A

## DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>OH</sub>	Minimum High-Level Output Voltage, SQ <sub>H</sub>	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage, SQ <sub>H</sub>	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	2.0	0.1	0.1	0.1	μA
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>OZ</sub>	Maximum Three-State Leakage Current, Q <sub>A</sub> -Q <sub>H</sub>	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	2.0	±0.5	±5.0	±10	μA
			4.5	±0.5	±5.0	±10	
			6.0	±0.5	±5.0	±10	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	2.0	4.0	40	160	μA
			4.5	4.0	40	160	
			6.0	4.0	40	160	

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Shift Clock to SQ <sub>H</sub> (Figures 1 and 7)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to SQ <sub>H</sub> (Figures 2 and 7)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Clock to Q <sub>A</sub> -Q <sub>H</sub> (Figures 3 and 7)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Q <sub>A</sub> -Q <sub>H</sub> (Figures 4 and 8)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Q <sub>A</sub> -Q <sub>H</sub> (Figures 4 and 8)	2.0	135	170	205	ns
		4.5	27	34	41	
		6.0	23	29	35	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Q <sub>A</sub> -Q <sub>H</sub> (Figures 3 and 7)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, SQ <sub>H</sub> (Figures 1 and 7)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q <sub>A</sub> -Q <sub>H</sub>	—	15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		300	

# MC54/74HC595A

## TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
$t_{su}$	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
$t_{su}$	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$t_h$	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0	5.0	5.0	5.0	ns
		4.5	5.0	5.0	5.0	
		6.0	5.0	5.0	5.0	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
$t_w$	Minimum Pulse Width, Shift Clock (Figure 1)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
$t_w$	Minimum Pulse Width, Latch Clock (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

## FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ <sub>H</sub>	Parallel Outputs QA-QH
Reset shift register	L	X	X	L, H,	L	L	U	L	U
Shift data into shift register	H	D		L, H,	L	D → SR <sub>A</sub> ; SR <sub>N</sub> → SR <sub>N+1</sub>	U	SR <sub>G</sub> → SR <sub>H</sub>	U
Shift register remains unchanged	H	X	L, H,	L, H,	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H,		L	U	SR <sub>N</sub> → LR <sub>N</sub>	U	SR <sub>N</sub>
Latch register remains unchanged	X	X	X	L, H,	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high-impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents  
LR = latch register contents

D = data (L, H) logic level  
U = remains unchanged

X = don't care  
Z = high impedance

\* = depends on Reset and Shift Clock inputs  
\*\* = depends on Latch Clock input

## PIN DESCRIPTIONS

### INPUTS

**A (Pin 14)** — Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

### CONTROL INPUTS

**Shift Clock (Pin 11)** — Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

**Reset (Pin 10)** — Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

**Latch Clock (Pin 12)** — Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

**Output Enable (Pin 13)** — Active-low Output Enable. A low on this input allows the data from the latches to be

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# MC54/74HC595A

presented at the outputs. A high on this input forces the outputs ( $Q_A$ - $Q_H$ ) into the high-impedance state. The serial output is not affected by this control unit.

3-state, latch outputs.

**SQH (Pin 9)** — Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

## OUTPUTS

**$Q_A$ - $Q_H$  (Pins 15, 1, 2, 3, 4, 5, 6, 7)** — Noninverted,

## SWITCHING WAVEFORMS

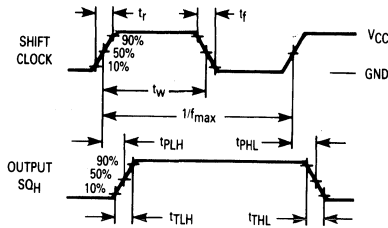


Figure 1.

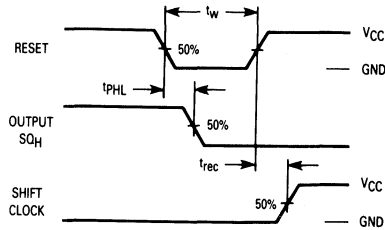


Figure 2.

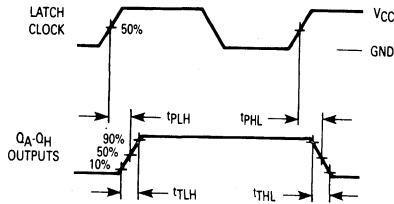


Figure 3.

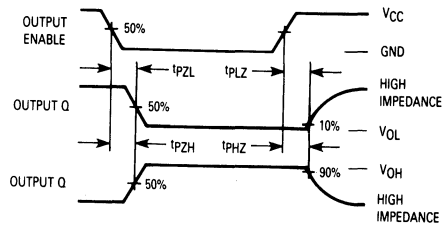


Figure 4.

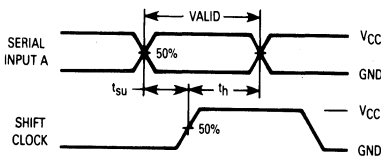


Figure 5.

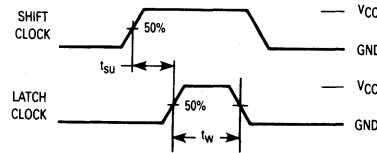
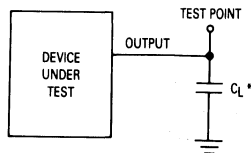


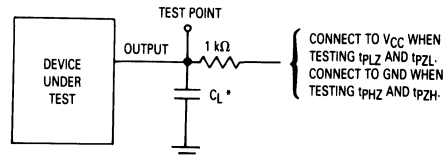
Figure 6.

## TEST CIRCUITS



\*Includes all probe and jig capacitance.

Figure 7.

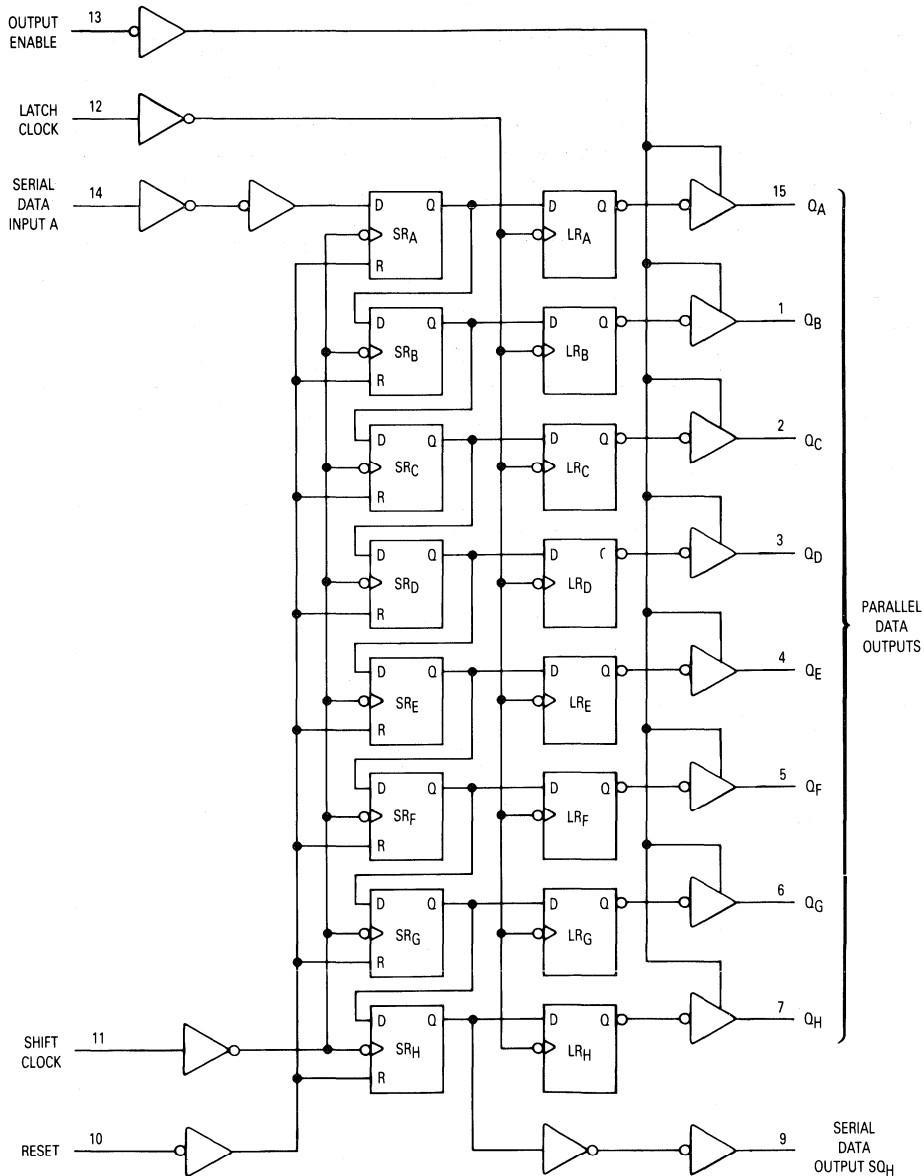


\*Includes all probe and jig capacitance.

Figure 8.

# MC54/74HC595A

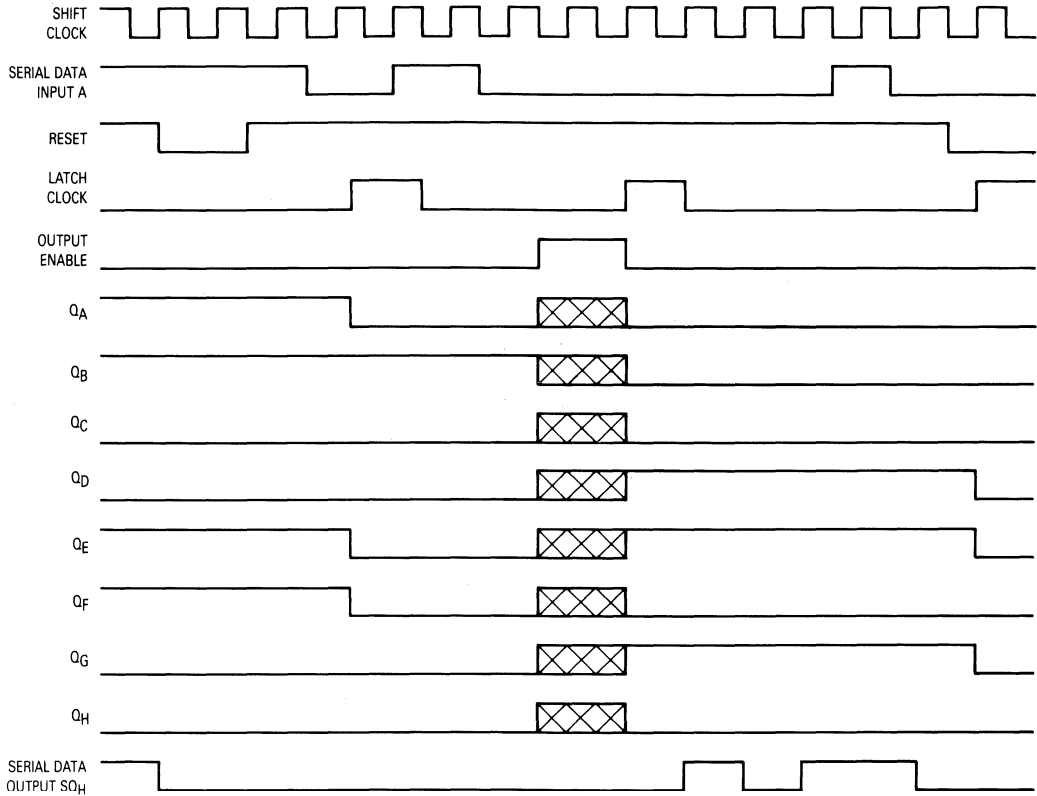
## EXPANDED LOGIC DIAGRAM



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# MC54/74HC595A

## TIMING DIAGRAM



5



# 8-Bit Serial or Parallel-Input/ Serial-Output Shift Register with Input Latch

## High-Performance Silicon-Gate CMOS

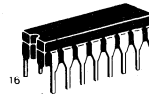
The MC54/74HC597 is identical in pinout to the LS597. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit input latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table).

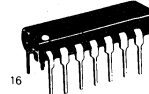
The HC597 is similar in function to the HC589, which is a 3-state device.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 516 FETs or 129 Equivalent Gates

### MC54/74HC597



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



**N SUFFIX  
 PLASTIC  
 CASE 648-08**



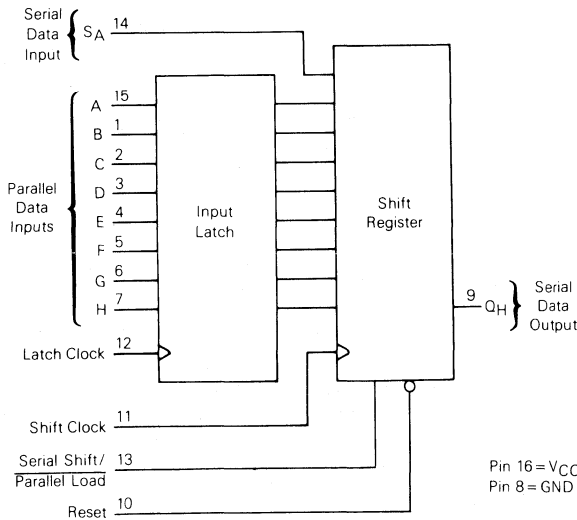
**D SUFFIX  
 SOIC  
 CASE 751B-04**

#### ORDERING INFORMATION

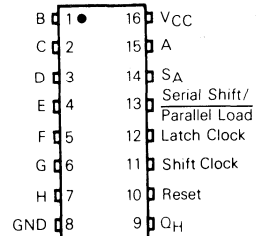
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### LOGIC DIAGRAM



#### PIN ASSIGNMENT



# MC54/74HC597

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0$ V 0 $V_{CC} = 4.5$ V 0 $V_{CC} = 6.0$ V 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out}  \leq 20$ $\mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out}  \leq 20$ $\mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0$ mA $ I_{out}  \leq 5.2$ mA	6.0	5.9	5.9	5.9	
			4.5	3.98	3.84	3.70	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0$ mA $ I_{out}  \leq 5.2$ mA	6.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
			6.0	8	80	160	
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ $\mu\text{A}$	6.0	8	80	160	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 4.

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# MC54/74HC597

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Clock to Q <sub>H</sub> (Figures 1 and 8)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Shift Clock to Q <sub>H</sub> (Figures 2 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q <sub>H</sub> (Figures 3 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Serial Shift/Parallel Load to Q <sub>H</sub> (Figures 4 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		50	

## PIN DESCRIPTIONS

### DATA INPUTS

**A, B, C, D, E, F, G, H (PINS 15, 1, 2, 3, 4, 5, 6, 7)** — Parallel data inputs. Data on these inputs is stored in the input latch on the rising edge of the Latch Clock input.

**S<sub>A</sub> (PIN 14)** — Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

### CONTROL INPUTS

**SERIAL SHIFT/PARALLEL LOAD (PIN 13)** — Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the input latch, and serial shifting is inhibited.

**RESET (PIN 10)** — Asynchronous, Active-low shift register reset. A low level applied to this input resets the shift register to a low level, but does not change the data in the input latch.

**SHIFT CLOCK (PIN 11)** — Serial shift register clock. A low-to-high transition on this input shifts data on the Serial Data Input into the shift register and data in stage H is shifted out Q<sub>H</sub>, being replaced by the data previously stored in stage G.

**LATCH CLOCK (PIN 12)** — Latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the input latch.

### OUTPUT

**Q<sub>H</sub> (PIN 9)** — Serial data output. This pin is the output from the last stage of the shift register.

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# MC54/74HC597

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>SU</sub>	Minimum Setup Time, Parallel Data Inputs A-H to Latch Clock (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>SU</sub>	Minimum Setup Time, Serial Data Input S <sub>A</sub> to Shift Clock (Figure 6)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>SU</sub>	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>H</sub>	Minimum Hold Time, Latch Clock to Parallel Data Inputs A-H (Figure 5)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t <sub>H</sub>	Minimum Hold Time, Shift Clock to Serial Data Input S <sub>A</sub> (Figure 6)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>REC</sub>	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>W</sub>	Minimum Pulse Width, Latch Clock and Shift Clock (Figures 1 and 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>W</sub>	Minimum Pulse Width, Reset (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>W</sub>	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

## FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Reset	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S <sub>A</sub>	Parallel Inputs A-H	Latch Contents	Shift Register Contents	Output Q <sub>H</sub>
Reset shift register	L	X	L, H,	X	X	X	U	L	L
Reset shift register; load parallel data into data latch	L	X		X	X	a-h	a-h	L	L
Load parallel data into data latch	H	H		L, H,	X	a-h	a-h	U	U
Transfer latch contents to shift register	H	L	L, H,	X	X	X	U	LR <sub>N</sub> → SR <sub>N</sub>	LR <sub>H</sub>
Contents of data latch and shift register are unchanged	H	H	L, H,	L, H,	X	X	U	U	U
Load parallel data into data latch and shift register	H	L		X	X	a-h	a-h	a-h	h
Shift serial data into shift register	H	H	X		D	X	*	SR <sub>A</sub> = D; SR <sub>N</sub> → SR <sub>N+1</sub>	SR <sub>G</sub> → SR <sub>H</sub>
Load parallel data into data latch and shift serial data into shift register	H	H			D	a-h	a-h	SR <sub>A</sub> = D; SR <sub>N</sub> → SR <sub>N+1</sub>	SR <sub>G</sub> → SR <sub>H</sub>

LR = latch register contents

SR = shift register contents

a-h = data at parallel data inputs A-H

D = data (L, H) at serial data input S<sub>A</sub>

U = remains unchanged

X = don't care

\* = depends on latch clock input

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# MC54/74HC597

## SWITCHING WAVEFORMS

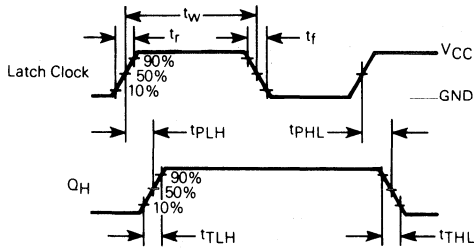


Figure 1. (Serial Shift/Parallel Load = L)

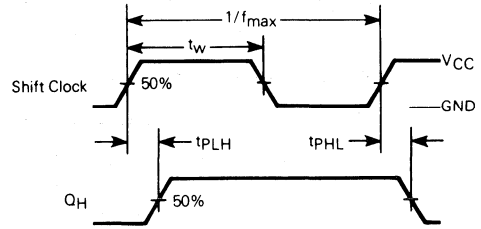


Figure 2. (Serial Shift/Parallel Load = H)

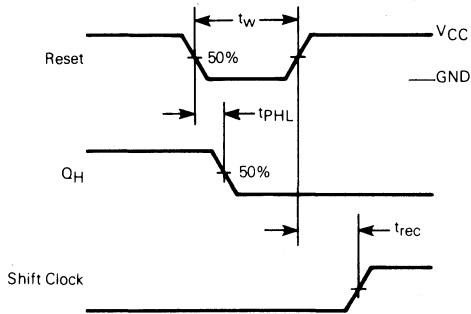


Figure 3.

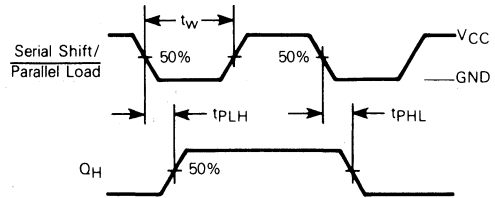


Figure 4.

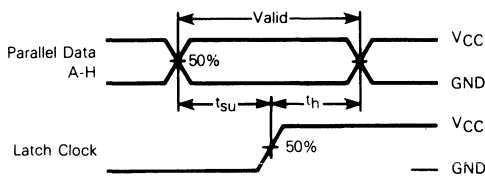


Figure 5.

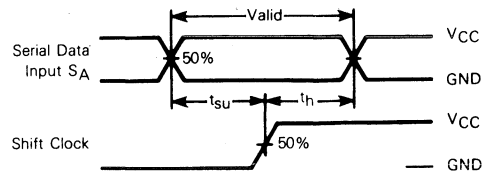


Figure 6.

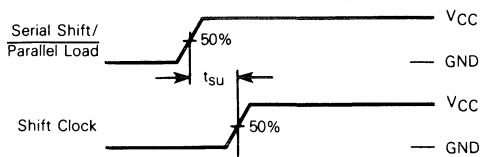
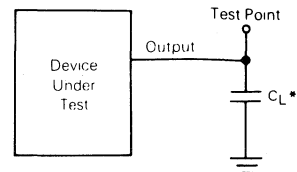


Figure 7.

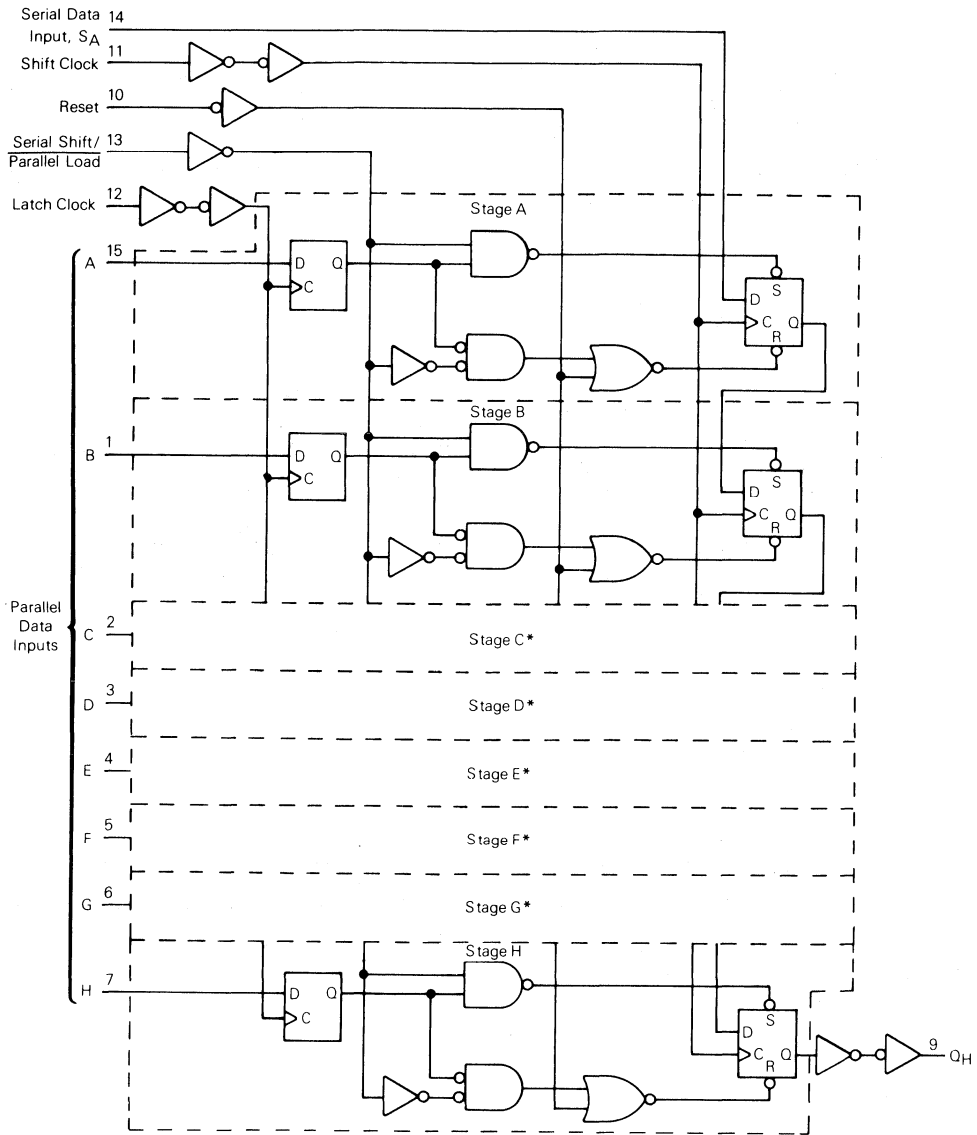


\* Includes all probe and jig capacitance.

8. Test Circuit

# MC54/74HC597

## EXPANDED LOGIC DIAGRAM

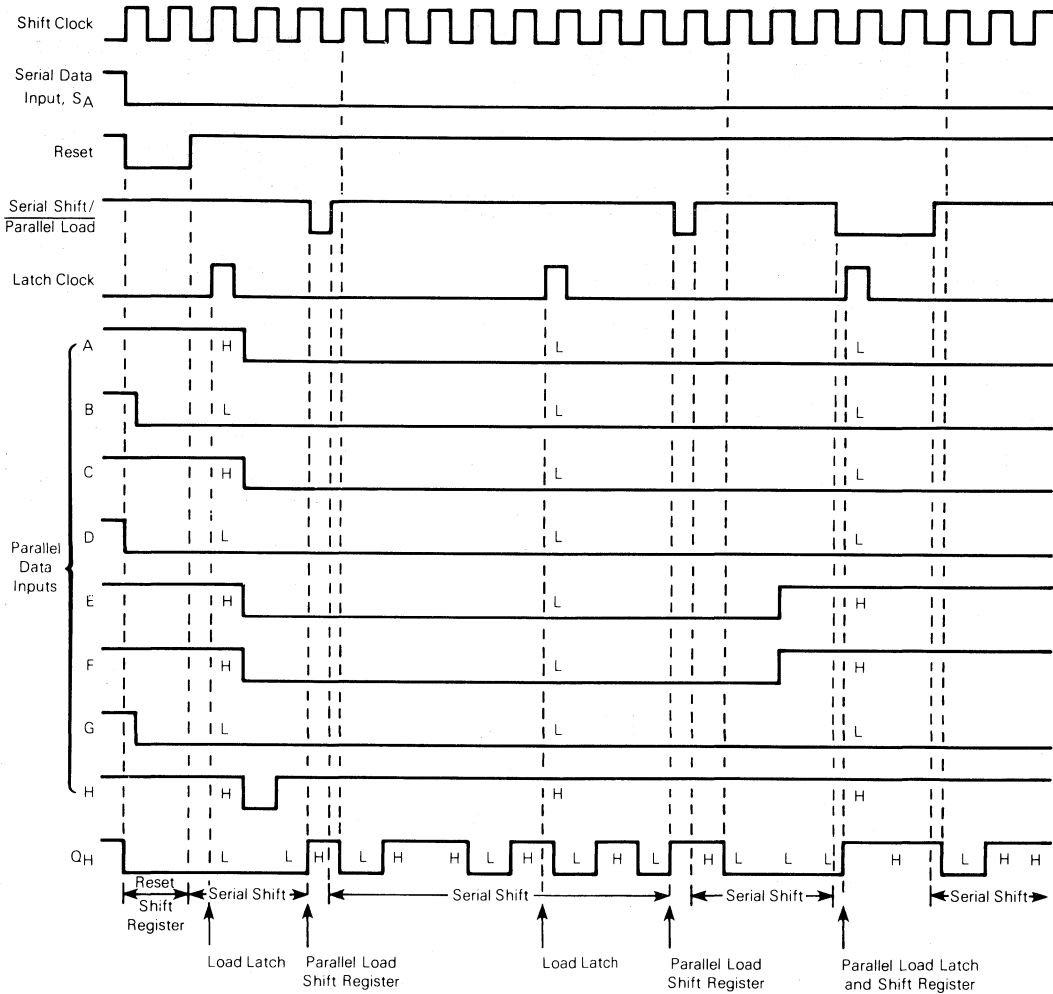


\* NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.

5

# MC54/74HC597

## TIMING DIAGRAM



## Octal 3-State Inverting Bus Transceiver

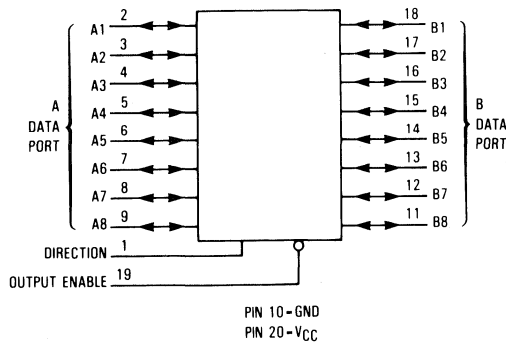
### High-Performance Silicon-Gate CMOS

The MC54/74HC640A is identical in pinout to the LS640. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

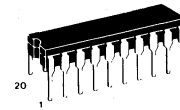
The HC640A is a 3-state transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 276 FETs or 69 Equivalent Gates

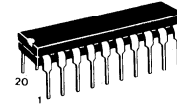
LOGIC DIAGRAM



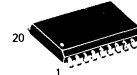
## MC54/74HC640A



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03



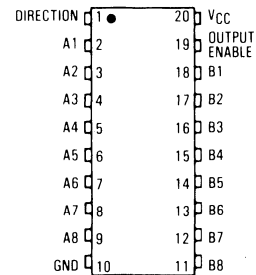
DW SUFFIX  
 SOIC  
 CASE 751D-03

### ORDERING INFORMATION

MC74HCXXXAN Plastic  
 MC54HCXXXAJ Ceramic  
 MC74HCXXXADW SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data transmitted from Bus B to Bus A (inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses isolated (High-Impedance State)

X = don't care



# MC54/74HC640A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>I/O</sub>	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>I/O</sub>	DC I/O Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND, Pin 1 or 19	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC640A

## DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Guaranteed Limit						Unit
			25°C to -55°C		≤85°C		≤125°C		
			Min	Max	Min	Max	Min	Max	
V <sub>IC+</sub>	V <sub>CC</sub> Input Diode Forward Voltage	V <sub>CC</sub> = 0 V, GND = Open I <sub>IN</sub> (each pin) = 100 μA	0.3	2.5	0.3	2.5	0.3	2.5	V
V <sub>IC-</sub>	GND Input Diode Forward Voltage	GND = 0 V, V <sub>CC</sub> = Open I <sub>IN</sub> (each pin) = -100 μA	-0.3	-2.5	-0.3	-2.5	-0.3	-2.5	V

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C		≤125°C	
			Min	Max	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	25	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance, Pin 1 or 19	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	—	15	15	15	pF

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub>	Typical (at 25°C, V <sub>CC</sub> = 5.0 V)	pF
		40	

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4.

5

## SWITCHING WAVEFORMS

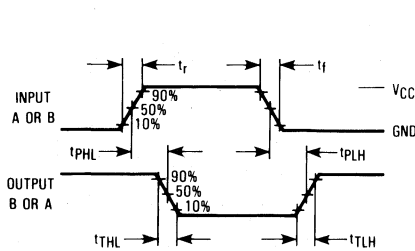


Figure 1

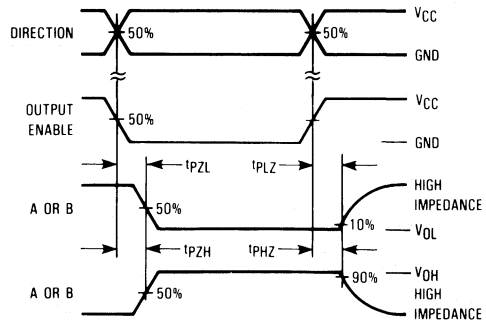
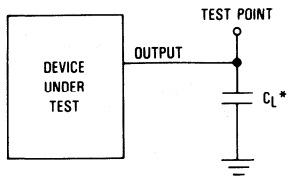


Figure 2

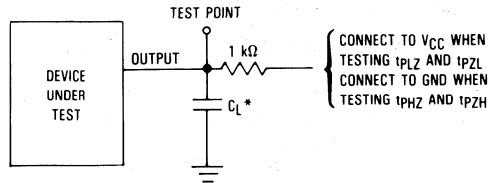
# MC54/74HC640A

## TEST CIRCUITS



\*Includes all probe and jig capacitance

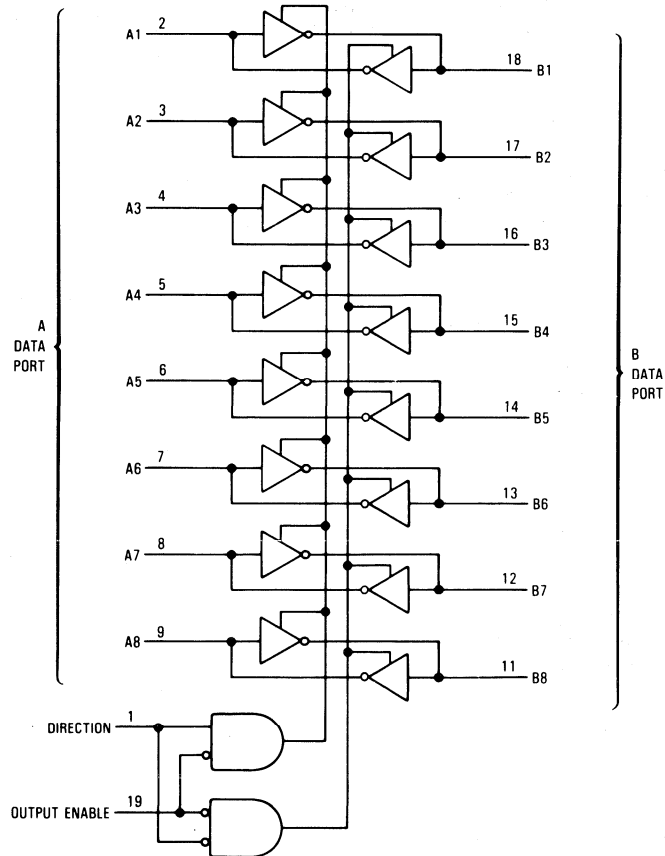
Figure 3.



\*Includes all probe and jig capacitance

Figure 4.

## EXPANDED LOGIC DIAGRAM



# Octal 3-State Bus Transceivers and D Flip-Flops

## High-Performance Silicon-Gate CMOS

The MC54/74HC646 is identical in pinout to the LS646. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

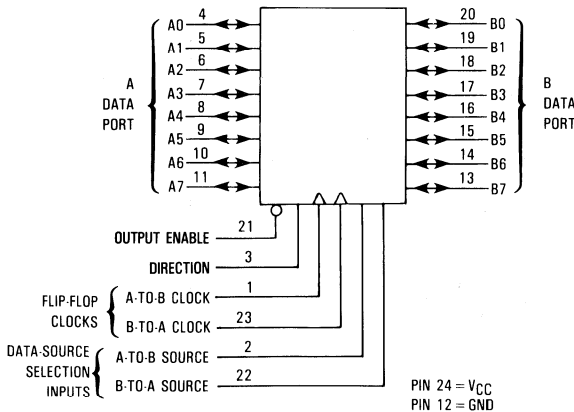
These devices are bus transceivers with D flip-flops. Depending on the status of the Data-Source Selection pins, data may be routed to the outputs either from the flip-flops or transmitted real-time from the inputs (see Function Table and Application Information).

The Output Enable and the Direction pins control the transceiver's function. Bus A and Bus B cannot be routed as outputs to each other simultaneously, but can be routed as inputs to the A and B flip-flops. Also, the A and B flip-flops can be routed as outputs to Bus A and Bus B simultaneously. Additionally, when either or both of the ports are in the high-impedance state, these I/O pins may be used as inputs to the D flip-flops for data storage.

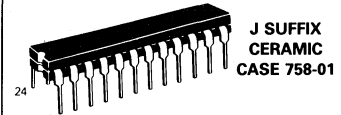
The user should note that because the clocks are not gated with the Direction and Output Enable pins, data at the A and B ports may be clocked into the storage flip-flops at any time.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 780 FETs or 195 Equivalent Gates

**LOGIC DIAGRAM**



## MC54/74HC646

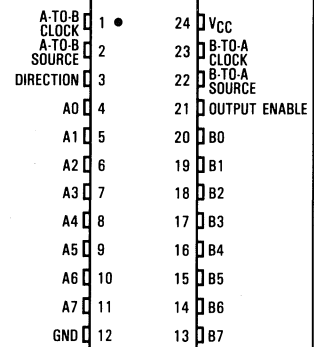


### ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



# MC54/74HC646

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>I/O</sub>	DC I/O Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>I/O</sub>	DC I/O Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260	°C
		300	

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	6.0	5.9	5.9	5.9	
			4.5	3.98	3.84	3.70	
6.0	5.48	5.34	5.20				
	V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1
4.5				0.1	0.1	0.1	
V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA			6.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.40	
6.0	0.26	0.33	0.40				
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND (Pins 1, 2, 3, 21, 22, and 23)	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND, I/O Pins	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC646

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 3, 4 and 9)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output B (or Input B to Output A) (Figures 1, 2 and 9)	2.0	170	215	255	ns
		4.5	34	43	51	
		6.0	29	37	43	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A-to-B Clock to Output B (or B-to-A Clock to Output A) (Figures 3, 4 and 9)	2.0	220	275	330	ns
		4.5	44	55	66	
		6.0	37	47	56	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A-to-B Source to Output B (or B-to-A Source to Output A) (Figures 5, 6 and 9)	2.0	170	215	255	ns
		4.5	34	43	51	
		6.0	29	37	43	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Direction or Output Enable to Output A or B (Figures 7, 8 and 10)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Direction or Output Enable to Output A or B (Figures 7, 8 and 10)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 9)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		60	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Input A to A-to-B Clock (or Input B to B-to-A Clock) (Figures 3 and 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, A-to-B Clock to Input A (or B-to-A Clock to Input B) (Figures 3 and 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, A-to-B Clock (or B-to-A Clock) (Figures 3 and 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC646

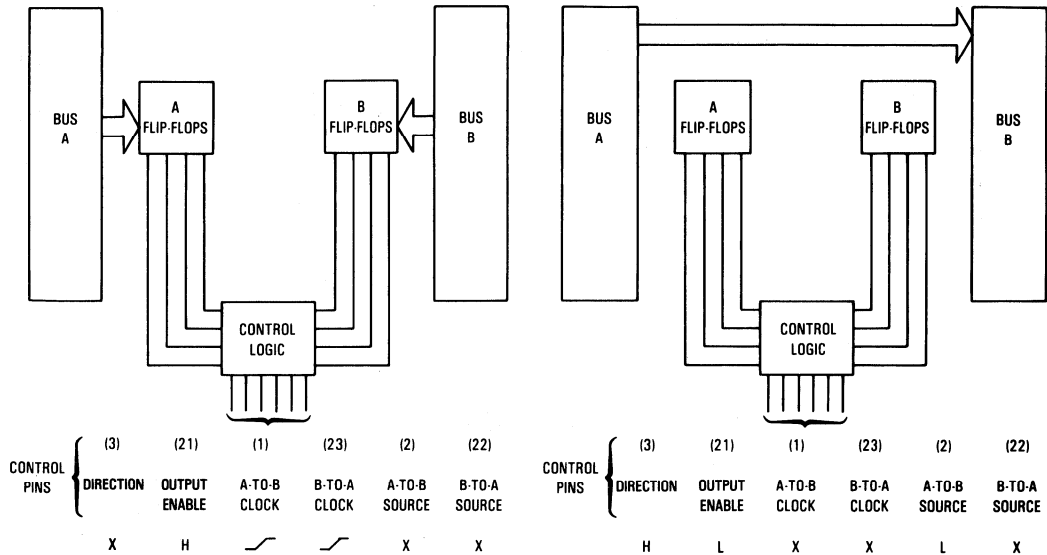
## FUNCTION TABLE - HC646

Control Inputs						Data Port Status		Storage Flip-Flop States		Description of Operation
Output Enable	Direction	A-to-B Clock	B-to-A Clock	A-to-B Source	B-to-A Source	A	B	Q <sub>A</sub>	Q <sub>B</sub>	
H	X	H, L,	H, L,	X	X	Input: X	Input: X	no change	no change	The output functions of the A and B ports are disabled.
				X	X	L H X X	X X L H	L H X X	X X L H	The ports may be used as inputs to the storage flip-flops. Data at the inputs are clocked into the flip-flops with the rising edge of the Clocks.
L	H	H, L,	X*	L	X	L H	L H	no change no change	no change no change	The output mode of the B data port is enabled and behaves according to the following logic equation:  $B = [A \cdot (\overline{A\text{-to-B Source}})] + [Q_A \cdot (A\text{-to-B Source})]$ 1.) When A-to-B Source is low, the data at the A data port are displayed at the B data port. The states of the storage flip-flops are not affected.
				H	X	X	Q <sub>A</sub>	no change	no change	2.) When A-to-B Source is high, the states of the A storage flip-flops are displayed at the B data port.
			X*	L	X	L H	L H	L H	no change no change	3.) When A-to-B Source is low, the data at the A data port are clocked into the A storage flip-flops by a rising-edge signal on the A-to-B Clock.
				H	X	L H	Q <sub>A</sub> Q <sub>A</sub>	L H	no change no change	4.) When A-to-B Source is high, the data at the A data port are clocked into the A storage flip-flops by a rising-edge signal on the A-to-B Clock. The states, Q <sub>A</sub> , of the storage flip-flops propagate directly to the B data port.
L	L	X*	H, L,	X	L	L H	L H	no change no change	no change no change	The output mode of the A data port is enabled and behaves according to the following logic equation:  $A = [B \cdot (\overline{B\text{-to-A Source}})] + [Q_B \cdot (B\text{-to-A Source})]$ 1.) When B-to-A Source is low, the data at the B data port are displayed at the A data port. The states of the storage flip-flops are not affected.
				X	H	Q <sub>B</sub>	X	no change	no change	2.) When B-to-A Source is high, the states of the B storage flip-flops are displayed at the A data port.
		X*		X	L	L H	L H	no change no change	L H	3.) When B-to-A Source is low, the data at the B data port are clocked into the B storage flip-flops by a rising-edge signal on the B-to-A Clock.
				X	H	Q <sub>B</sub> Q <sub>B</sub>	L H	no change no change	L H	4.) When B-to-A Source is high, the data at the B data port are clocked into the B storage flip-flops by a rising-edge signal on the B-to-A Clock. The states, Q <sub>B</sub> , of the storage flip-flops propagate directly to the A data port.

\*The clocks are not internally gated with either the Output Enables or the Source inputs. Therefore, data at the A and B ports may be clocked into the storage flip-flops at any time.

# MC54/74HC646

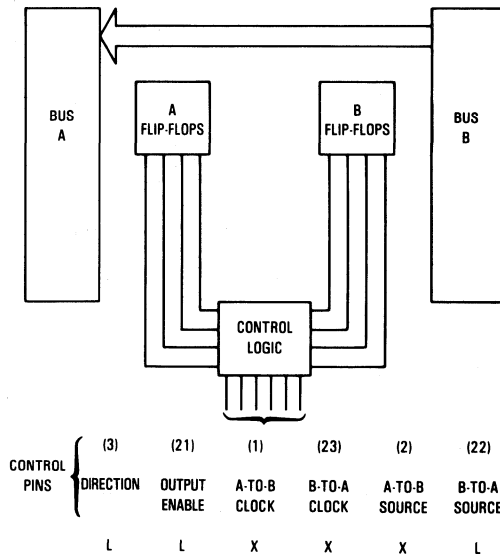
## TYPICAL APPLICATIONS



Data Storage From A and/or B Bus

Real-Time Transfer From Bus A to Bus B

5



Real-Time Transfer From Bus B to Bus A



# MC54/74HC646

## TIMING DIAGRAMS AND SWITCHING DIAGRAMS — HC646

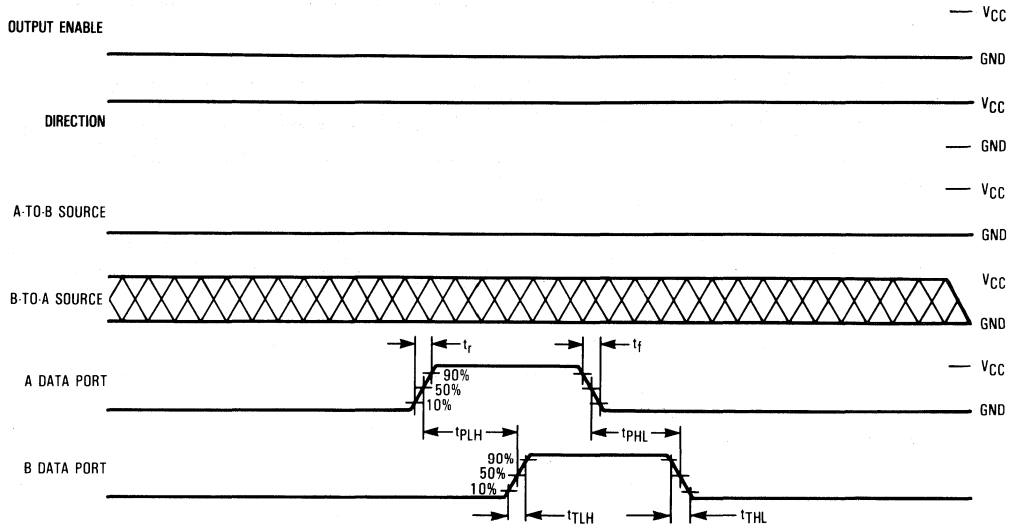


Figure 1. A Data Port = Input, B Data Port = Output

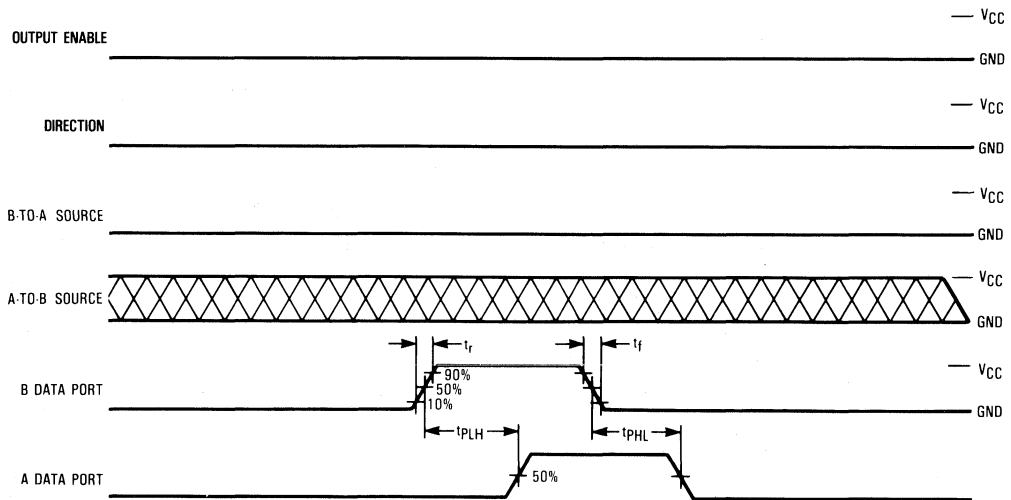


Figure 2. A Data Port = Output, B Data Port = Input

NOTE:  = Don't Care State

# MC54/74HC646

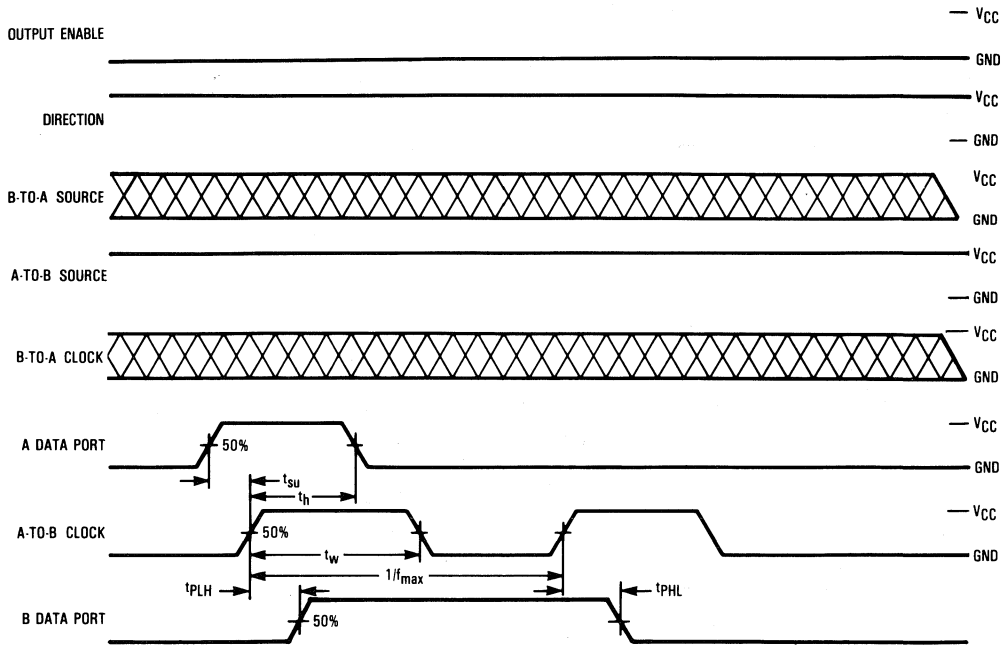


Figure 3. A Data Port = Input, B Data Port = Output

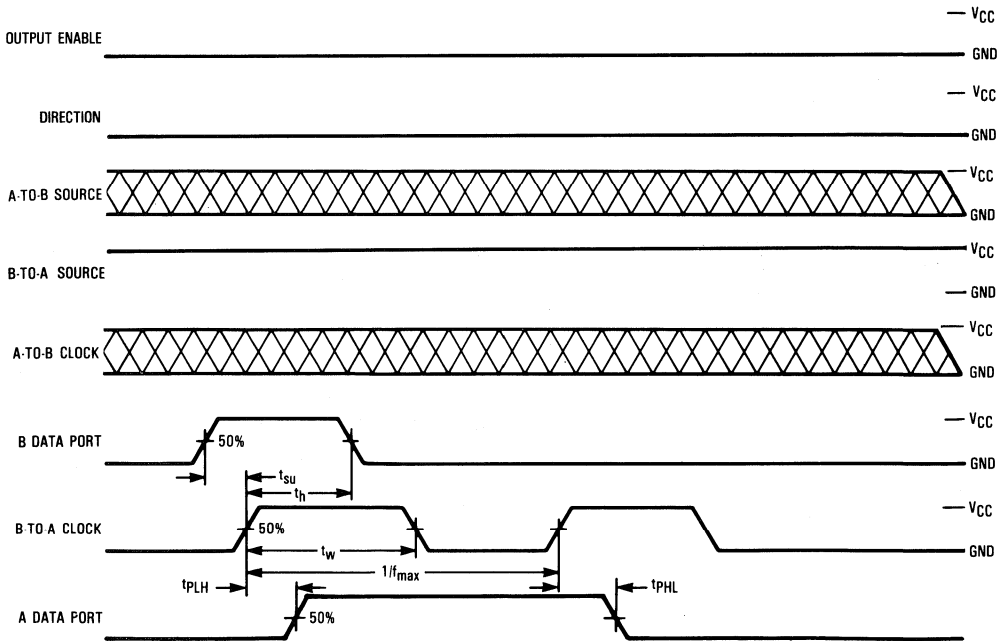
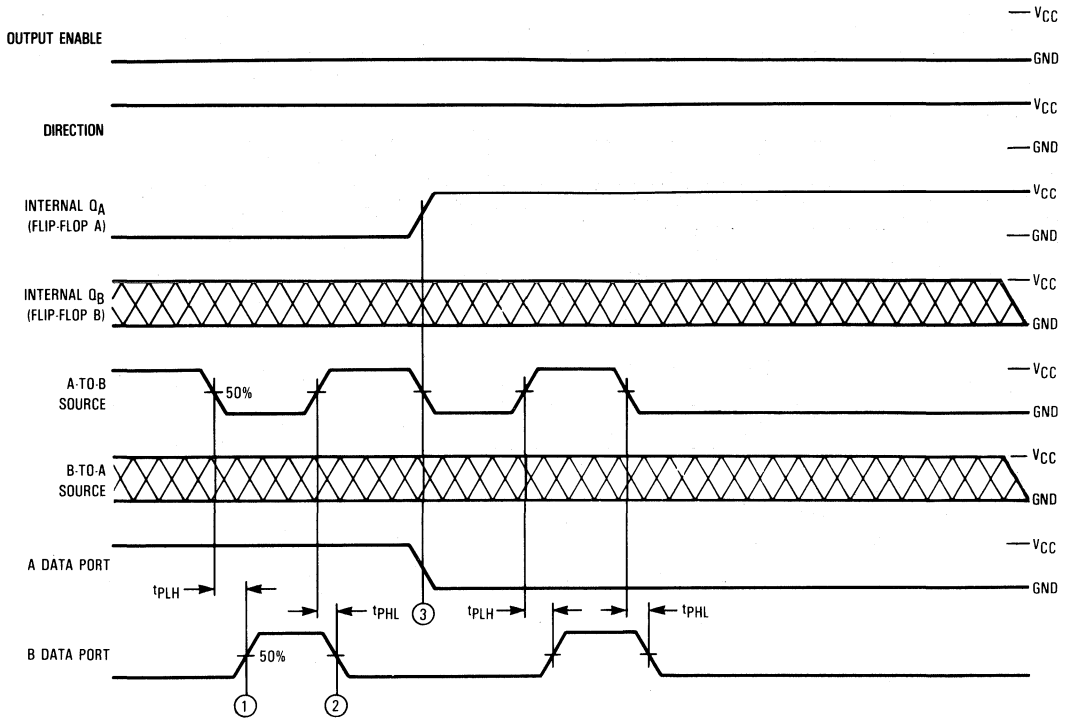


Figure 4. B Data Port = Input, A Data Port = Output

5

# MC54/74HC646

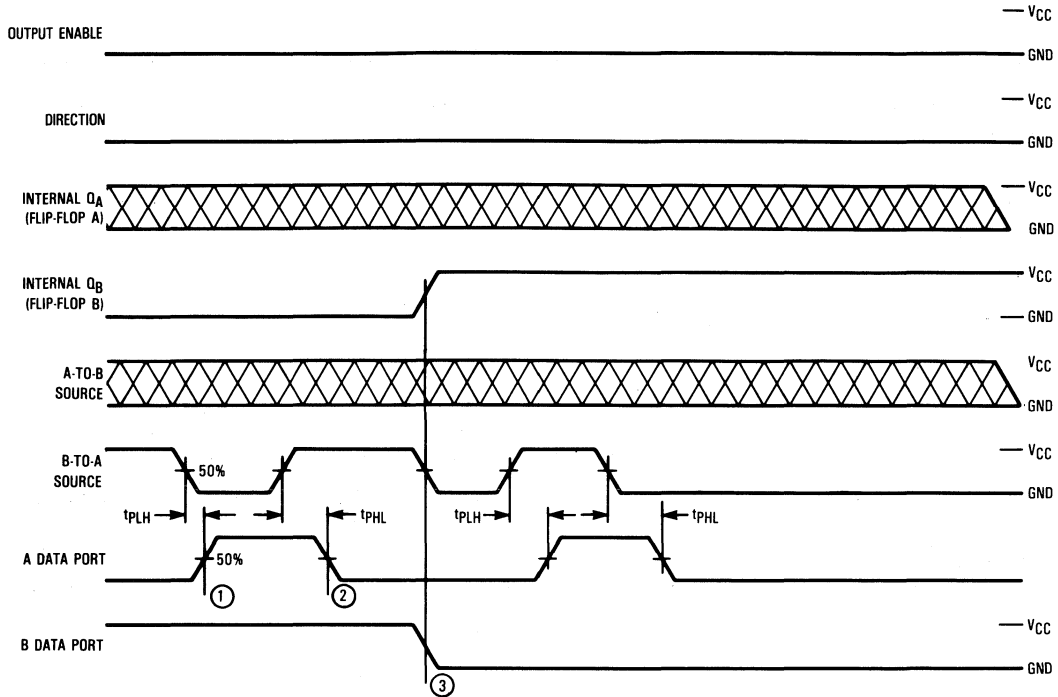


**NOTES:**

1. B Data Port (output) changes from the level of the storage flip-flop,  $Q_A$ , to the level of A Data Port (input).
2. B Data Port (output) changes from the level of A Data Port (input) to the level of the storage flip-flop,  $Q_A$ .
3. The A storage flip-flop, A-to-B Source, and A Data Port (input) have simultaneously changed states.

**Figure 5. A Data Port = Input, B Data Port = Output**

# MC54/74HC646



**NOTES:**

1. A Data Port (output) changes from the level of the storage flip-flop,  $Q_B$ , to the level of B Data Port (input).
2. A Data Port (output) changes from the level of B Data Port (input) to the level of storage flip-flop,  $Q_B$ .
3. The B storage flip-flop, B-to-A Source, and B Data Port (input) have simultaneously changed states for the purpose of this example. A Data Port (output) is now displaying the voltage level of B Data Port (input).

**Figure 6. A Data Port = Output, B Data Port = Input**

**5**

## PIN DESCRIPTIONS

### INPUTS/OUTPUTS

**A0-A7 (PINS 4-11) and B0-B7 (PINS 20-27)** — A and B data ports. These pins may function either as inputs to or outputs from the transceivers.

### CONTROL INPUTS

**OUTPUT ENABLE (PIN 21)** — Active-low output enable. When this pin is low, the outputs are enabled and function normally. When this pin is high, the A and B data ports are in high-impedance states. See the Function Table.

**DIRECTION (PIN 3)** — Data direction control. When the Output Enable pin is low, this control pin determines the direction of data flow. When Direction is high, the A data

ports are inputs and the B data ports are outputs. When Direction is low, the A data ports are outputs and the B data ports are inputs.

**A-TO-B CLOCK, B-TO-A CLOCK (PINS 1, 23)** — Clocks for the internal D flip-flops. With a low-to-high transition on the appropriate Clock pin, data on the A (or B) inputs are clocked into the internal A (or B) flip-flops. These clocks are not internally gated with the Output Enable or the Direction pins, therefore data at the A and B pins may be clocked into the storage flip-flops at any time.

**A-TO-B SOURCE, B-TO-A SOURCE (PINS 2, 22)** — Data-source selection pins. Depending upon the states of these pins (see the Function Table), data at the outputs may come either from the inputs or from the D flip-flops.

# MC54/74HC646

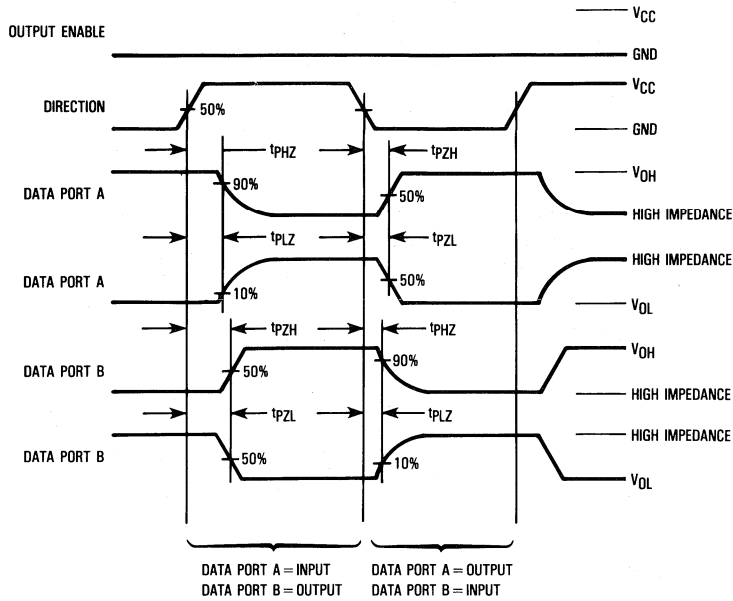


Figure 7

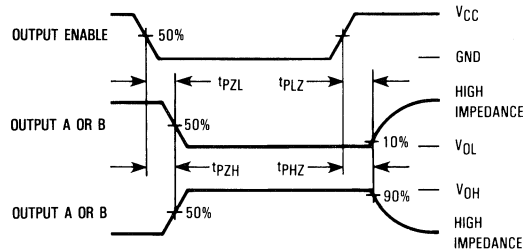
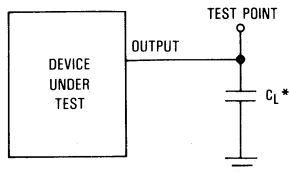
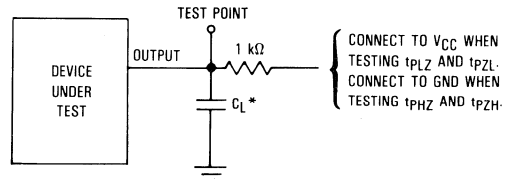


Figure 8



\*Includes all probe and jig capacitance.

Figure 9. Test Circuit

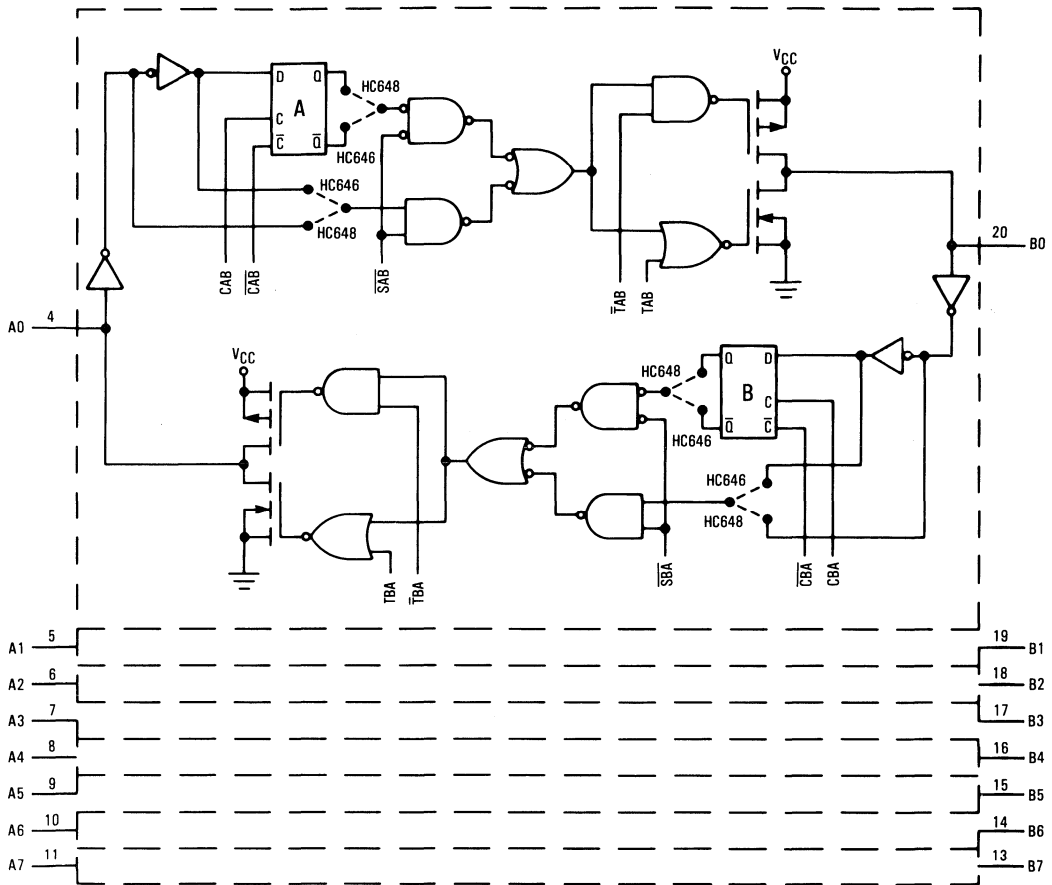


\*Includes all probe and jig capacitance.

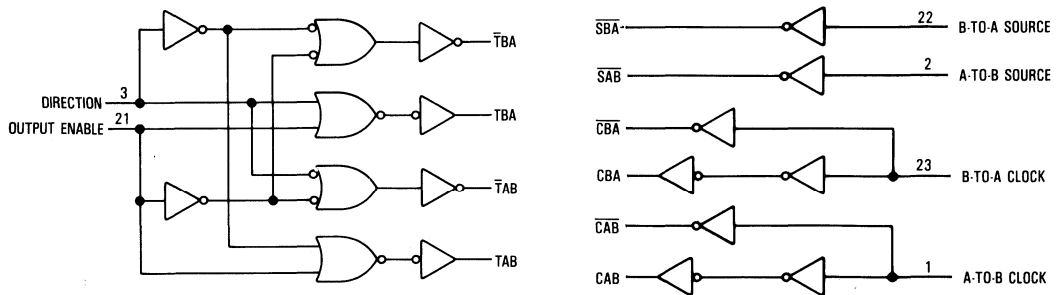
Figure 10. Test Circuit

# MC54/74HC646

## LOGIC DETAIL



5



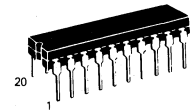
**MC54/74HC688**

**8-Bit Equality Comparator**  
**High-Performance Silicon-Gate CMOS**

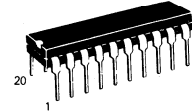
The MC54/74HC688 is identical in pinout to the LS688. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC688 compares two 8-bit binary or BCD words and indicates whether or not they are equal. By using the Cascade Input, two or more of the devices may be cascaded to compare words of more than 8 bits.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 116 FETs or 29 Equivalent Gates



**J SUFFIX**  
**CERAMIC**  
**CASE 732-03**



**N SUFFIX**  
**PLASTIC**  
**CASE 738-03**



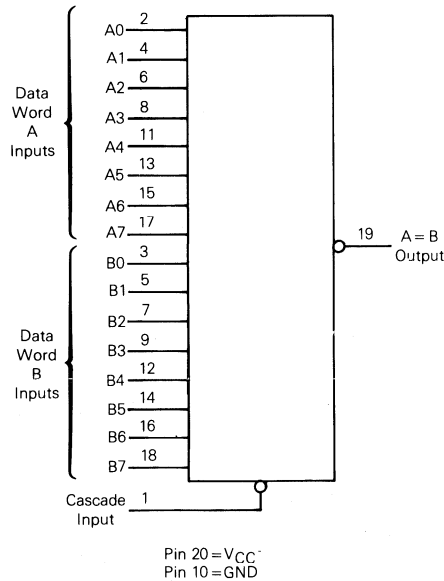
**DW SUFFIX**  
**SOIC**  
**CASE 751D-03**

**ORDERING INFORMATION**

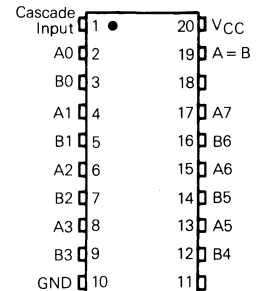
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs		Output
Data Words	Cascade	A = B
A = B	L	L
A > B	L	H
A < B	L	H
X	H	H

# MC54/74HC688

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level. (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	2.0	0.1	0.1	0.1	μA
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	2.0	0.26	0.33	0.40	μA
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
			6.0	8	80	160	
			6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HC688

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output A = B (Figures 1 and 3)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Cascade Input to Output A = B (Figures 2 and 3)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		30	

## SWITCHING WAVEFORMS

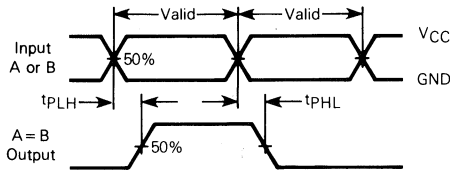


Figure 1.

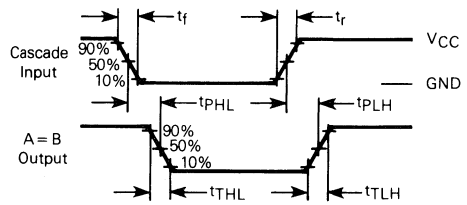
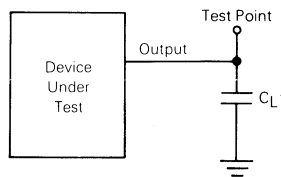


Figure 2.

## TEST CIRCUIT



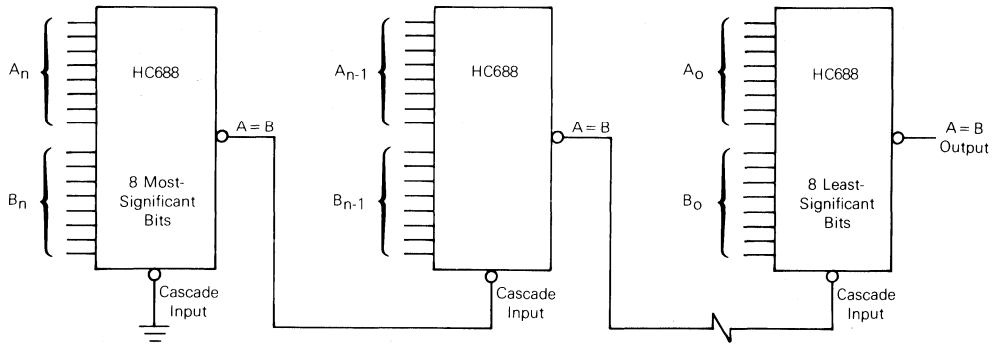
\* Includes all probe and jig capacitance.

Figure 3.

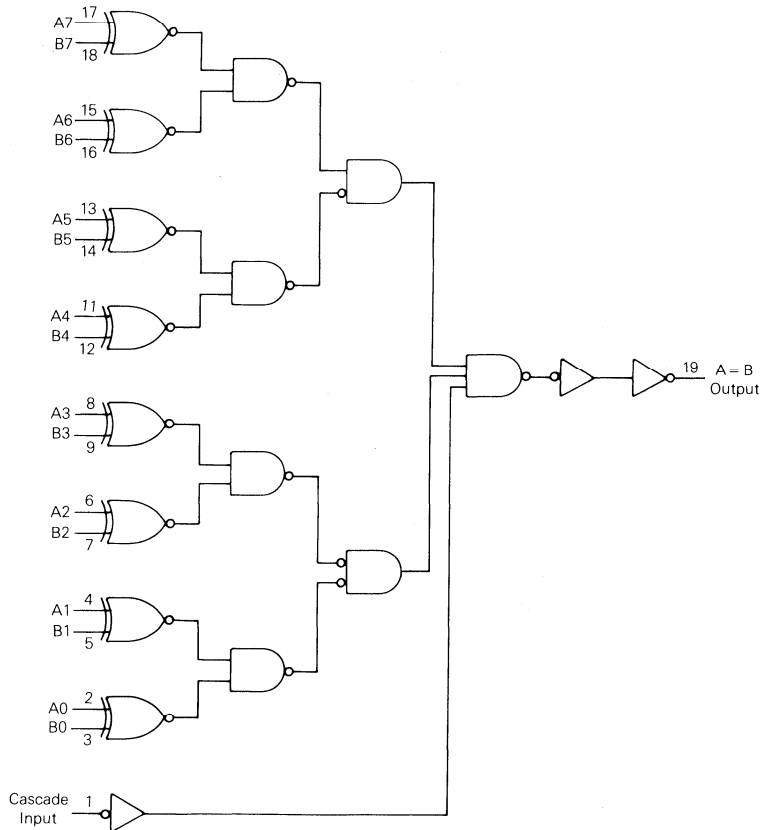
# MC54/74HC688

## TYPICAL APPLICATION

Two or more HC688 8-bit Equality Comparators may be cascaded to compare binary or BCD numbers having more than 8 bits. One method of accomplishing this is shown here.



## EXPANDED LOGIC DIAGRAM



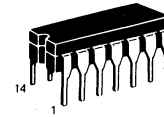
5

**MC54/74HC4002**

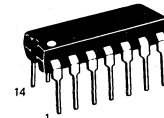
**Dual 4-Input NOR Gate**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC4002 is identical in pinout to the MC14002B and MC14002UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 28 FETs or 7 Equivalent Gates



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



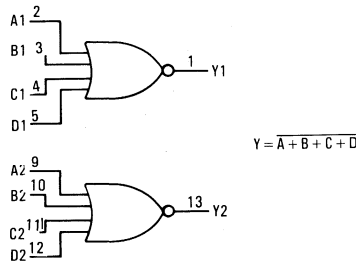
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

**ORDERING INFORMATION**

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

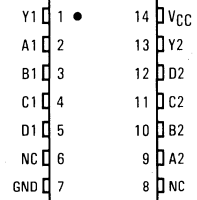
$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

**LOGIC DIAGRAM**



PIN 14 =  $V_{CC}$   
 PIN 7 = GND  
 PINS 6, 8 = NO CONNECTION

**PIN ASSIGNMENT**



NC = NO CONNECTION

**FUNCTION TABLE**

Inputs				Output
A	B	C	D	Y
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

X = don't care

# MC54/74HC4002

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	2.0	0.1	0.1	0.1	μA
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	2.0	0.26	0.33	0.40	μA
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC4002

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		26	

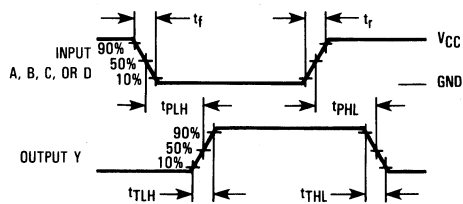
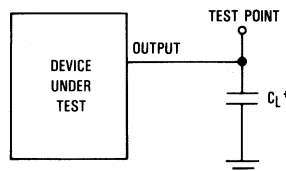


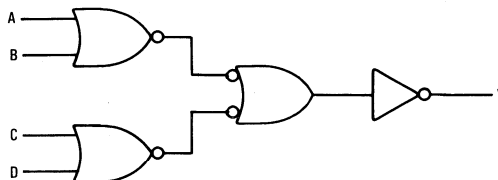
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM (1/2 of the Device)



## Quad Analog Switch/ Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

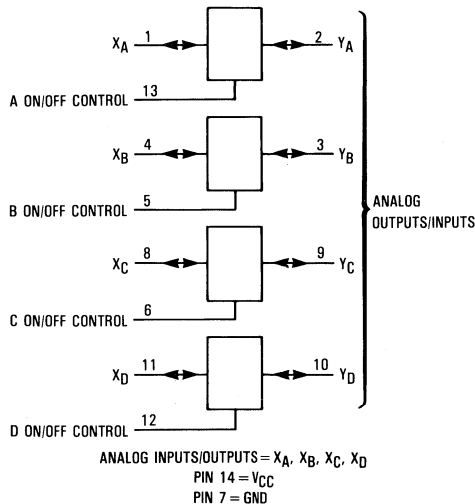
The MC54/74HC4016 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from  $V_{CC}$  to GND).

The HC4016 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances ( $R_{ON}$ ) are much more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

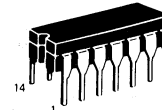
This device is identical in both function and pinout to the HC4066. The ON/OFF Control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316. For analog switches with lower  $R_{ON}$  characteristics, use the HC4066.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Analog Input Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 32 FETs or 8 Equivalent Gates

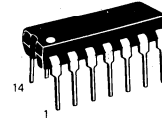
**LOGIC DIAGRAM**



### MC54/74HC4016



**J SUFFIX**  
**CERAMIC**  
 CASE 632-08



**N SUFFIX**  
**PLASTIC**  
 CASE 646-06



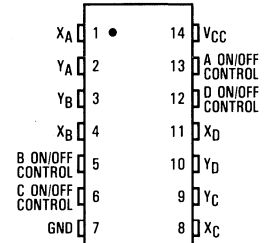
**D SUFFIX**  
**SOIC**  
 CASE 751A-02

#### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

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## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND)	-0.5 to +14.0	V
V <sub>IS</sub>	Analog Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>in</sub>	Digital Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
I	DC Current Into or Out of Any Pin	±25	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750	mW
		500	
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C
		300	

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V	
V <sub>IS</sub>	Analog Input Voltage (Referenced to GND)	GND	V <sub>CC</sub>	V	
V <sub>in</sub>	Digital Input Voltage (Referenced to GND)	GND	V <sub>CC</sub>	V	
V <sub>IO</sub> *	Static or Dynamic Voltage Across Switch	-	1.2	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)			ns	
		V <sub>CC</sub> = 2.0 V	0		1000
		V <sub>CC</sub> = 4.5 V	0		500
		V <sub>CC</sub> = 9.0 V	0		400
		V <sub>CC</sub> = 12.0 V	0		250

\*For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn, i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Voltage ON/OFF Control Inputs	R <sub>ON</sub> = per spec	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			9.0	6.3	6.3	6.3	
			12.0	8.4	8.4	8.4	
V <sub>IL</sub>	Maximum Low-Level Voltage ON/OFF Control Inputs	R <sub>ON</sub> = per spec	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			9.0	1.8	1.8	1.8	
			12.0	2.4	2.4	2.4	
I <sub>in</sub>	Maximum Input Leakage Current, ON/OFF Control Inputs	V <sub>in</sub> = V <sub>CC</sub> or GND	12.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND V <sub>IO</sub> = 0 V	6.0	2	20	40	μA
			12.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.

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## DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
R <sub>ON</sub>	Maximum "ON" Resistance	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to GND I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0†	—	—	—	Ω
			4.5	320	400	480	
			9.0	170	215	255	
			12.0	170	215	255	
		V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Endpoints) I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0	—	—	—	
			4.5	180	225	270	
			9.0	135	170	205	
			12.0	135	170	205	
ΔR <sub>ON</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - GND) I <sub>S</sub> ≤ 2.0 mA	2.0	—	—	—	Ω
			4.5	30	35	40	
			9.0	20	25	30	
			12.0	20	25	30	
I <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> V <sub>IO</sub> = V <sub>CC</sub> or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I <sub>on</sub>	Maximum On-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V<sub>CC</sub> - GND) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 4.

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, ON/OFF Control Inputs: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0	50	65	75	ns
		4.5	10	13	15	
		9.0	10	13	15	
		12.0	10	13	15	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	150	190	225	ns
		4.5	30	38	45	
		9.0	30	38	45	
		12.0	30	38	45	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	125	160	185	ns
		4.5	25	32	37	
		9.0	25	32	37	
		12.0	25	32	37	
C	Maximum Capacitance	ON/OFF Control Input	—	10	10	pF
		Control Input = GND	—	—	—	
		Analog I/O Feedthrough	—	35 1.0	35 1.0	

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Switch) (Figure 13) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		15	



# MC54/74HC4016

## ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND unless noted)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f <sub>in</sub> = 1 MHz Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub> Increase f <sub>in</sub> Frequency Until dB Meter Reads -3 dB R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off-Channel Feedthrough Isolation (Figure 6)	f <sub>in</sub> = Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	-50 -50 -50 -40 -40 -40	dB
—	Feedthrough Noise, Control to Switch (Figure 7)	V <sub>in</sub> ≤ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns) Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	60 130 200 30 65 100	mV <sub>pp</sub>
—	Crosstalk Between Any Two Switches (Figure 12)	f <sub>in</sub> = Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	-70 -70 -70 -80 -80 -80	dB
THD	Total Harmonic Distortion (Figure 14)	f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF THD = THD <sub>Measured</sub> - THD <sub>Source</sub> V <sub>IS</sub> = 4.0 V <sub>pp</sub> sine wave V <sub>IS</sub> = 8.0 V <sub>pp</sub> sine wave V <sub>IS</sub> = 11.0 V <sub>pp</sub> sine wave	4.5 9.0 12.0	0.10 0.06 0.04	%

\*Guaranteed limits not tested. Determined by design and verified by qualification.

# MC54/74HC4016

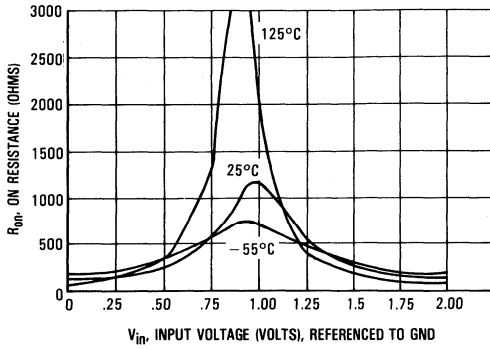


Figure 1a. Typical On Resistance,  $V_{CC} = 2.0$  V

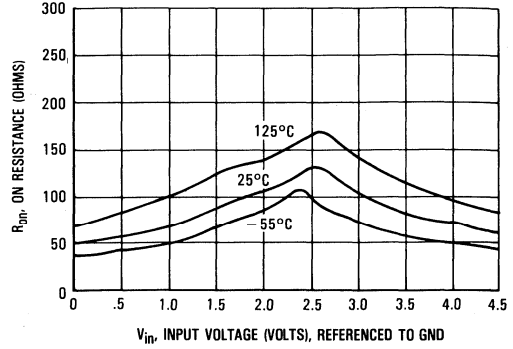


Figure 1b. Typical On Resistance,  $V_{CC} = 4.5$  V

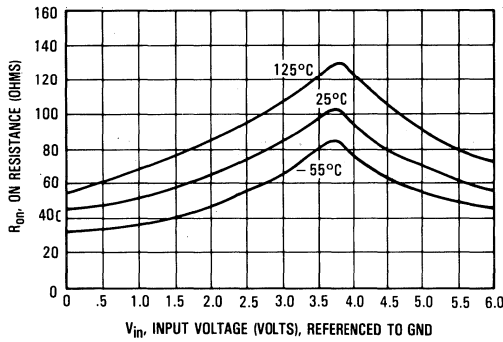


Figure 1c. Typical On Resistance,  $V_{CC} = 6.0$  V

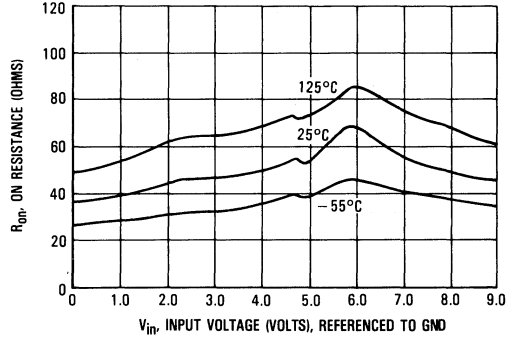


Figure 1d. Typical On Resistance,  $V_{CC} = 9.0$  V

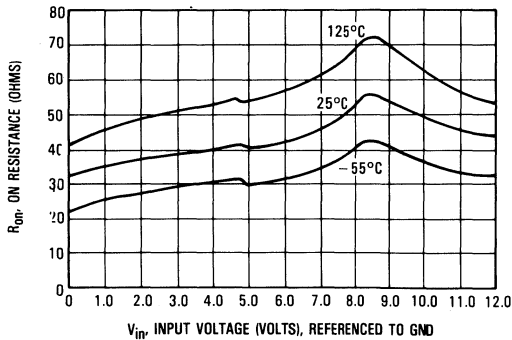


Figure 1e. Typical On Resistance,  $V_{CC} = 12.0$  V

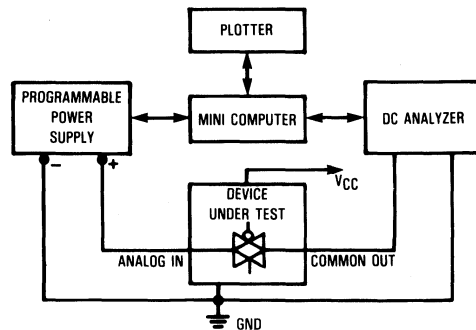


Figure 2. On Resistance Test Set-Up

# MC54/74HC4016

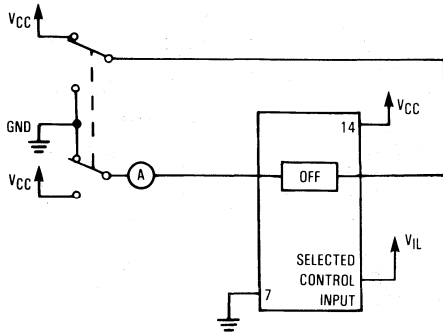


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

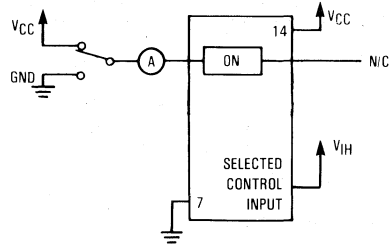
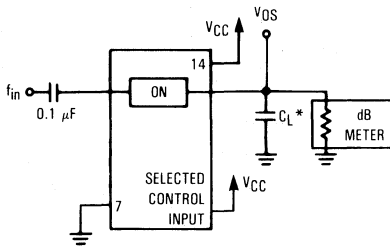
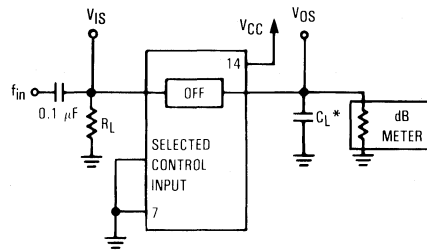


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



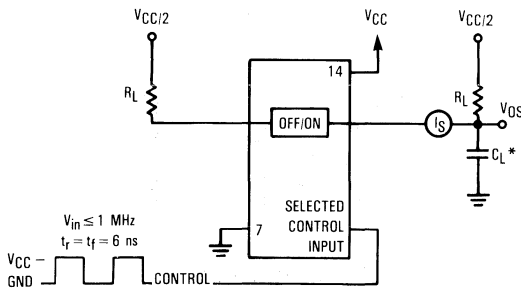
\*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth Test Set-Up



\*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

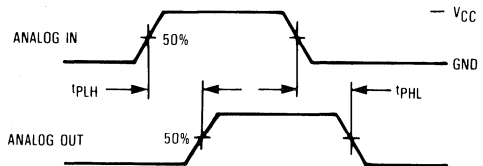
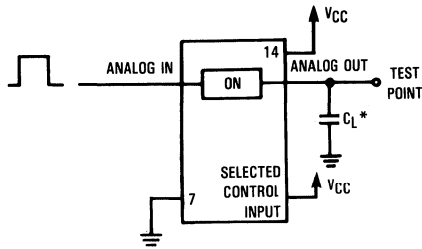


Figure 8. Propagation Delays, Analog In to Analog Out



\*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

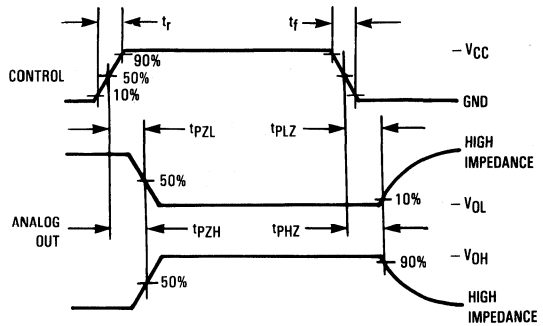
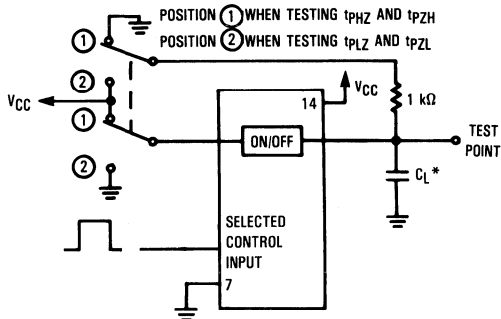
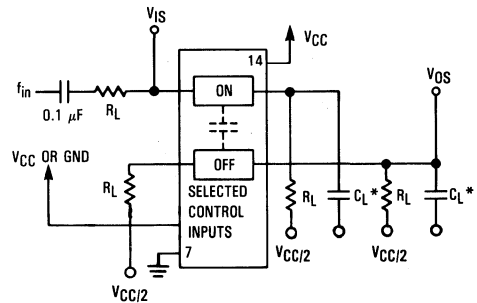


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



\*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



\*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

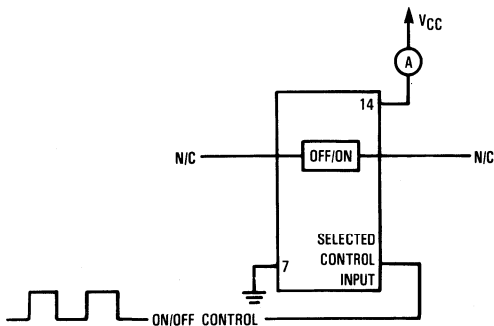
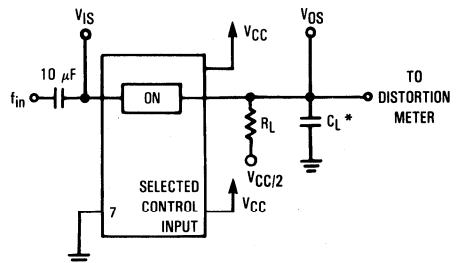


Figure 13. Power Dissipation Capacitance Test Set-Up



\*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

5

# MC54/74HC4016

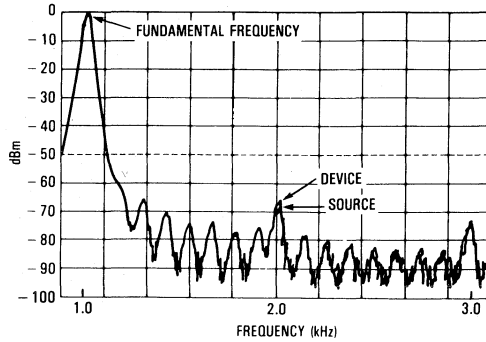


Figure 15. Plot, Harmonic Distortion

## APPLICATION INFORMATION

The ON/OFF Control pins should be at  $V_{CC}$  or GND logic levels,  $V_{CC}$  being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and GND. The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below GND. In the example below,

the difference between  $V_{CC}$  and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above  $V_{CC}$  and/or below GND are anticipated on the analog channels, external diodes ( $D_x$ ) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the  $D_x$  diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear-out mechanism.

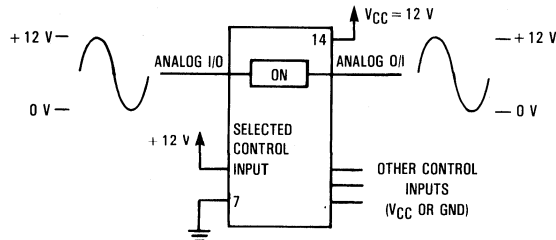


Figure 16. 12 V Application

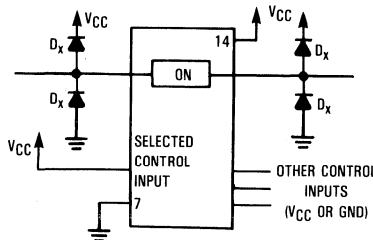


Figure 17. Transient Suppressor Application

# MC54/74HC4016

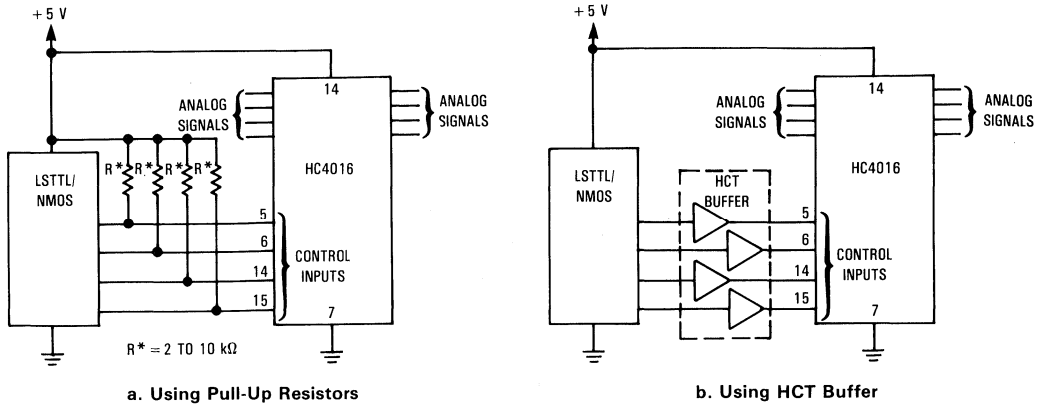


Figure 18. LSTTL/NMOS to HCMOS Interface

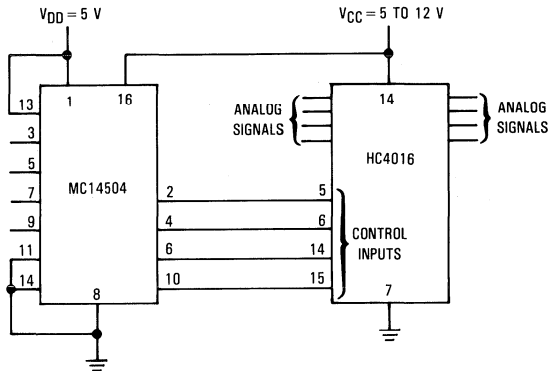


Figure 19. TTL/NMOS-to-CMOS Level Converter  
Analog Signal Peak-to-Peak Greater than 5 V  
(Also see HC4316)

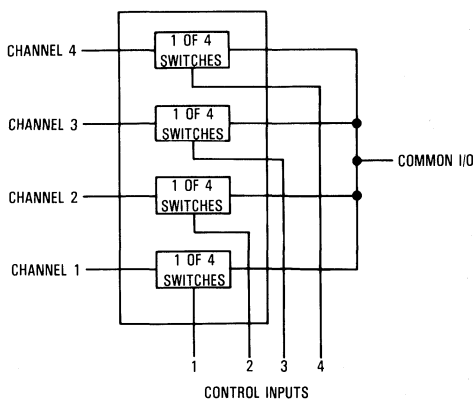


Figure 20. 4-Input Multiplexer

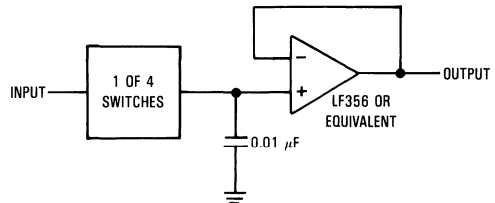


Figure 21. Sample/Hold Amplifier

5

## Decade Counter

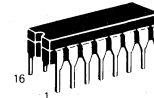
### High-Performance Silicon-Gate CMOS

The MC54/74HC4017 is identical in pinout to the standard CMOS MC14017B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

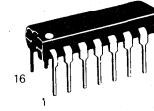
The HC4017 uses a five stage Johnson counter and decoding logic to provide high-speed operation. This device also has an active-high, as well as active-low clock input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 176 FETs or 44 Equivalent Gates

## MC54/74HC4017



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



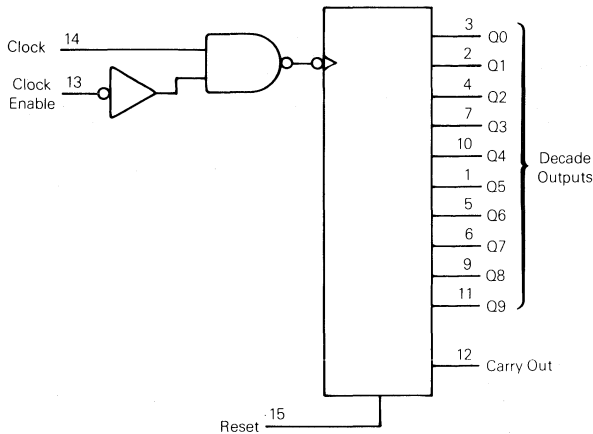
**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

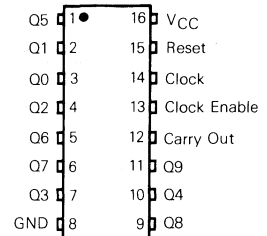
$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### LOGIC DIAGRAM



Pin 16 =  $V_{CC}$   
 Pin 8 = GND

### PIN ASSIGNMENT



# MC54/74HC4017

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	- 1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level. (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
Ceramic DIP: - 10 mW/°C from 100° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	- 55	+ 125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit			
				25°C to - 55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$				
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V			
			4.5	3.15	3.15	3.15				
			6.0	4.2	4.2	4.2				
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V			
			4.5	0.9	0.9	0.9				
			6.0	1.2	1.2	1.2				
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V			
			4.5	4.4	4.4	4.4				
			6.0	5.9	5.9	5.9				
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V			
			4.5	0.1	0.1	0.1				
			6.0	0.1	0.1	0.1				
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$			
			$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0		8	80	160

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HC4017

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 9)	2.0	4.0	3.2	2.6	MHz
		4.5	20	16	13	
		6.0	24	19	15	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 9)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Carry Out (Figures 2 and 9)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (Figures 3 and 9)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t <sub>PLH</sub>	Maximum Propagation Delay, Reset to Carry Out (Figures 3 and 9)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock Enable to Q (Figures 4 and 9)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock Enable to Carry Out (Figures 5 and 9)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 8 and 9)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	





# MC54/74HC4017

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{su}$	Minimum Setup Time, Clock Enable to Clock (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_{su}$	Minimum Setup Time, Clock Enable to Clock (Inhibit Count) (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_h$	Minimum Hold Time, Clock to Clock Enable (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_{rec}$	Minimum Recovery Time, Reset to Clock (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_w$	Minimum Pulse Width, Clock Input (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Reset Input (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Clock Enable Input (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

FUNCTION TABLE

Clock	Clock Enable	Reset	Output State*
L	X	L	no change
X	H	L	no change
X	X	H	reset counter, Q0 = H, Q1-Q9 = L, C0 = H
	L	L	advance to next state
	X	L	no change
X		L	no change
H		L	advance to next state

X = Don't care

\* Carry Out = H for Q0, Q1, Q2, Q3, or Q4 = H; Carry Out = L otherwise.

## PIN DESCRIPTIONS

### INPUTS

**CLOCK (PIN 14)** — Counter clock input. While Clock Enable is low, a low-to-high transition on this input advances the counter to its next state.

**RESET (PIN 15)** — Asynchronous counter reset input. A high level at this input initializes the counter and forces Q0 and Carry Out to a high, Q1-Q9 are forced to a low level.

**CLOCK ENABLE (PIN 13)** — Active-low clock enable input. A low level on this input allows the device to count. A high level on this input inhibits the counting operation. This input may also be used as a negative-edge clock input, using Clock (Pin 14) as an active-high enable pin.

### OUTPUTS

**Q0-Q9 (PINS 3, 2, 4, 7, 10, 1, 5, 6, 9, 11)** — Decoded decade counter outputs. Each of these outputs is high for one clock period only.

**CARRY OUT (PIN 12)** — Cascading output pin. This output is used either as a cascading output or a symmetrical divide-by-ten output. This output goes low when a count of five is reached and high when the counter advances to zero or when reset. When the counters are cascaded this output provides a rising-edge signal for the clock input of the next counter stage.

# MC54/74HC4017

## SWITCHING WAVEFORMS

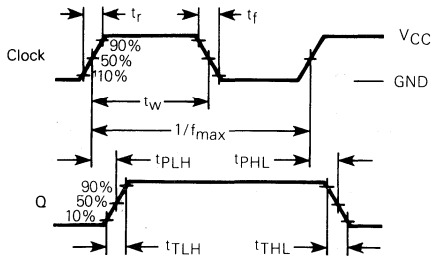


Figure 1.

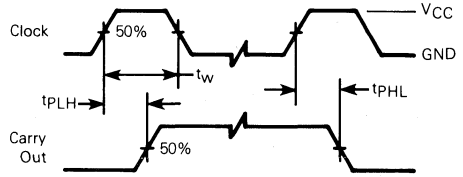


Figure 2.

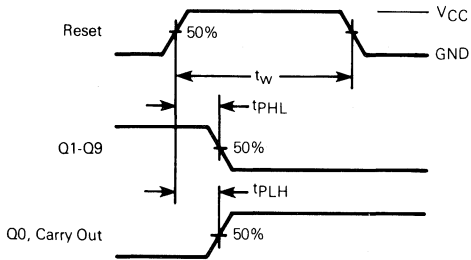


Figure 3.

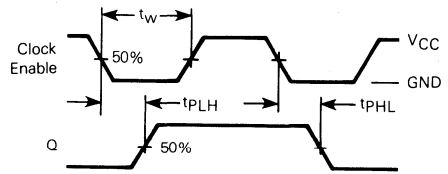


Figure 4.

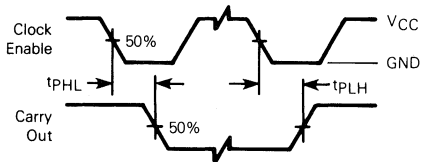


Figure 5.

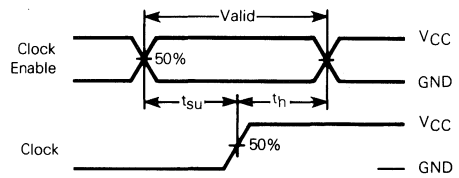


Figure 6.

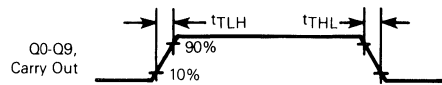


Figure 8.

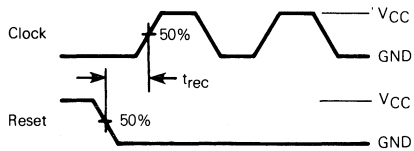
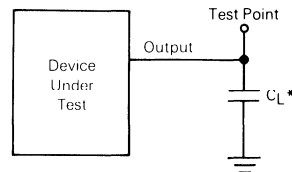


Figure 7.

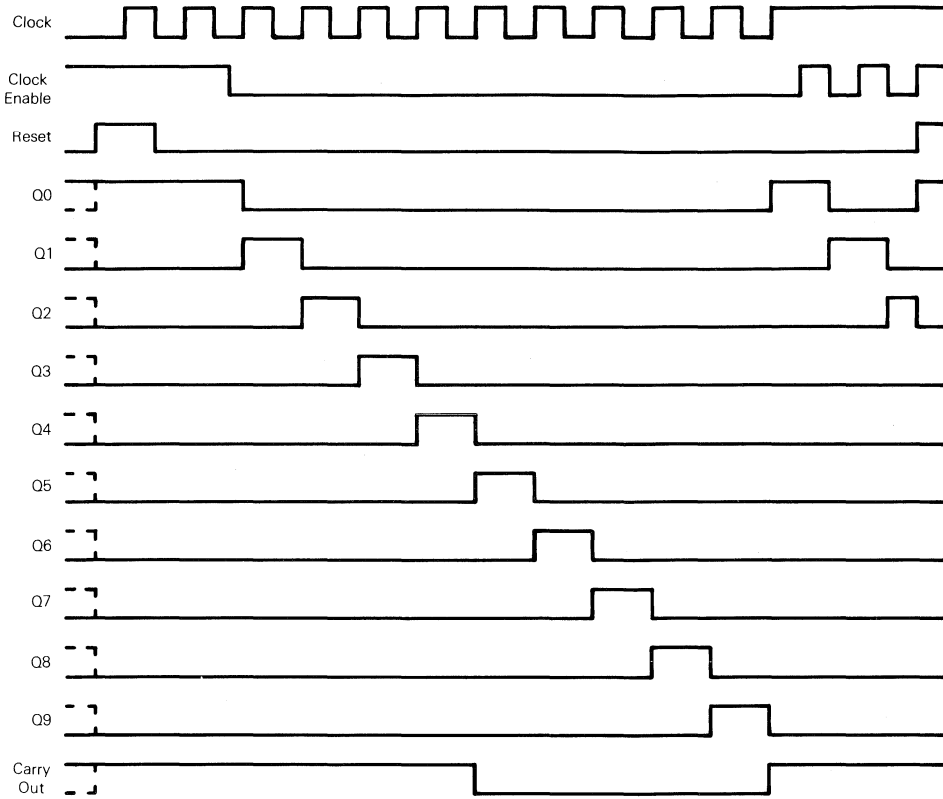


\* Includes all probe and jig capacitance.

Figure 9. Test Circuit

# MC54/74HC4017

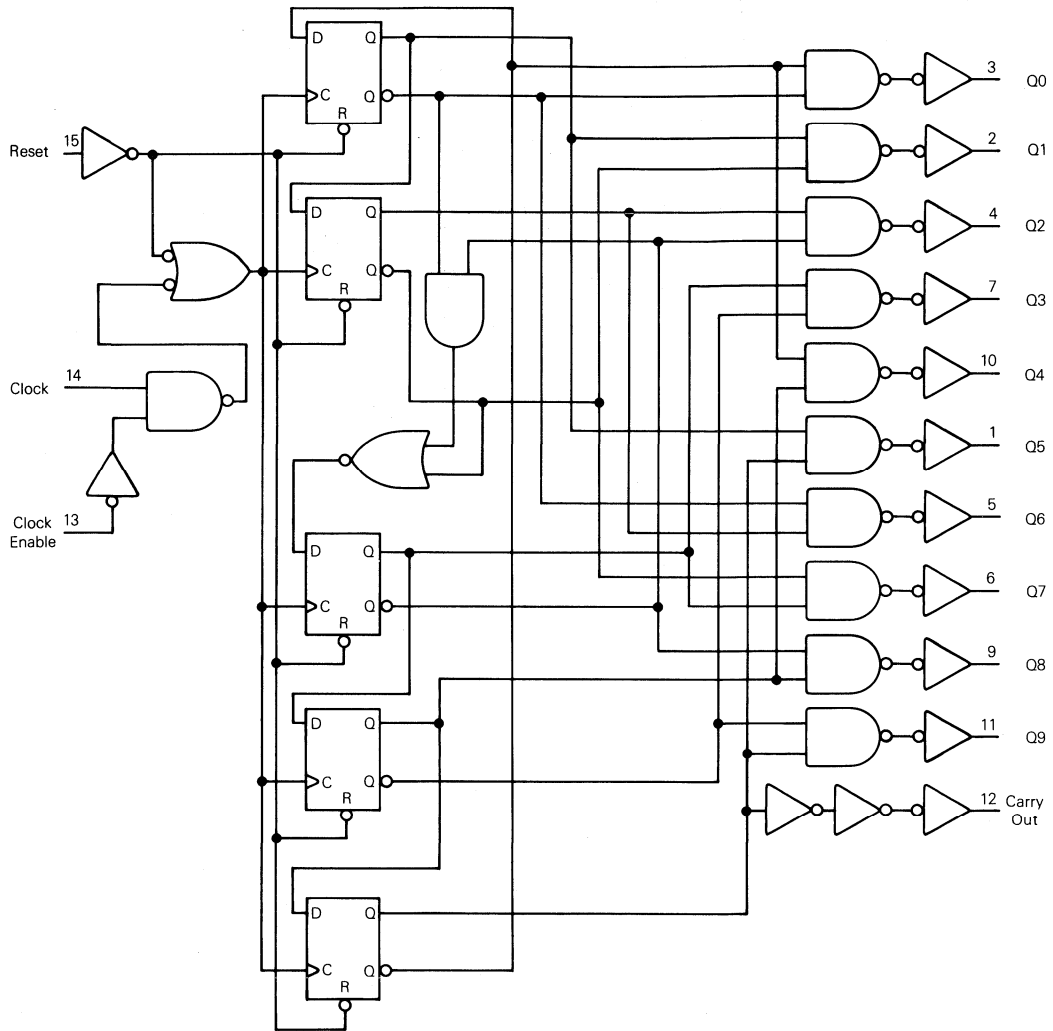
## TIMING DIAGRAM



5

# MC54/74HC4017

## EXPANDED LOGIC DIAGRAM



# MC54/74HC4017

## TYPICAL APPLICATIONS

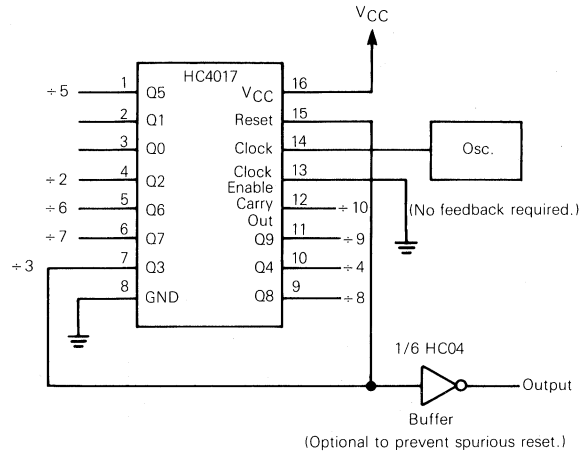


Figure 10 shows a divide by 2 through 10 circuit using one HC4017. Please note that since Reset is asynchronous, the output pulse widths are narrow.

**Figure 10. ÷2 Through ÷10 Circuit**

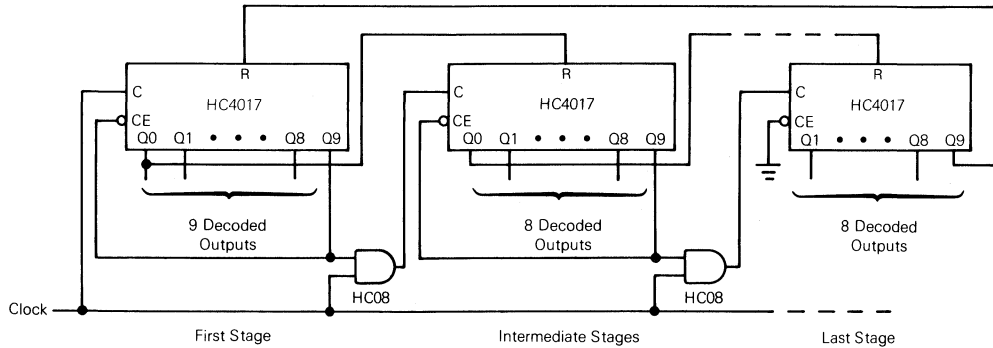


Figure 11 shows a technique for cascading the counters to extend the number of decoded output states. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

**Figure 11. Counter Expansion**

## 14-Stage Binary Ripple Counter

### High-Performance Silicon-Gate CMOS

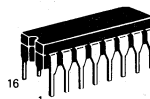
The MC54/74HC4020 is identical in pinout to the standard CMOS MC14020B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master-slave flip-flops with 12 stages brought out to pins. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

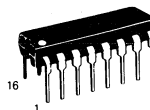
State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4020 for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates

## MC54/74HC4020



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



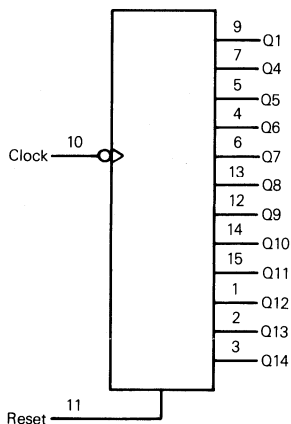
**N SUFFIX  
 PLASTIC  
 CASE 648-08**

### ORDERING INFORMATION

MC74HCXXXXN Plastic  
 MC54HCXXXXJ Ceramic

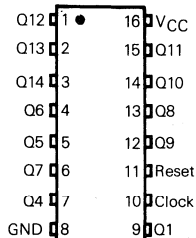
$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### LOGIC DIAGRAM



Pin 16 = VCC  
 Pin 8 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

# MC54/74HC4020

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260	°C
		300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HC4020

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	5.0	4.0	3.4	MHz
		4.5	25	20	17	
		6.0	29	24	20	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0	240	300	360	ns
		4.5	48	60	72	
		6.0	41	51	61	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Q <sub>N</sub> to Q <sub>N+1</sub> (Figures 3 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

\*For T<sub>A</sub> = 25°C and C<sub>L</sub> = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC} = 2.0 \text{ V: } t_p = [205 + 107.5(N - 1)] \text{ ns}$$

$$V_{CC} = 4.5 \text{ V: } t_p = [41 + 21.5(N - 1)] \text{ ns}$$

$$V_{CC} = 6.0 \text{ V: } t_p = [35 + 18.3(N - 1)] \text{ ns}$$

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		30	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC4020

## PIN DESCRIPTIONS

### INPUTS

**CLOCK (PIN 10)** — Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

**RESET (PIN 11)** — Active-high reset. A high level applied

to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

### OUTPUTS

**Q1, Q4—Q14 (PINS 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3)** — Active-high outputs. Each QN output divides the Clock input frequency by  $2^N$ .

## SWITCHING WAVEFORMS

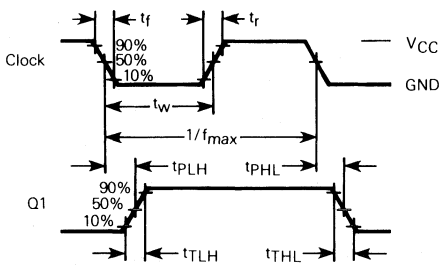


Figure 1.

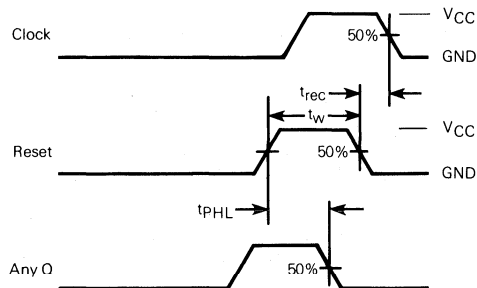


Figure 2.

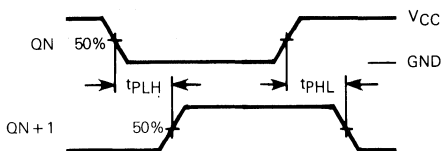
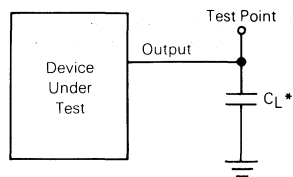


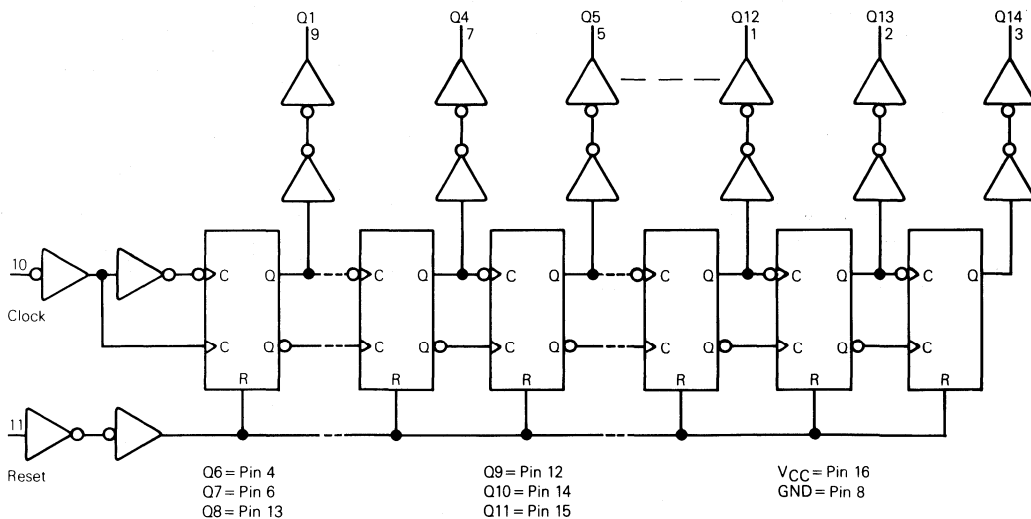
Figure 3.



\* Includes all probe and jig capacitance.

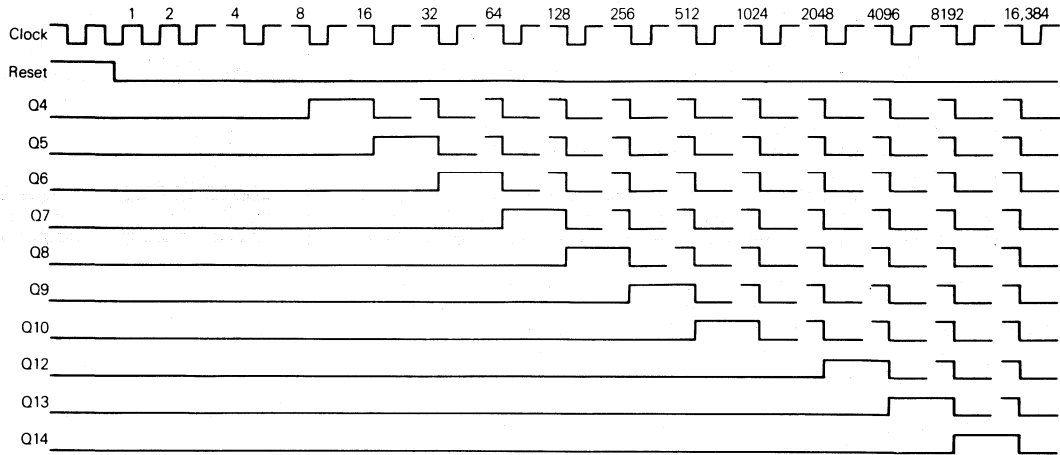
Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM



# MC54/74HC4020

## TIMING DIAGRAM

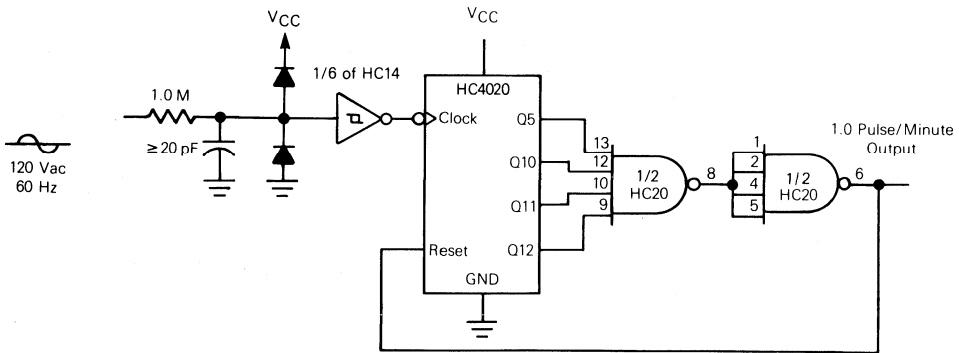


## APPLICATIONS INFORMATION

### TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the MC54/74HC14, Schmitt-trigger inverter. The HC14 squares-up the input waveform and feeds the

HC4020. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



## 7-Stage Binary Ripple Counter High-Performance Silicon-Gate CMOS

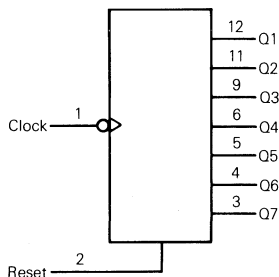
The MC54/74HC4024 is identical in pinout to the standard CMOS MC14024. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 7 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4024 for some designs.

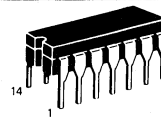
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 206 FETs or 51.5 Equivalent Gates

### LOGIC DIAGRAM

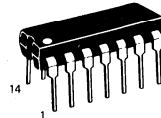


Pin 14 =  $V_{CC}$   
 Pin 7 = GND  
 Pins 8, 10 and 13 = No Connection

## MC54/74HC4024



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



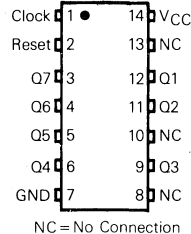
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

# MC54/74HC4024

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC4024

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	5.4	4.4	3.6	MHz
		4.5	27	22	18	
		6.0	32	26	21	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, QN to QN + 1 (Figures 3 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

\* For T<sub>A</sub> = 25°C and C<sub>L</sub> = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC} = 2.0 \text{ V: } t_p = [205 + 100(N - 1)] \text{ ns}$$

$$V_{CC} = 4.5 \text{ V: } t_p = [41 + 20(N - 1)] \text{ ns}$$

$$V_{CC} = 6.0 \text{ V: } t_p = [35 + 17(N - 1)] \text{ ns}$$

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		30	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

## PIN DESCRIPTIONS

### INPUTS

**CLOCK (PIN 1)** — Negative-edge triggering clock input. A high-to-low transition of this input advances the state of the counter.

**RESET (PIN 2)** — Active-high asynchronous reset. A high level applied to this input resets the counter to its zero state, thus forcing all Q outputs low.

### OUTPUTS

**Q1-Q7 (PINS 12, 11, 9, 6, 5, 4, 3)** — Active-high outputs. Each QN output divides the Clock input frequency by 2<sup>N</sup>.

# MC54/74HC4024

## SWITCHING WAVEFORMS

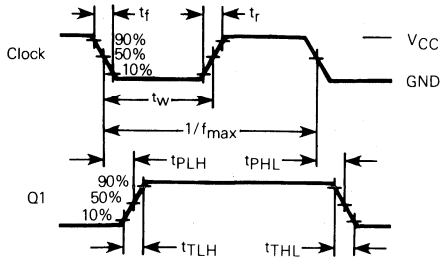


Figure 1.

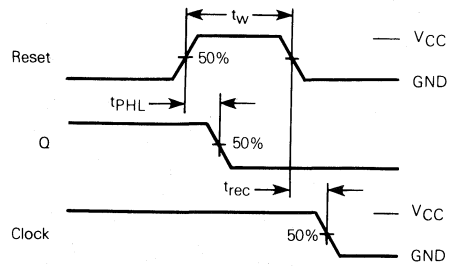


Figure 2.

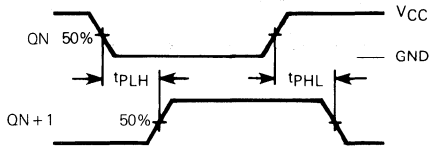
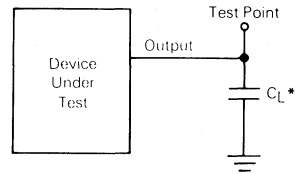


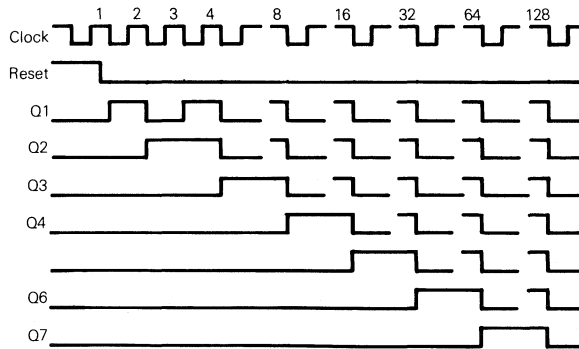
Figure 3.



\* Includes all probe and jig capacitance.

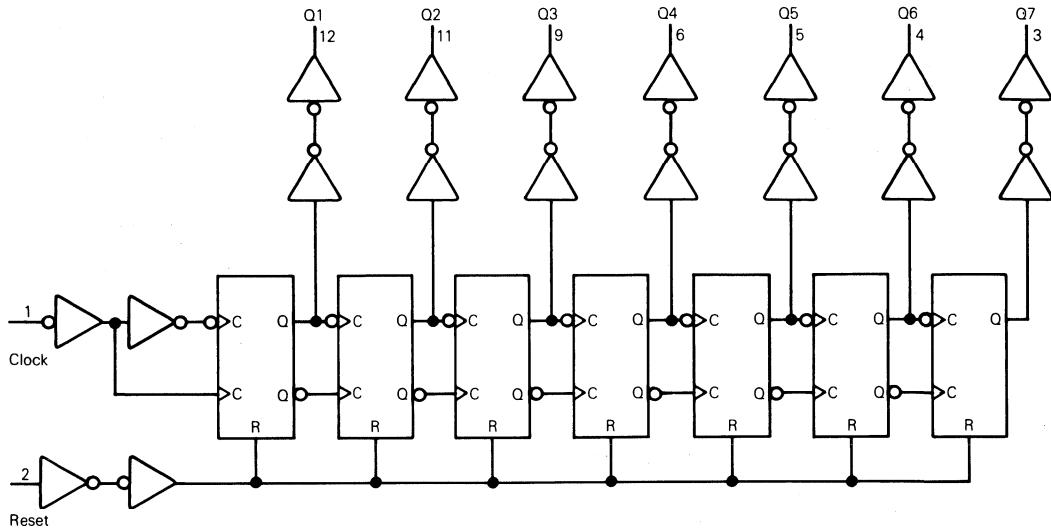
Figure 4. Test Circuit

## TIMING DIAGRAM



# MC54/74HC4024

## EXPANDED LOGIC DIAGRAM



5



## 12-Stage Binary Ripple Counter

### High-Performance Silicon-Gate CMOS

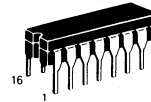
The MC54/74HC4040 is identical in pinout to the standard CMOS MC14040. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

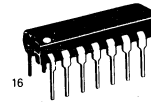
State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4040 for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates

## MC54/74HC4040



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



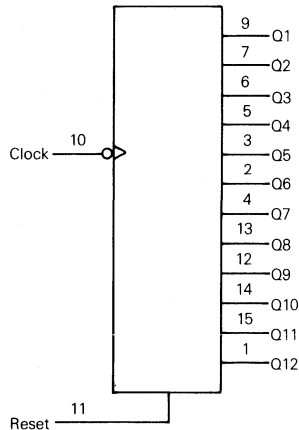
**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**

### ORDERING INFORMATION

·MC74HCXXXXN Plastic  
 MC54HCXXXXJ Ceramic

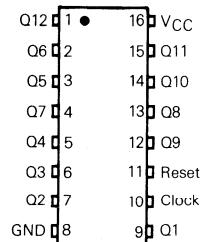
$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### LOGIC DIAGRAM



Pin 16 =  $V_{CC}$   
 Pin 8 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

# MC54/74HC4040

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC4040

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, QN to QN + 1 (Figures 3 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

\*For T<sub>A</sub> = 25°C and C<sub>L</sub> = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC} = 2.0 \text{ V: } t_p = [205 + 107.5(N - 1)] \text{ ns}$$

$$V_{CC} = 4.5 \text{ V: } t_p = [41 + 21.5(N - 1)] \text{ ns}$$

$$V_{CC} = 6.0 \text{ V: } t_p = [35 + 18.3(N - 1)] \text{ ns}$$

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = CPD V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4.

## PIN DESCRIPTIONS

### INPUTS

**CLOCK (PIN 10)** — Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

**RESET (PIN 11)** — Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

### OUTPUTS

**Q1 THRU Q12 (PINS 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1)**  
— Active-high outputs. Each QN output divides the Clock input frequency by 2<sup>N</sup>.

5

# MC54/74HC4040

## SWITCHING WAVEFORMS

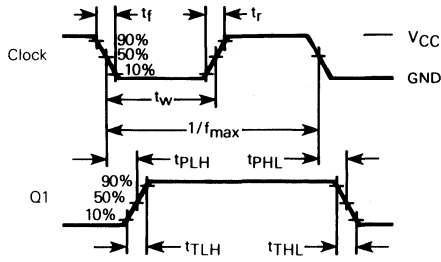


Figure 1.

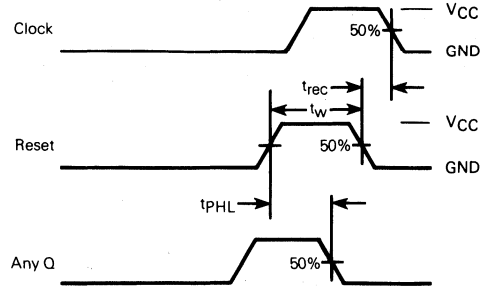


Figure 2.

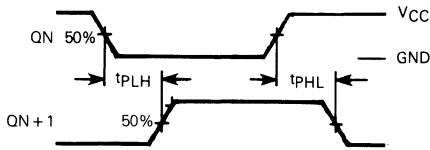
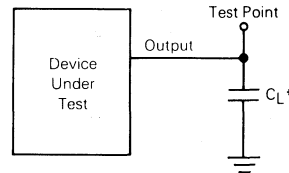


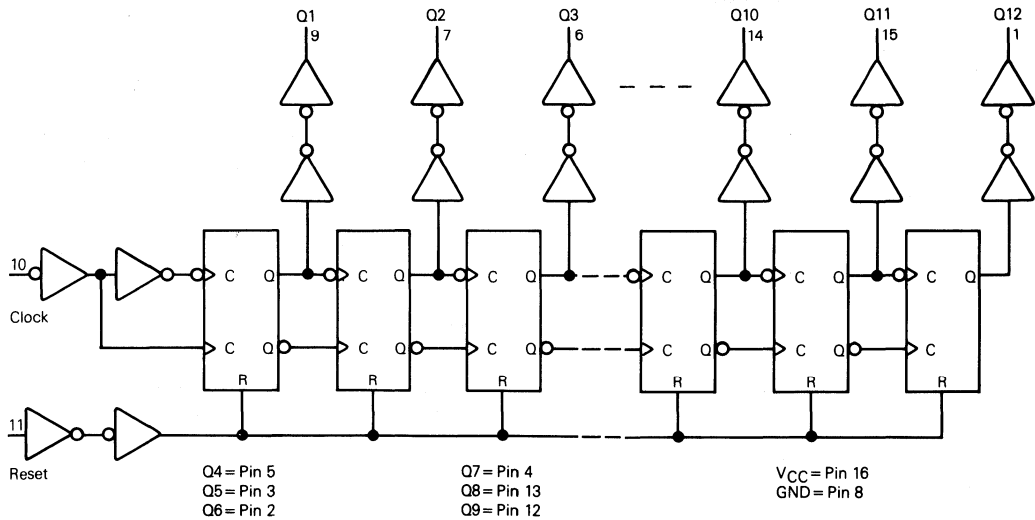
Figure 3.



\* Includes all probe and jig capacitance.

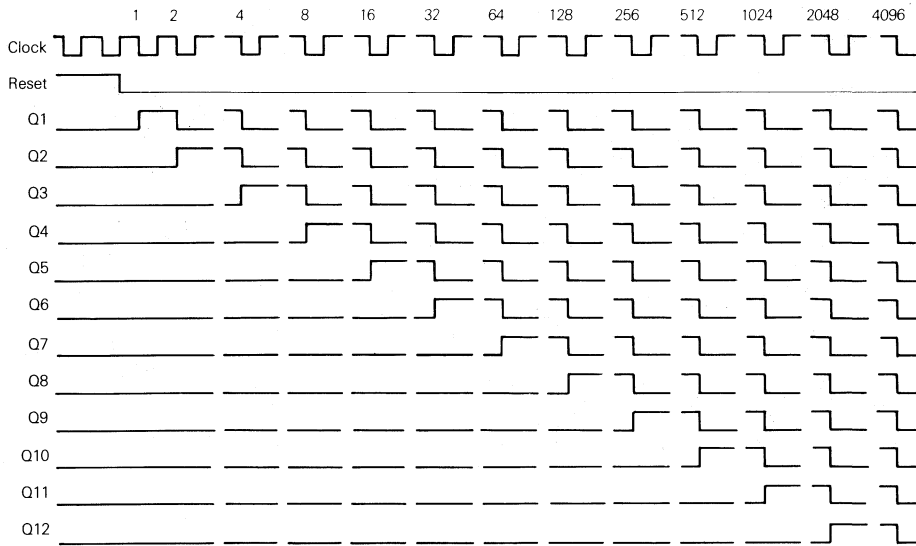
Figure 4. Test Circuit

## EXPANDED LOGIC DIAGRAM



# MC54/74HC4040

## TIMING DIAGRAM

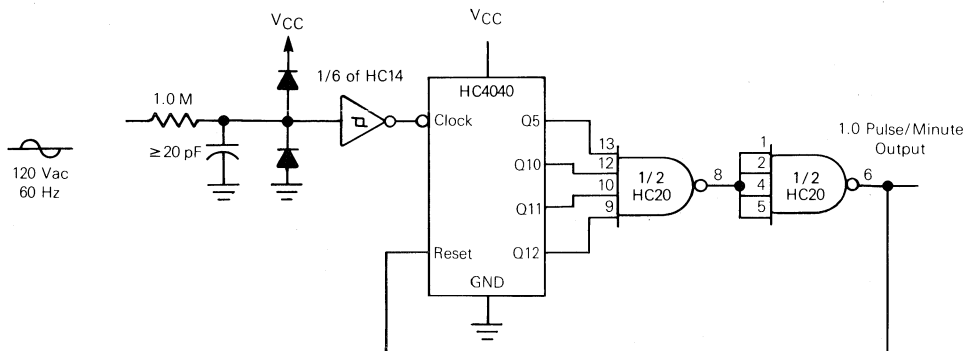


## APPLICATIONS INFORMATION

### TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the HC14, Schmitt-trigger inverter. The HC14 squares-up the input waveform and feeds the HC4040.

Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



## Phase-Locked Loop

### High-Performance Silicon-Gate CMOS

The MC54/74HC4046A is similar in function to the MC14046 Metal gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

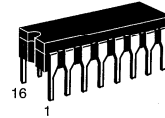
The HC4046A phase-locked loop contains three phase comparators, a voltage-controlled oscillator (VCO) and unity gain op-amp DEM<sub>OUT</sub>. The comparators have two common signal inputs, COMP<sub>IN</sub>, and SIG<sub>IN</sub>. Input SIG<sub>IN</sub> and COMP<sub>IN</sub> can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor to small voltage signals). The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal PC1<sub>OUT</sub> and maintains 90 degrees phase shift at the center frequency between SIG<sub>IN</sub> and COMP<sub>IN</sub> signals (both at 50% duty cycle). Phase comparator 2 (with leading-edge sensing logic) provides digital error signals PC2<sub>OUT</sub> and PCP<sub>OUT</sub> and maintains a 0 degree phase shift between SIG<sub>IN</sub> and COMP<sub>IN</sub> signals (duty cycle is immaterial). The linear VCO produces an output signal VCO<sub>OUT</sub> whose frequency is determined by the voltage of input VCO<sub>IN</sub> signal and the capacitor and resistors connected to pins C1A, C1B, R1 and R2. The unity gain op-amp output DEM<sub>OUT</sub> with an external resistor is used where the VCO<sub>IN</sub> signal is needed but no loading can be tolerated. The inhibit input, when high, disables the VCO and all op-amps to minimize standby power consumption.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

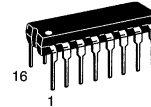
- Output Drive Capability: 10 LSTTL Loads
- Low Power Consumption Characteristic of CMOS Devices
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A Maximum (except SIG<sub>IN</sub> and COMP<sub>IN</sub>)
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Low Quiescent Current: 80  $\mu$ A Maximum (VCO disabled)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on all Inputs
- Chip Complexity: 279 FETs or 70 Equivalent Gates

Pin No.	Symbol	Name and Function
1	PCP <sub>OUT</sub>	Phase Comparator Pulse Output
2	PC1 <sub>OUT</sub>	Phase Comparator 1 Output
3	COMP <sub>IN</sub>	Comparator Input
4	VCO <sub>OUT</sub>	VCO Output
5	INH	Inhibit Input
6	C1A	Capacitor C1 Connection A
7	C1B	Capacitor C1 Connection B
8	GND	Ground (0 V) V <sub>SS</sub>
9	VCO <sub>IN</sub>	VCO Input
10	DEM <sub>OUT</sub>	Demodulator Output
11	R1	Resistor R1 Connection
12	R2	Resistor R2 Connection
13	PC2 <sub>OUT</sub>	Phase Comparator 2 Output
14	SIG <sub>IN</sub>	Signal Input
15	PC3 <sub>OUT</sub>	Phase Comparator 3 Output
16	VCC	Positive Supply Voltage

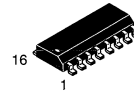
## MC54/74HC4046A



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**

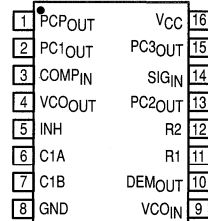


**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

### ORDERING INFORMATION

MC74HCXXAN	Plastic
MC54HCXXAJ	Ceramic
MC74HCXXAD	SOIC

### PIN ASSIGNMENT



# MC54/74HC4046A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND) VCO only	3.0	6.0	V	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND) NON-VCO	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Pin 5)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## [Phase Comparator Section]

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	V <sub>CC</sub> Volts	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage DC Coupled SIG <sub>IN</sub> , COMP <sub>IN</sub>	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage DC Coupled SIG <sub>IN</sub> , COMP <sub>IN</sub>	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage PCP <sub>OUT</sub> , PCn <sub>OUT</sub>	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 mA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			4.5	3.98	3.84	3.7	

NOTE: Information on typical parametric values can be found in Chapter 4.

(continued)

5

# MC54/74HC4046A

## [Phase Comparator Section]

DC ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to GND)							
Symbol	Parameter	Test Conditions	VCC Volts	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>OL</sub>	Maximum Low-Level Output Voltage Qa-Qh PC <sub>2</sub> OUT, PC <sub>3</sub> OUT	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I <sub>in</sub>	Maximum Input Leakage Current SIG <sub>IN</sub> , COMP <sub>IN</sub>	V <sub>in</sub> = V <sub>CC</sub> or GND	2.0	±3.0	±4.0	±5.0	μA
			3.0	±7.0	±9.0	±11.0	
			4.5	±18.0	±23.0	±27.0	
			6.0	±30.0	±38.0	±45.0	
I <sub>OZ</sub>	Maximum Three-State Leakage Current PC <sub>2</sub> OUT	Output in High-Impedance State V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package) (VCO disabled) Pins 3, 5 and 14 at V <sub>CC</sub> Pin 9 at GND; Input Leakage at Pins 3 and 14 to be excluded	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   = 0 μA	6.0	4.0	40	160	μA

## [Phase Comparator Section]

AC ELECTRICAL CHARACTERISTICS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)						
Symbol	Parameter	VCC Volts	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, SIG <sub>IN</sub> /COMP <sub>IN</sub> to PC <sub>1</sub> OUT (Figure 1)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, SIG <sub>IN</sub> /COMP <sub>IN</sub> to PC <sub>2</sub> OUT (Figure 1)	2.0	340	425	510	ns
		4.5	68	85	102	
		6.0	58	72	87	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, SIG <sub>IN</sub> /COMP <sub>IN</sub> to PC <sub>3</sub> OUT (Figure 1)	2.0	270	340	405	ns
		4.5	54	68	81	
		6.0	46	58	69	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, SIG <sub>IN</sub> /COMP <sub>IN</sub> Output Disable Time to PC <sub>2</sub> OUT (Figures 2 and 3)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Propagation Delay, SIG <sub>IN</sub> /COMP <sub>IN</sub> Output Enable Time to PC <sub>2</sub> OUT (Figures 2 and 3)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time (Figure 1)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	

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**[VCO Section]**

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)										
Symbol	Parameter	Test Conditions	V <sub>CC</sub> Volts	Guaranteed Limit				Unit		
				25°C to -55°C		≤ 85°C			≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage INH	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	3.0	2.1	2.1	2.1	2.1	V		
			4.5	3.15	3.15	3.15	3.15			
			6.0	4.2	4.2	4.2	4.2			
V <sub>IL</sub>	Maximum Low-Level Input Voltage INH	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	3.0	0.90	0.9	0.9	0.9	V		
			4.5	1.35	1.35	1.35	1.35			
			6.0	1.8	1.8	1.8	1.8			
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>COOUT</sub>	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	3.0	1.9	1.9	1.9	1.9	V		
			4.5	4.4	4.4	4.4	4.4			
			6.0	5.9	5.9	5.9	5.9			
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>COOUT</sub>	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	3.0	0.1	0.1	0.1	0.1	V		
			4.5	0.1	0.1	0.1	0.1			
			6.0	0.1	0.1	0.1	0.1			
I <sub>in</sub>	Maximum Input Leakage Current INH, V <sub>COIN</sub>	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	0.1	1.0	1.0	1.0	μA		
V <sub>VCOIN</sub>	Operating Voltage Range at V <sub>COIN</sub> over the range specified for R1; For linearity see Fig. 15A, Parallel value of R1 and R2 should be > 2.7 kΩ	INH = V <sub>IL</sub>	3.0	Min	Max	Min	Max	Min	Max	V
			4.5	0.1	1.0	0.1	1.0	0.1	1.0	
			6.0	0.1	4.0	0.1	4.0	0.1	4.0	
R1	Resistor Range		3.0	3.0	300	3.0	300	3.0	300	kΩ
			4.5	3.0	300	3.0	300	3.0	300	
			6.0	3.0	300	3.0	300	3.0	300	
R2	Resistor Range		3.0	3.0	300	3.0	300	3.0	300	kΩ
			4.5	3.0	300	3.0	300	3.0	300	
			6.0	3.0	300	3.0	300	3.0	300	
C1	Capacitor Range		3.0	40	No Limit					pF
			4.5	40						
			6.0	40						

**[VCO Section]**

AC ELECTRICAL CHARACTERISTICS (C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns)									
Symbol	Parameter	V <sub>CC</sub> Volts	Guaranteed Limit				Unit		
			25°C to -55°C		≤ 85°C			≤ 125°C	
Δf/T	Frequency Stability with Temperature Changes (Figure 13A, B, C)	3.0	Min	Max	Min	Max	Min	Max	% / K
		4.5							
		6.0							
f <sub>o</sub>	VCO Center Frequency (Duty Factor = 50%) (Figure 14A, B, C, D)	3.0	3						MHz
		4.5	11						
		6.0	13						
Δf/VCO	VCO Frequency Linearity	3.0	See Figures 15A, B, C				%		
		4.5							
		6.0							
∂ VCO	Duty Factor at V <sub>COOUT</sub>	3.0	Typical 50%				%		
		4.5							
		6.0							

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## [Demodulator Section]

DC ELECTRICAL CHARACTERISTICS									
Symbol	Parameter	Test Conditions	V <sub>CC</sub> Volts	Guaranteed Limit				Unit	
				25°C to -55°C		≤ 85°C			≤ 125°C
				Min	Max	Min	Max		Min
RS	Resistor Range	At RS > 300 kΩ the Leakage Current can influence V <sub>DEMOUT</sub>	3.0						kΩ
			4.5	50	300				
			6.0	50	300				
V <sub>OFF</sub>	Offset Voltage V <sub>COIN</sub> to V <sub>DEMOUT</sub>	V <sub>I</sub> = V <sub>VCOIN</sub> = 1/2 V <sub>CC</sub> ; Values taken over RS Range.	3.0 4.5 6.0	See Figure 12				mV	
RD	Dynamic Output Resistance at DEM <sub>OUT</sub>	V <sub>DEMOUT</sub> = 1/2 V <sub>CC</sub>	3.0 4.5 6.0	Typical 25 Ω				Ω	

## SWITCHING WAVEFORMS

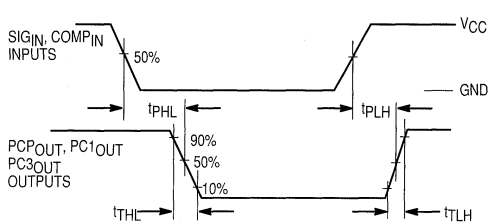


Figure 1.

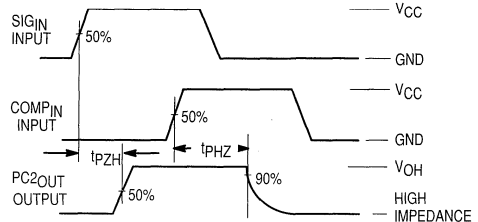


Figure 2.

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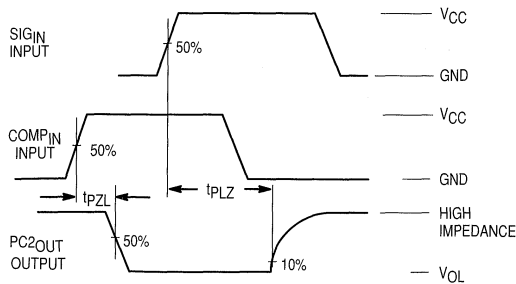
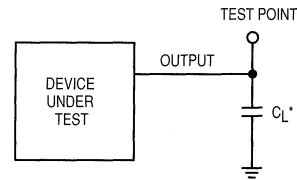


Figure 3.



\*INCLUDES ALL PROBE AND JIG CAPACITANCE

Figure 4. Test Circuit

DETAILED CIRCUIT DESCRIPTION

Voltage Controlled Oscillator/Demodulator Output

The VCO requires two or three external components to operate. These are R1, R2, C1. Resistor R1 and Capacitor C1 are selected to determine the center frequency of the VCO (see typical performance curves Figure 14). R2 can be used to set the offset frequency with 0 volts at VCO input. For example, if R2 is decreased, the offset frequency is increased. If R2 is omitted the VCO range is from 0 Hz. The effect of R2 is shown in Figure 24, typical performance curves. By increasing the value of R2 the lock range of the PLL is increased and the gain (volts/Hz) is decreased. Thus, for a narrow lock range, large swings on the VCO input will cause less frequency variation.

Internally, the resistors set a current in a current mirror, as shown in Figure 5. The mirrored current drives one side of the

capacitor. Once the voltage across the capacitor charges up to  $V_{ref}$  of the comparators, the oscillator logic flips the capacitor which causes the mirror to charge the opposite side of the capacitor. The output from the internal logic is then taken to VCO output (Pin 4).

The input to the VCO is a very high impedance CMOS input and thus will not load down the loop filter, easing the filters design. In order to make signals at the VCO input accessible without degrading the loop performance, the VCO input voltage is buffered through a unity gain Op-amp to Demod Output. This Op-amp can drive loads of 50K ohms or more and provides no loading effects to the VCO input voltage (see Figure 12).

An inhibit input is provided to allow disabling of the VCO and all Op-amps (see Figure 5). This is useful if the internal VCO is not being used. A logic high on inhibit disables the VCO and all Op-amps, minimizing standby power consumption.

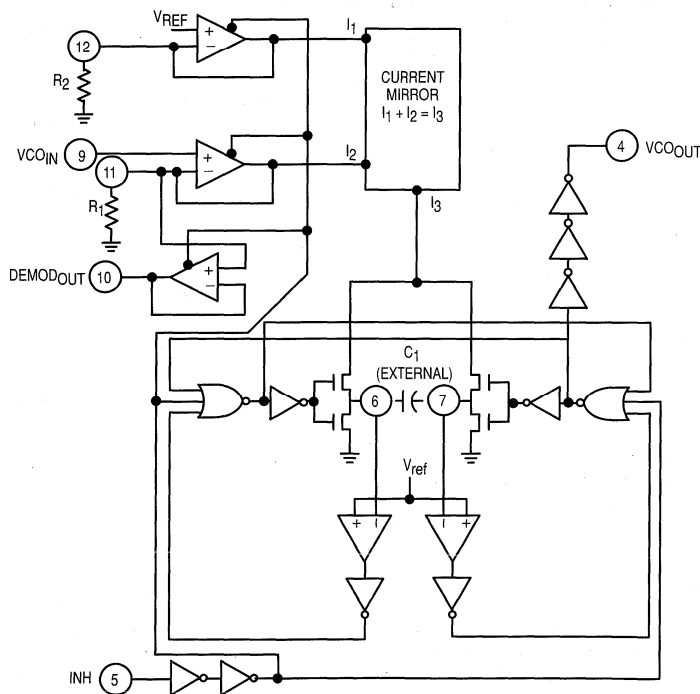


Figure 5. Logic Diagram for VCO

The output of the VCO is a standard high speed CMOS output with an equivalent LS-TTL fan out of 10. The VCO output is approximately a square wave. This output can either directly feed the COMP<sub>IN</sub> of the phase comparators or feed external prescalers (counters) to enable frequency synthesis.

**Phase Comparators**

All three phase comparators have two inputs, SIG<sub>IN</sub> and COMP<sub>IN</sub>. The SIG<sub>IN</sub> and COMP<sub>IN</sub> have a special DC bias

network that enables AC coupling of input signals. If the signals are not AC coupled, standard 54HC/74HC input levels are required. Both input structures are shown in Figure 6. The outputs of these comparators are essentially standard 54HC/74HC outputs (comparator 2 is TRI-STATEABLE). In normal operation V<sub>CC</sub> and ground voltage levels are fed to the loop filter. This differs from some phase detectors which supply a current to the loop filter and should be considered in the design. (The MC14046 also provides a voltage).

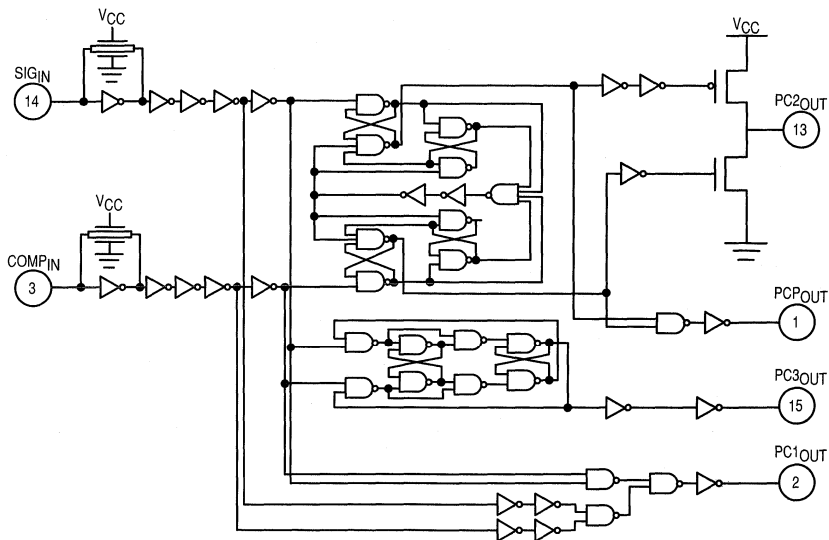


Figure 6. Logic Diagram for Phase Comparators

**Phase Comparator 1**

This comparator is a simple XOR gate similar to the 54/74HC86. Its operation is similar to an overdriven balanced modulator. To maximize lock range the input frequencies must have a 50% duty cycle. Typical input and output waveforms are shown in Figure 7. The output of the phase detector feeds the loop filter which averages the output voltage. The frequency range upon which the PLL will lock onto if initially out of lock is defined as the capture range. The capture range for phase detector 1 is dependent on the loop filter design. The capture range can be as large as the lock range, which is equal to the VCO frequency range.

To see how the detector operates, refer to Figure 7. When two square wave signals are applied to this comparator, an output waveform (whose duty cycle is dependent on the phase difference between the two signals) results. As the phase difference increases, the output duty cycle increases and the voltage after the loop filter increases. In order to achieve lock when the PLL input frequency increases, the VCO input voltage must increase and the phase difference between COMP<sub>IN</sub> and SIG<sub>IN</sub> will increase. At an input frequency equal to  $f_{min}$ , the VCO input is at 0 V. This requires the phase detector output to be grounded; hence, the two input signals must be in phase. When the input frequency is  $f_{max}$ , the VCO input

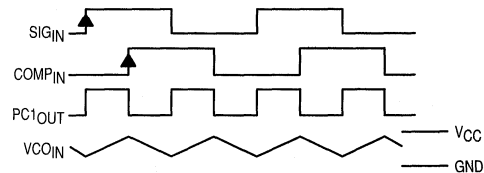


Figure 7. Typical Waveforms for PLL Using Phase Comparator 1

must be V<sub>CC</sub> and the phase detector inputs must be 180 degrees out of phase.

The XOR is more susceptible to locking onto harmonics of the SIG<sub>IN</sub> than the digital phase detector 2. For instance, a signal 2 times the VCO frequency results in the same output duty cycle as a signal equal to the VCO frequency. The difference is that the output frequency of the 2f example is twice that of the other example. The loop filter and VCO range should be designed to prevent locking on to harmonics.

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### Phase Comparator 2

This detector is a digital memory network. It consists of four flip-flops and some gating logic, a three state output and a phase pulse output as shown in Figure 6. This comparator acts only on the positive edges of the input signals and is independent of duty cycle.

Phase comparator 2 operates in such a way as to force the PLL into lock with 0 phase difference between the VCO output and the signal input positive waveform edges. Figure 8 shows some typical loop waveforms. First assume that SIG<sub>IN</sub> is leading the COMP<sub>IN</sub>. This means that the VCO's frequency must be increased to bring its leading edge into proper phase alignment. Thus the phase detector 2 output is set high. This will cause the loop filter to charge up the VCO input, increasing the VCO frequency. Once the leading edge of the COMP<sub>IN</sub> is detected, the output goes TRI-STATE holding the VCO input at the loop filter voltage. If the VCO still lags the SIG<sub>IN</sub> then the phase detector will again charge up the VCO input for the time between the leading edges of both waveforms.

If the VCO leads the SIG<sub>IN</sub> then when the leading edge of the VCO is seen; the output of the phase comparator goes low. This discharges the loop filter until the leading edge of the SIG<sub>IN</sub> is detected at which time the output disables itself again. This has the effect of slowing down the VCO to again make the rising edges of both waveforms coincidental.

When the PLL is out of lock, the VCO will be running either slower or faster than the SIG<sub>IN</sub>. If it is running slower the phase detector will see more SIG<sub>IN</sub> rising edges and so the output of the phase comparator will be high a majority of the time, raising the VCO's frequency. Conversely, if the VCO is running faster than the SIG<sub>IN</sub>, the output of the detector will be low most of the time and the VCO's output frequency will be decreased.

As one can see, when the PLL is locked, the output of phase comparator 2 will be disabled except for minor corrections at the leading edge of the waveforms. When PC<sub>2</sub> is TRI-STATE, the PCP output is high. This output can be used to determine when the PLL is in the locked condition.

This detector has several interesting characteristics. Over the entire VCO frequency range there is no phase difference between the COMP<sub>IN</sub> and the SIG<sub>IN</sub>. The lock range of the PLL is the same as the capture range. Minimal power was consumed in the loop filter since in lock the detector output is a high impedance. When no SIG<sub>IN</sub> is present, the detector will see only VCO leading edges, so the comparator output will stay low, forcing the VCO to  $f_{min}$ .

Phase comparator 2 is more susceptible to noise, causing the PLL to unlock. If a noise pulse is seen on the SIG<sub>IN</sub>, the comparator treats it as another positive edge of the SIG<sub>IN</sub> and will cause the output to go high until the VCO leading edge is seen, potentially for an entire SIG<sub>IN</sub> period. This would cause the VCO to speed up during that time. When using PC<sub>1</sub>, the output of that phase detector would be disturbed for only the short duration of the noise spike and would cause less upset.

### Phase Comparator 3

This is a positive edge-triggered sequential phase detector using an RS flip-flop as shown in Figure 6. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG<sub>IN</sub> and COMP<sub>IN</sub> are not important. It has some similar characteristics to the edge sensitive comparator. To see how this detector works, assume input pulses are applied to the SIG<sub>IN</sub> and COMP<sub>IN</sub>'s as shown in Figure 9. When the SIG<sub>IN</sub> leads the COMP<sub>IN</sub>, the flop is set. This will charge the loop filter and cause the VCO to speed up, bringing the comparator into phase with the SIG<sub>IN</sub>. The phase angle between SIG<sub>IN</sub> and COMP<sub>IN</sub> varies from 0° to 360° and is 180° at  $f_0$ . The voltage swing for PC<sub>3</sub> is greater than for PC<sub>2</sub> but consequently has more ripple in the signal to the VCO. When no SIG<sub>IN</sub> is present the VCO will be forced to  $f_{max}$  as opposed to  $f_{min}$  when PC<sub>2</sub> is used.

The operating characteristics of all three phase comparators should be compared to the requirements of the system design and the appropriate one should be used.

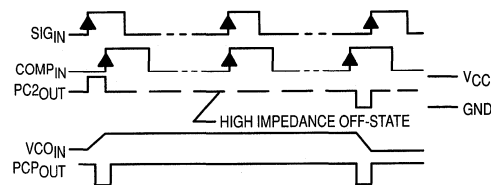


Figure 8. Typical Waveforms for PLL Using Phase Comparator 2

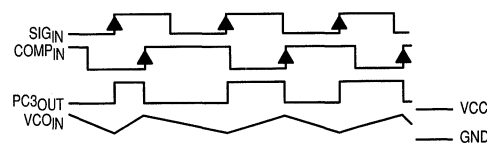


Figure 9. Typical Waveform for PLL Using Phase Comparator 3

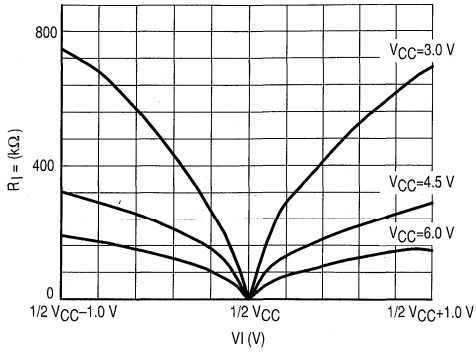


Figure 10. Input Resistance at SIG<sub>1N</sub>, COMP<sub>1N</sub> with  $\Delta V_1 = 1.0$  V at Self-Bias Point

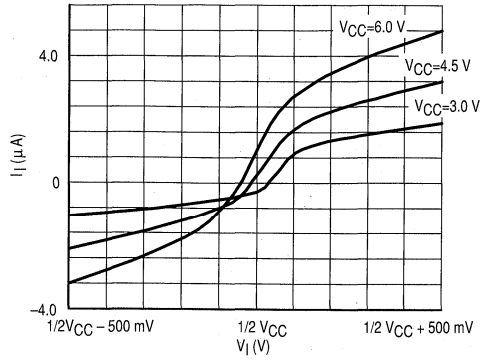


Figure 11. Input Current at SIG<sub>1N</sub>, COMP<sub>1N</sub> with  $\Delta V_1 = 500$  mV at Self-Bias Point

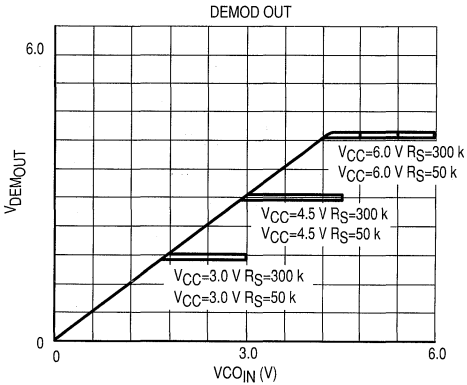


Figure 12. Offset Voltage at Demodulator Output as a Function of VCO<sub>1N</sub> and R<sub>S</sub>

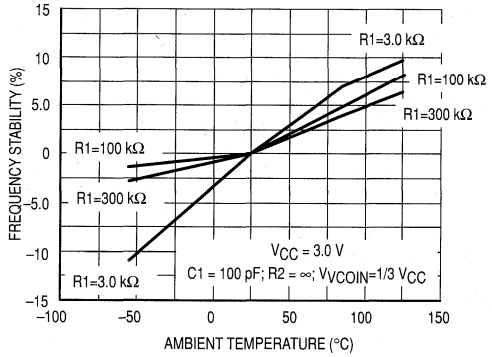


Figure 13A. Frequency Stability versus Ambient Temperature: VCC = 3.0 V

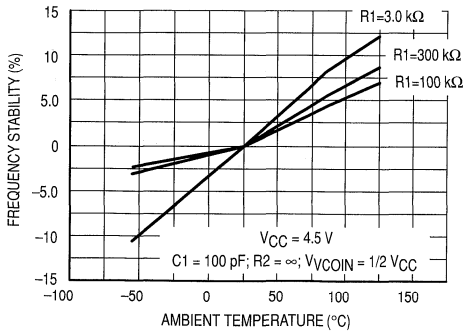


Figure 13B. Frequency Stability versus Ambient Temperature: VCC = 4.5 V

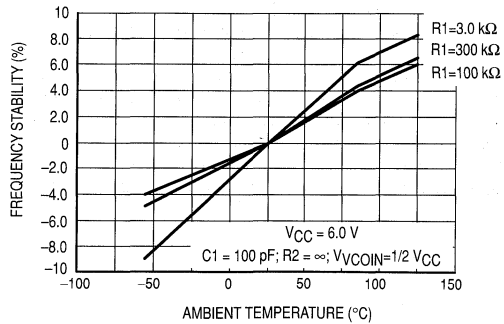


Figure 13C. Frequency Stability versus Ambient Temperature: VCC = 6.0 V

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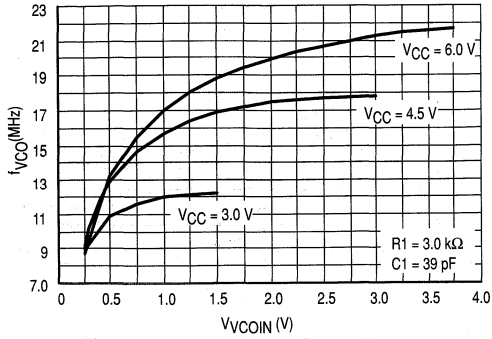


Figure 14A. VCO Frequency ( $f_{VCO}$ ) as a Function of the VCO Input Voltage ( $V_{VCOIN}$ )

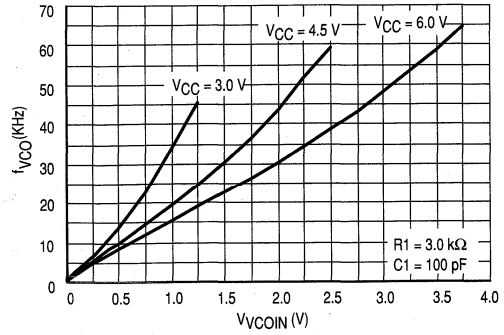


Figure 14B. VCO Frequency ( $f_{VCO}$ ) as a Function of the VCO Input Voltage ( $V_{VCOIN}$ )

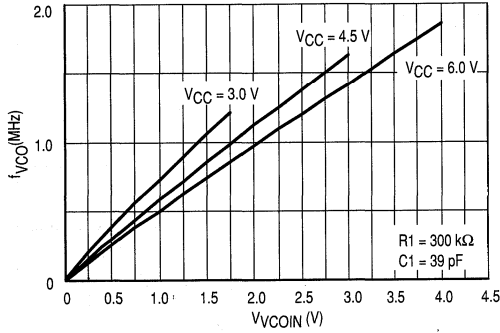


Figure 14C. VCO Frequency ( $f_{VCO}$ ) as a Function of the VCO Input Voltage ( $V_{VCOIN}$ )

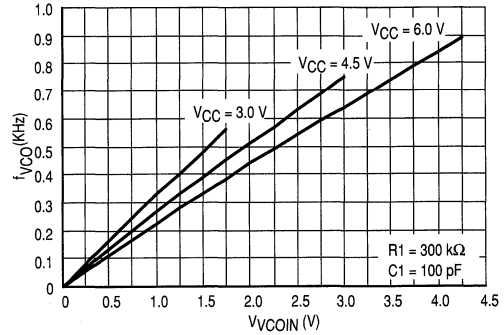


Figure 14D. VCO Frequency ( $f_{VCO}$ ) as a Function of the VCO Input Voltage ( $V_{VCOIN}$ )

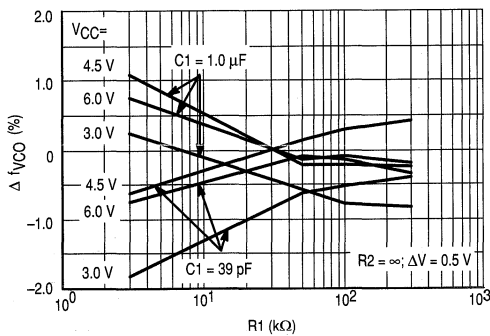
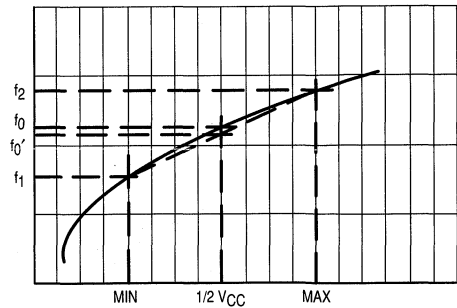


Figure 15A. Frequency Linearity versus  $R_1$ ,  $C_1$  and  $V_{CC}$



$\Delta V = 0.5 \text{ V}$  OVER THE  $V_{CC}$  RANGE:  
FOR VCO LINEARITY

$$f_0' = (f_1 + f_2) / 2$$

$$\text{LINEARITY} = (f_0' - f_0) / f_0' \times 100\%$$

Figure 15B. Definition of VCO Frequency Linearity

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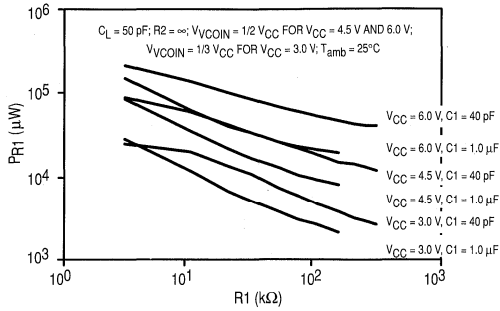


Figure 16. Power Dissipation versus R1

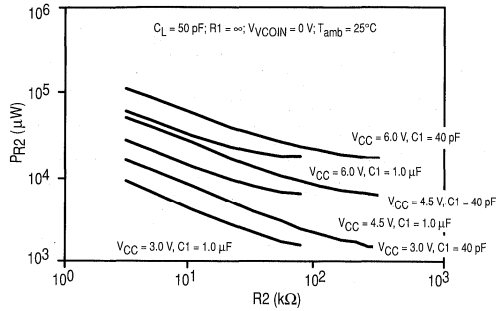


Figure 17. Power Dissipation versus R2

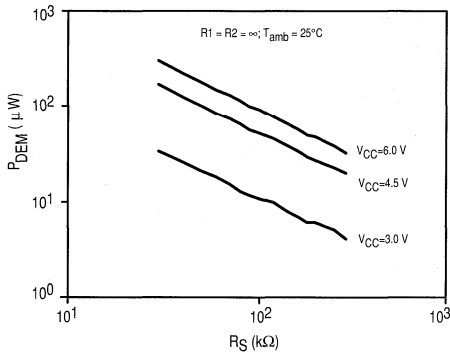


Figure 18. DC Power Dissipation of Demodulator versus RS

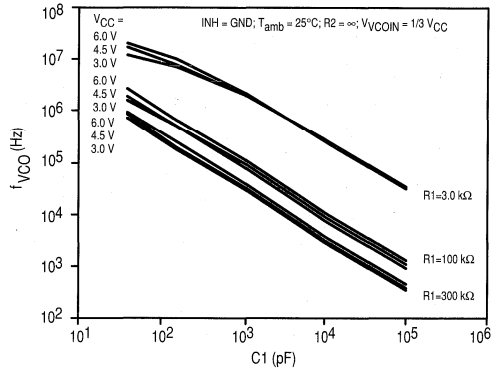


Figure 19. VCO Center Frequency versus C1

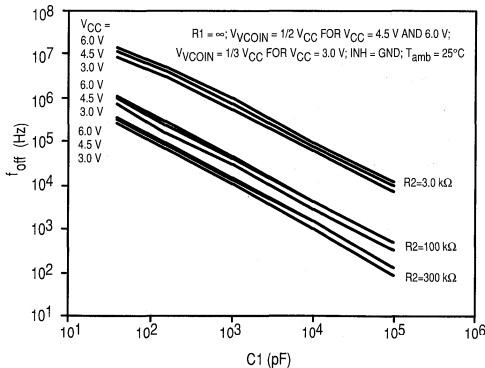


Figure 20. Frequency Offset versus C1

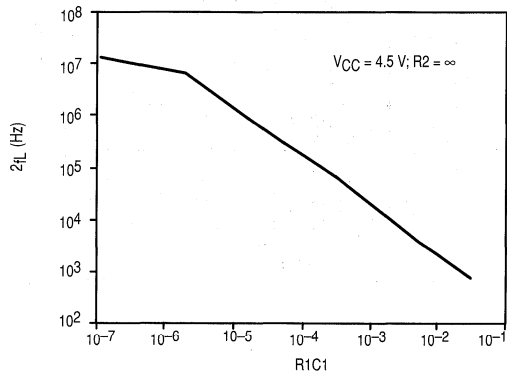


Figure 21. Typical Frequency Lock Range ( $2f_L$ ) versus  $R_1C_1$



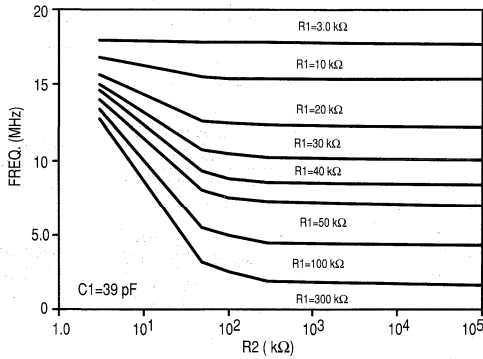


Figure 22. R2 versus  $f_{max}$

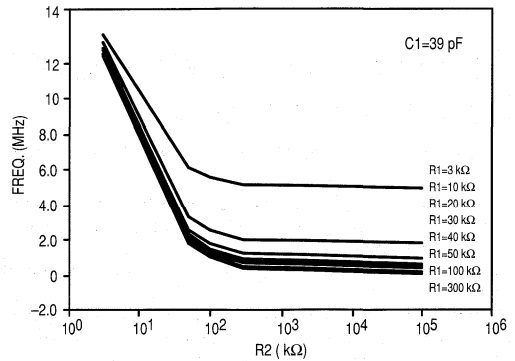


Figure 23. R2 versus  $f_{min}$

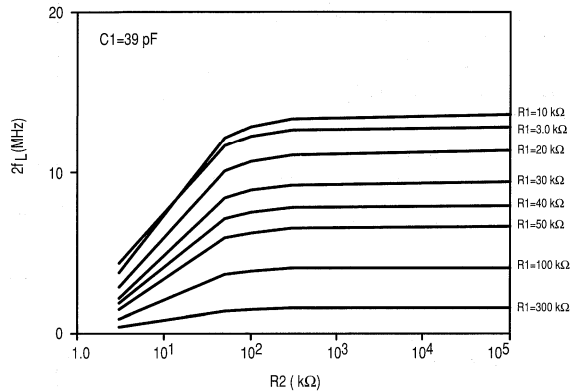


Figure 24. R2 versus Frequency Lock Range ( $2f_L$ )

**APPLICATION INFORMATION**

The following information is a guide for approximate values of R1, R2, and C1. Figures 19, 20, and 21 should be used as references as indicated below, also the values of R1, R2, and C1 should not violate the Maximum values indicated in the DC ELECTRICAL CHARACTERISTICS tables.

Phase Comparator 1		Phase Comparator 2		Phase Comparator 3	
$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$
<ul style="list-style-type: none"> <li>Given <math>f_0</math></li> <li>Use <math>f_0</math> with Figure 19 to determine R1 and C1. (see Figure 23 for characteristics of the VCO operation)</li> </ul>	<ul style="list-style-type: none"> <li>Given <math>f_0</math> and <math>f_L</math></li> <li>Calculate <math>f_{min}</math> <math>f_{min} = f_0 - f_L</math></li> <li>Determine values of C1 and R2 from Figure 20.</li> <li>Determine R1-C1 from Figure 21.</li> <li>Calculate value of R1 from the value of C1 and the product of R1C1 from Figure 21. (see Figure 24 for characteristics of the VCO operation)</li> </ul>	<ul style="list-style-type: none"> <li>Given <math>f_{max}</math> and <math>f_0</math></li> <li>Determine the value of R1 and C1 using Figure 19 and use Figure 21 to obtain <math>2f_L</math> and then use this to calculate <math>f_{min}</math>.</li> </ul>	<ul style="list-style-type: none"> <li>Given <math>f_0</math> and <math>f_L</math></li> <li>Calculate <math>f_{min}</math> <math>f_{min} = f_0 - f_L</math></li> <li>Determine values of C1 and R2 from Figure 20.</li> <li>Determine R1-C1 from Figure 21.</li> <li>Calculate value of R1 from the value of C1 and the product of R1C1 from Figure 21. (see Figure 24 for characteristics of the VCO operation)</li> </ul>	<ul style="list-style-type: none"> <li>Given <math>f_{max}</math> and <math>f_0</math></li> <li>Determine the value of R1 and C1 using Figure 19 and Figure 21 to obtain <math>2f_L</math> and then use this to calculate <math>f_{min}</math>.</li> </ul>	<ul style="list-style-type: none"> <li>Given <math>f_0</math> and <math>f_L</math></li> <li>Calculate <math>f_{min}</math>: <math>f_{min} = f_0 - f_L</math></li> <li>Determine values of C1 and R2 from Figure 20.</li> <li>Determine R1-C1 from Figure 21.</li> <li>Calculate value of R1 from the value of C1 and the product of R1C1 from Figure 21. (see Figure 24 for characteristics of the VCO operation)</li> </ul>

# Hex Buffers/Logic-Level Down Converters

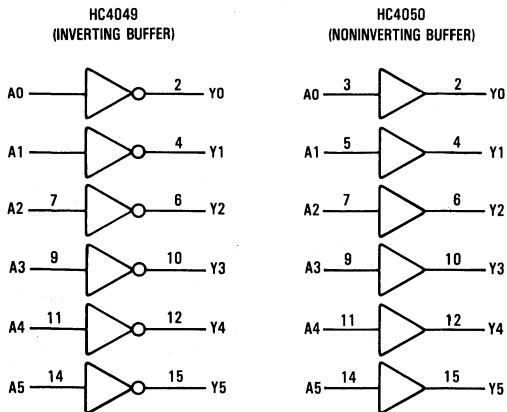
## High-Performance Silicon-Gate CMOS

The MC54/74HC4049 consists of six inverting buffers, and the MC54/74HC4050 consists of six noninverting buffers. They are identical in pinout to the MC14049UB and MC14050B metal-gate CMOS buffers. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The input protection circuitry on these devices has been modified by eliminating the V<sub>CC</sub> diodes to allow the use of input voltages up to 15 volts. Thus, the devices may be used as logic-level translators that convert from a high voltage to a low voltage while operating at the low-voltage power supply. They allow MC14000-series CMOS operating up to 15 volts to be interfaced with High-Speed CMOS at 2 to 6 volts. The protection diodes to GND are Zener diodes, which protect the inputs from both positive and negative voltage transients.

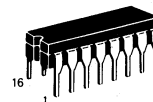
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 5  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates (4049)  
24 FETs or 6 Equivalent Gates (4050)

### LOGIC DIAGRAMS

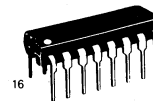


PIN 1 = V<sub>CC</sub>  
 PIN 8 = GND  
 PINS 13, 16 = NO CONNECTION

## MC54/74HC4049 MC54/74HC4050



J SUFFIX  
 CERAMIC  
 CASE 620-09



N SUFFIX  
 PLASTIC  
 CASE 648-08



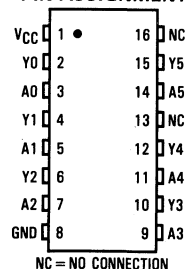
D SUFFIX  
 SOIC  
 CASE 751B-04

### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



NC = NO CONNECTION

### FUNCTION TABLE

A Inputs	Y Outputs	
	HC4049	HC4050
L	H	L
H	L	H

# MC54/74HC4049•MC54/74HC4050

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to +18	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC}+0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields **referenced to the GND pin, only**. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges  $GND \leq V_{in} \leq 15$  V and  $GND \leq V_{out} \leq V_{CC}$  are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ).

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}$	DC Input Voltage (Referenced to GND)	0	$V_{CC}$ to 15	V	
$V_{out}$	DC Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC}=2.0$ V $V_{CC}=4.5$ V $V_{CC}=6.0$ V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out}=0.1$ V or $V_{CC}-0.1$ V $ I_{out}  \leq 20$ $\mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out}=0.1$ V or $V_{CC}-0.1$ V $ I_{out}  \leq 20$ $\mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in}=V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in}=V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0$ mA $ I_{out}  \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in}=V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20$ $\mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in}=V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0$ mA $ I_{out}  \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
		$V_{in}=V_{CC}$ or GND $V_{in}=15$ V	6.0 6.0	$\pm 0.1$ 0.5	$\pm 1.0$ 5.0	$\pm 1.0$ 5.0	
$I_{in}$	Maximum Input Leakage Current	$V_{in}=V_{CC}$ or GND $V_{in}=15$ V	6.0 6.0	$\pm 0.1$ 0.5	$\pm 1.0$ 5.0	$\pm 1.0$ 5.0	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in}=15$ V or GND $I_{out}=0$ $\mu\text{A}$	6.0	2	20	40	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC4049•MC54/74HC4050

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	85	105	130	ns
		4.5	17	21	26	
		6.0	14	18	22	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> =5.0 V	pF
		27	

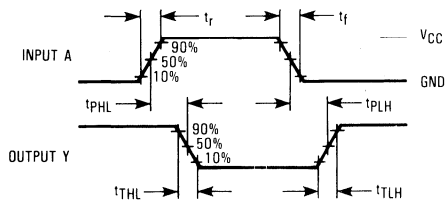


Figure 1a. Switching Waveforms (HC4049)

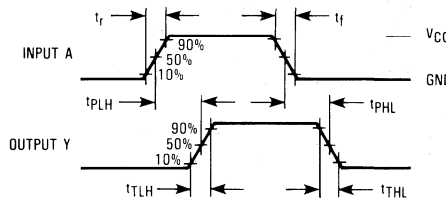
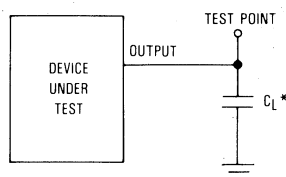


Figure 1b. Switching Waveforms (HC4050)

5



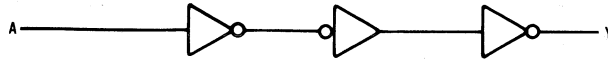
\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

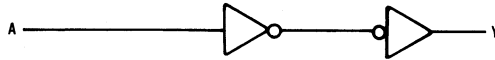
# MC54/74HC4049•MC54/74HC4050

## LOGIC DETAIL

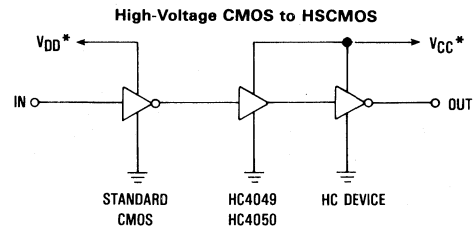
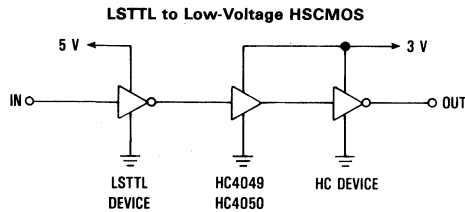
HC4049  
(1/6 of the Device)



HC4050  
(1/6 of the Device)



## TYPICAL APPLICATIONS



NOTE: To determine the noise immunity for the LSTTL to low-voltage configuration, use Eq. 1 and Eq. 2:  
 (TTL)  $V_{OH} - (\text{CMOS}) V_{IH}$  Eq. 1  
 (TTL)  $V_{OL} - (\text{CMOS}) V_{IL}$  Eq. 2

For the supply levels shown:  
 $2.4 - 3 (75\%) = 2.4 - 2.25 = 0.15 \text{ V}$   
 $0.4 - 3 (15\%) = 0.4 - 0.45 = 0.05 \text{ V}$

Therefore, worst case noise immunity is 50 mV.  
 For supply levels greater than 4.5 volts use the 74HCT04 for direct interface to TTL outputs.

\*Table 1. Supply Examples

V <sub>DD</sub>	V <sub>CC</sub>
15 V	2 V
12 V	5 V
12 V	3 V

## Analog Multiplexers/ Demultiplexers

### High-Performance Silicon-Gate CMOS

The MC54/74HC4051, MC54/74HC4052, and MC54/74HC4053 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from  $V_{CC}$  to  $V_{EE}$ ).

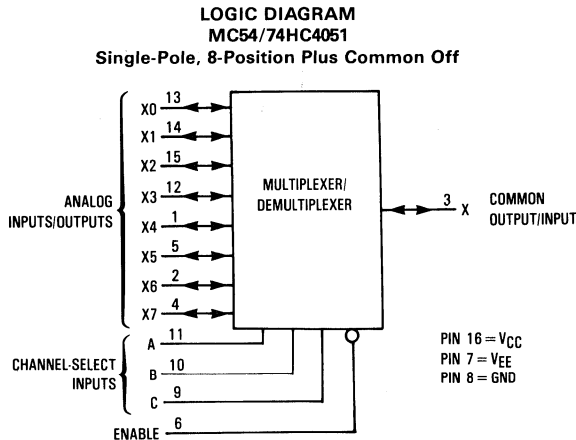
The HC4051, HC4052, and HC4053 are identical in pinout to the metal-gate MC14051B, MC14052B, and MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is high, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

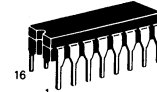
These devices have been designed so that the ON resistance ( $R_{ON}$ ) is more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

For multiplexers/demultiplexers with channel select latches, see HC4351, HC4352, and HC4353.

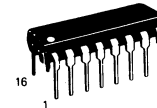
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ( $V_{CC} - V_{EE}$ ) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal-Gate Counterparts
- Low Noise
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: HC4051—184 FETs or 46 Equivalent Gates  
 HC4052—168 FETs or 42 Equivalent Gates  
 HC4053—156 FETs or 39 Equivalent Gates



## MC54/74HC4051 MC54/74HC4052 MC54/74HC4053



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



**DW SUFFIX**  
**SOIC**  
**CASE 751G-01**

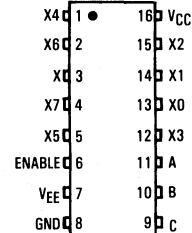
### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

$T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT

#### MC54/74HC4051



### FUNCTION TABLE

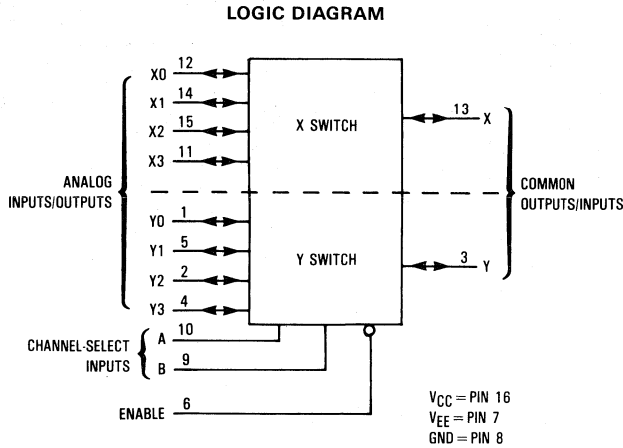
#### MC54/74HC4051

Control Inputs		ON Channels
Enable	Select	
		C B A
L	L L L	X0
L	L L H	X1
L	L H H	X2
L	H L L	X3
L	H L H	X4
L	H H L	X5
L	H H H	X6
L	H H H	X7
H	X X X	None

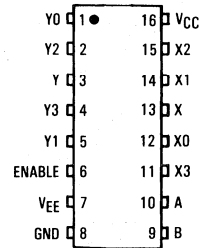
X = don't care

# MC54/74HC4051 • MC54/74HC4052 • MC54/74HC4053

## MC54/74HC4052 Double-Pole, 4-Position Plus Common Off



### PIN ASSIGNMENT

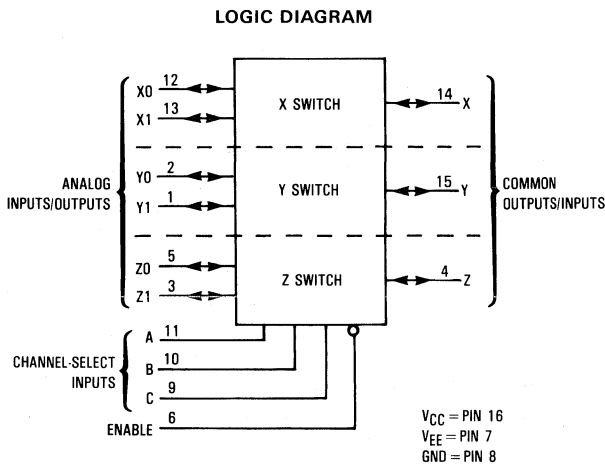


### FUNCTION TABLE

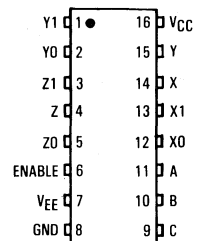
Control Inputs		Select		ON Channels	
Enable		B	A		
L	L	L	L	Y0	X0
L	L	L	H	Y1	X1
L	L	H	L	Y2	X2
L	L	H	H	Y3	X3
H	X	X	X	None	

X = Don't Care

## MC54/74HC4053 Triple Single-Pole, Double-Position Plus Common Off



### PIN ASSIGNMENT



### FUNCTION TABLE

Control Inputs		Select			ON Channels		
Enable		C	B	A			
L	L	L	L	L	Z0	Y0	X0
L	L	L	L	H	Z0	Y0	X1
L	L	L	H	L	Z0	Y1	X0
L	L	L	H	H	Z0	Y1	X1
L	L	H	L	L	Z1	Y0	X0
L	L	H	L	H	Z1	Y0	X1
L	L	H	H	L	Z1	Y1	X0
L	L	H	H	H	Z1	Y1	X1
H	X	X	X	X	None		

X = Don't Care

NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X Switch, Input B controls the Y Switch, and Input C controls the Z Switch.

# MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Ref. to GND) (Ref. to V <sub>EE</sub> )	-0.5 to +7.0 -0.5 to 14.0	V
V <sub>EE</sub>	Negative DC Supply Voltage (Ref. to GND)	-7.0 to +0.5	V
V <sub>IS</sub>	Analog Input Voltage	V <sub>EE</sub> - 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>in</sub>	Digital Input Voltage (Ref. to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
I	DC Current Into or Out of Any Pin	±25	mA
P <sub>D</sub>	Power Dissipation in Still Air Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 SOIC Package: -7 mW/°C from 65° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the ranges indicated in the Recommended Operating Conditions.

Unused digital input pins must be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused Analog I/O pins may be left open or terminated. See Applications Information.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Ref. to GND) (Ref. to V <sub>EE</sub> )	2.0 2.0	6.0 12.0	V
V <sub>EE</sub>	Negative DC Supply Voltage (Ref. to GND)	-6.0	GND	V
V <sub>IS</sub>	Analog Input Voltage	V <sub>EE</sub>	V <sub>CC</sub>	V
V <sub>in</sub>	Digital Input Voltage (Ref. to GND)	GND	V <sub>CC</sub>	V
V <sub>IO</sub> *	Static or Dynamic Voltage Across Switch	-	1.2	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time, (Channel Select or Enable Inputs)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

\*For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V<sub>EE</sub> = GND, Except Where Noted

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R <sub>on</sub> = Per Spec	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	R <sub>on</sub> = Per Spec	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
I <sub>in</sub>	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V <sub>in</sub> = V <sub>CC</sub> or GND, V <sub>EE</sub> = -6.0 V	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	Channel Select = V <sub>CC</sub> or GND Enable = V <sub>CC</sub> or GND V <sub>IS</sub> = V <sub>CC</sub> or GND V <sub>IO</sub> = 0 V  V <sub>EE</sub> = GND V <sub>EE</sub> = -6.0	6.0	2	20	40	μA
			6.0	8	80	160	
			6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

## DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V <sub>CC</sub>	V <sub>EE</sub>	Guaranteed Limit			Unit	
					25°C to -55°C	≤85°C	≤125°C		
R <sub>on</sub>	Maximum "ON" Resistance	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to V <sub>EE</sub> I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	4.5	0.0	190	240	280	Ω	
			4.5	-4.5	120	150	170		
			6.0	-6.0	100	125	140		
		V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or V <sub>EE</sub> (Endpoints) I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	4.5	0.0	150	190	230		
			4.5	-4.5	100	125	140		
			6.0	-6.0	80	100	115		
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - V <sub>EE</sub> ) I <sub>S</sub> ≤ 2.0 mA	4.5	0.0	30	35	40	Ω	
			4.5	-4.5	12	15	18		
			6.0	-6.0	10	12	14		
I <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IO</sub> = V <sub>CC</sub> - V <sub>EE</sub> Switch Off (Figure 3)	6.0	-6.0	0.1	0.5	1.0	μA	
			Maximum Off-Channel Leakage Current, Common Channel	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IO</sub> = V <sub>CC</sub> - V <sub>EE</sub> Switch Off (Figure 4)	HC4051	6.0	-6.0		0.2
	HC4052	6.0			-6.0	0.1	1.0		2.0
	HC4053	6.0			-6.0	0.1	1.0		2.0
		6.0			-6.0	0.1	1.0		2.0
	I <sub>on</sub>	Maximum On-Channel Leakage Current, Channel to Channel	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> Switch to Switch = V <sub>CC</sub> - V <sub>EE</sub> (Figure 5)	HC4051	6.0	-6.0	0.2		2.0
HC4052				6.0	-6.0	0.1	1.0	2.0	
HC4053				6.0	-6.0	0.1	1.0	2.0	
				6.0	-6.0	0.1	1.0	2.0	

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Channel-Select to Analog Output (Figure 9)	2.0	370	465	550	ns
		4.5	74	93	110	
		6.0	63	79	94	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	290	364	430	ns
		4.5	58	73	86	
		6.0	49	62	73	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	345	435	515	ns
		4.5	69	87	103	
		6.0	59	74	87	
C <sub>in</sub>	Maximum Input Capacitance, Channel-Select or Enable Inputs	—	10	10	10	pF
C <sub>I/O</sub>	Maximum Capacitance Analog I/O: All Switches Off Common O/I: HC4051 HC4052 HC4053 Feedthrough	—	35	35	35	pF
		—	130	130	130	
		—	80	80	80	
		—	50	50	50	
—	—	1.0	1.0	1.0		

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) (Figure 13) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V			pF
		45 (HC4051)	80 (HC4052)	45 (HC4053)	

5

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ADDITIONAL APPLICATION CHARACTERISTICS (GND=0.0 V)

Symbol	Parameter	Test Condition	V <sub>CC</sub> V	V <sub>EE</sub> V	Limit*			Unit
					25°C 54/74HC			
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6)	f <sub>in</sub> = 1 MHz Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub> Increase f <sub>in</sub> Frequency Until dB Meter Reads -3 dB R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	2.25	-2.25	51	52	53	MHz
			4.50	-4.50	80	95	120	
			6.00	-6.00	80	95	120	
-	Off-Channel Feedthrough Isolation (Figure 7)	f <sub>in</sub> = Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF	2.25	-2.25				dB
			4.50	-4.50				
			6.00	-6.00				
		f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	2.25	-2.25				
			4.50	-4.50				
			6.00	-6.00				
-	Feedthrough Noise, Channel Select Input to Common O/I (Figure 8)	V <sub>in</sub> ≤ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns) Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A Enable = GND R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF	2.25	-2.25				mVpp
			4.50	-4.50				
			6.00	-6.00				
		R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF	2.25	-2.25				
			4.50	-4.50				
			6.00	-6.00				
-	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051)	f <sub>in</sub> = Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF	2.25	-2.25				dB
			4.50	-4.50				
			6.00	-6.00				
		f <sub>in</sub> = 1 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	2.25	-2.25				
			4.50	-4.50				
			6.00	-6.00				
THD	Total Harmonic Distortion (Figure 14)	f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF THD = THD <sub>Measured</sub> - THD <sub>Source</sub> V <sub>IS</sub> = 4.0 V <sub>pp</sub> sine wave V <sub>IS</sub> = 8.0 V <sub>pp</sub> sine wave V <sub>IS</sub> = 11.0 V <sub>pp</sub> sine wave	2.25	-2.25			0.10	%
			4.50	-4.50			0.08	
			6.00	-6.00			0.05	

\* Limits not tested. Determined by design and verified by qualification.

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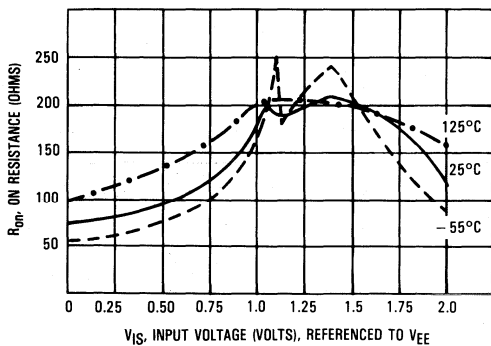


Figure 1a. Typical On Resistance,  $V_{CC} - V_{EE} = 2.0\text{ V}$

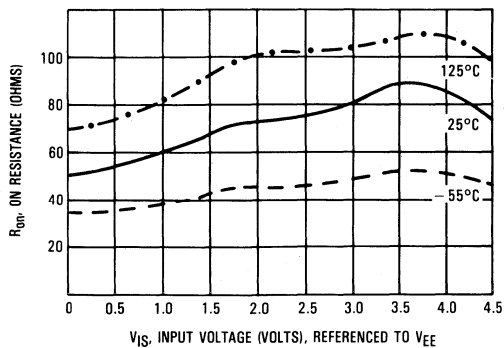


Figure 1b. Typical On Resistance,  $V_{CC} - V_{EE} = 4.5\text{ V}$

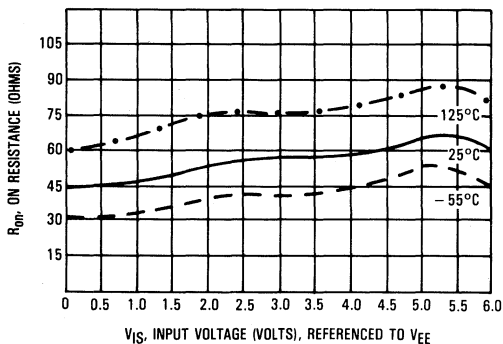


Figure 1c. Typical On Resistance,  $V_{CC} - V_{EE} = 6.0\text{ V}$

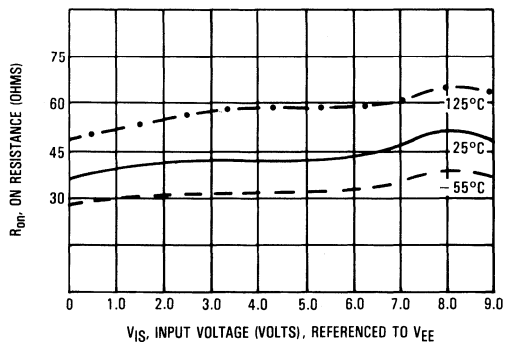


Figure 1d. Typical On Resistance,  $V_{CC} - V_{EE} = 9.0\text{ V}$

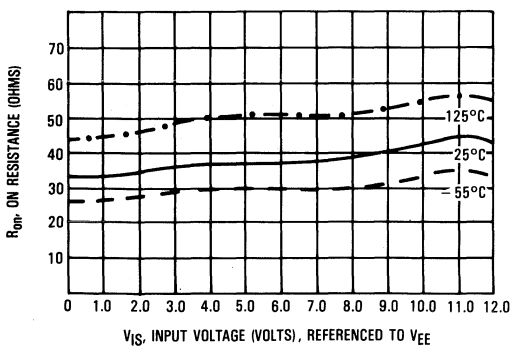


Figure 1e. Typical On Resistance,  $V_{CC} - V_{EE} = 12.0\text{ V}$

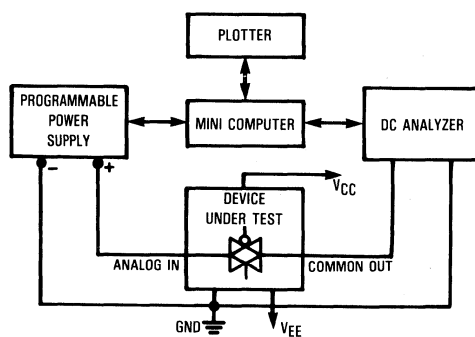


Figure 2. On Resistance Test Set-Up

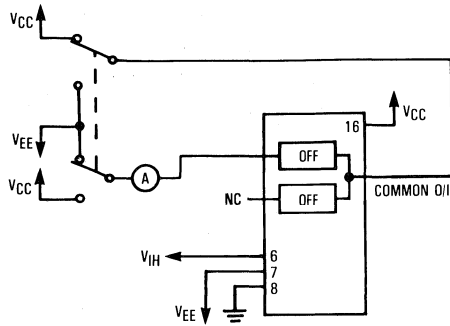


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

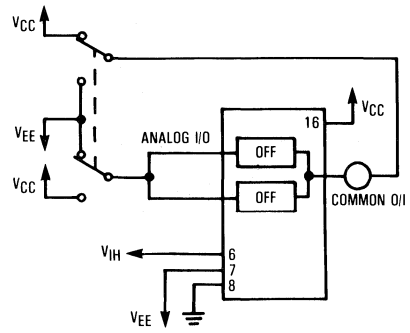


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

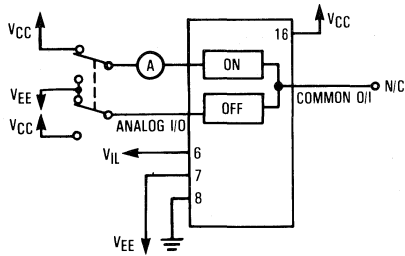
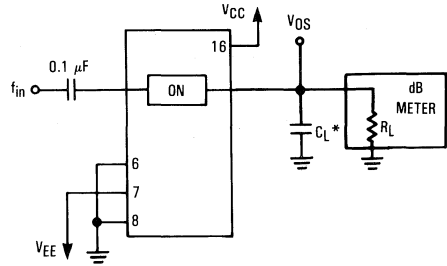
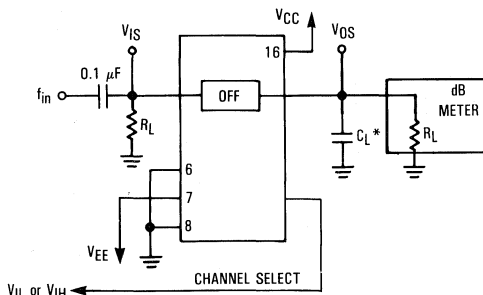


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



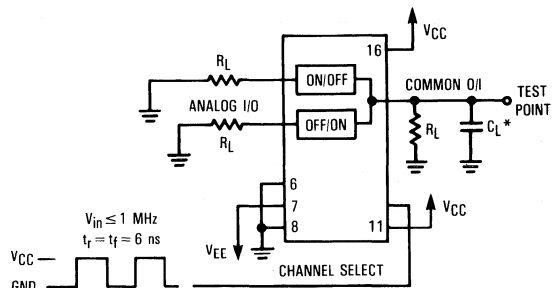
\*Includes all probe and jig capacitance.

Figure 6. Maximum On-Channel Bandwidth, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 7. Off-Channel Feedthrough Isolation, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

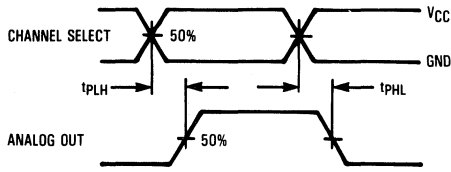
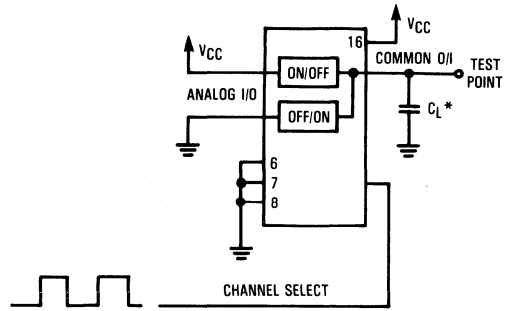


Figure 9a. Propagation Delays, Channel Select to Analog Out



\*Includes all probe and jig capacitance.

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

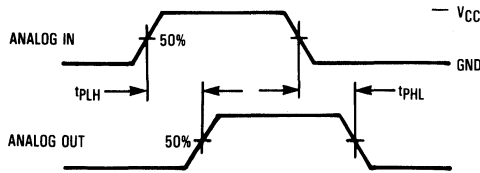
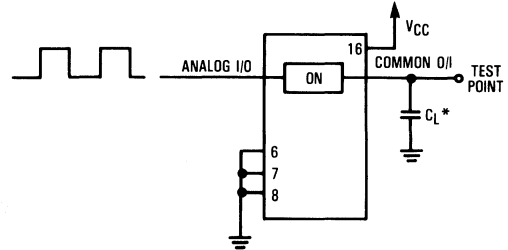


Figure 10a. Propagation Delays, Analog In to Analog Out



\*Includes all probe and jig capacitance.

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

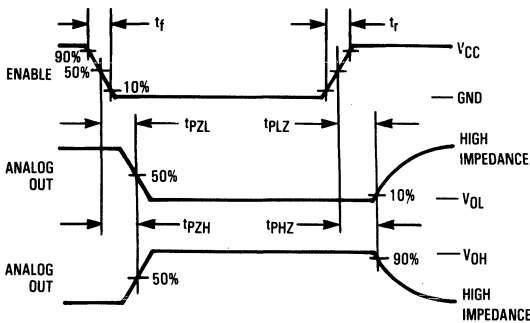


Figure 11a. Propagation Delays, Enable to Analog Out

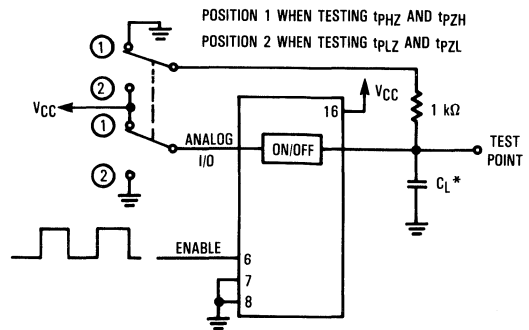
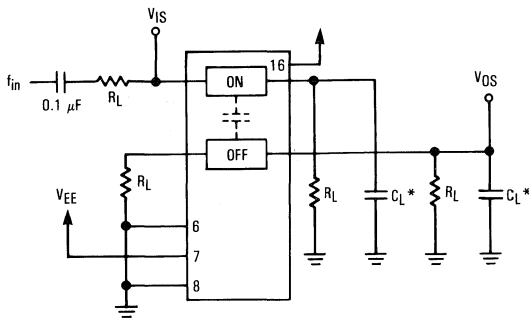


Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out



\*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

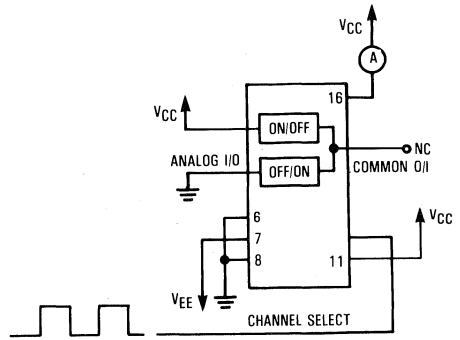
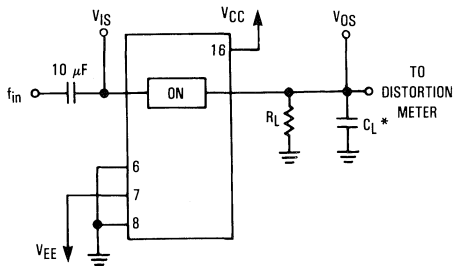


Figure 13. Power Dissipation Capacitance, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 14a. Total Harmonic Distortion, Test Set-Up

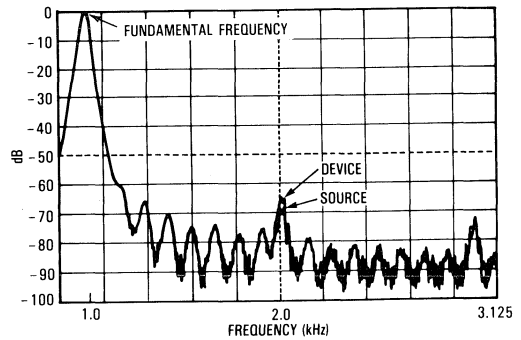


Figure 14b. Plot, Harmonic Distortion

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## APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at  $V_{CC}$  or GND logic levels.  $V_{CC}$  being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5 \text{ V} = \text{logic high} \\ \text{GND} &= 0 \text{ V} = \text{logic low} \end{aligned}$$

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and  $V_{EE}$ . The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below  $V_{EE}$ . In this example, the difference between  $V_{CC}$  and  $V_{EE}$  is ten volts. Therefore, using the configuration in Figure 15, a maximum analog signal of

ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked-up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{aligned} V_{CC} - \text{GND} &= 2 \text{ to } 6 \text{ volts} \\ V_{EE} - \text{GND} &= 0 \text{ to } -6 \text{ volts} \\ V_{CC} - V_{EE} &= 2 \text{ to } 12 \text{ volts} \\ &\text{and } V_{EE} \leq \text{GND} \end{aligned}$$

When voltage transients above  $V_{CC}$  and/or below  $V_{EE}$  are anticipated on the analog channels, external Germanium or Schottky diodes ( $D_x$ ) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

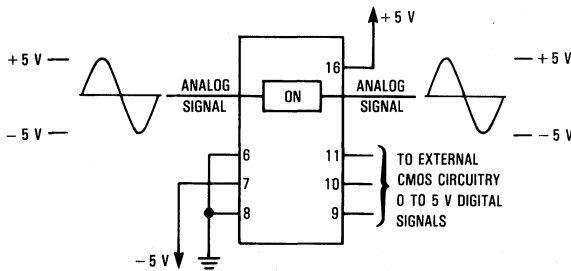


Figure 15. Application Example

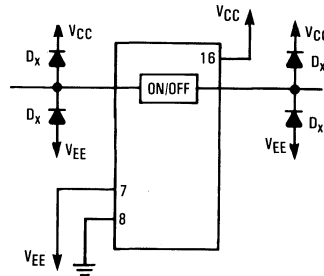
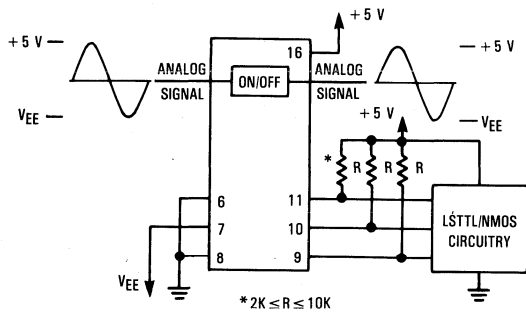
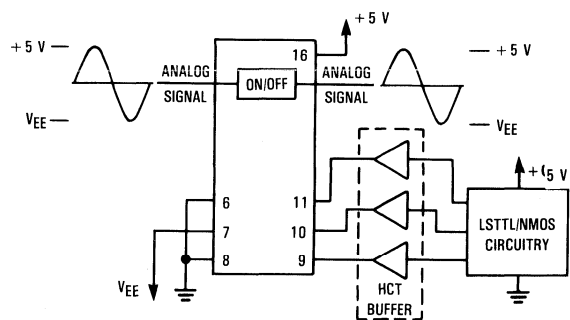


Figure 16. External Germanium or Schottky Clipping Diodes



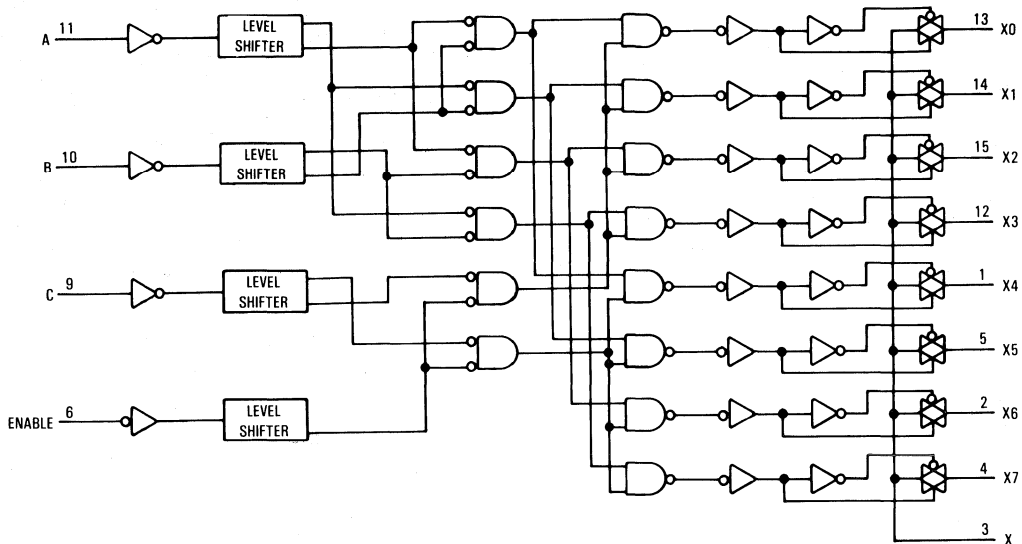
a. Using Pull-Up Resistors



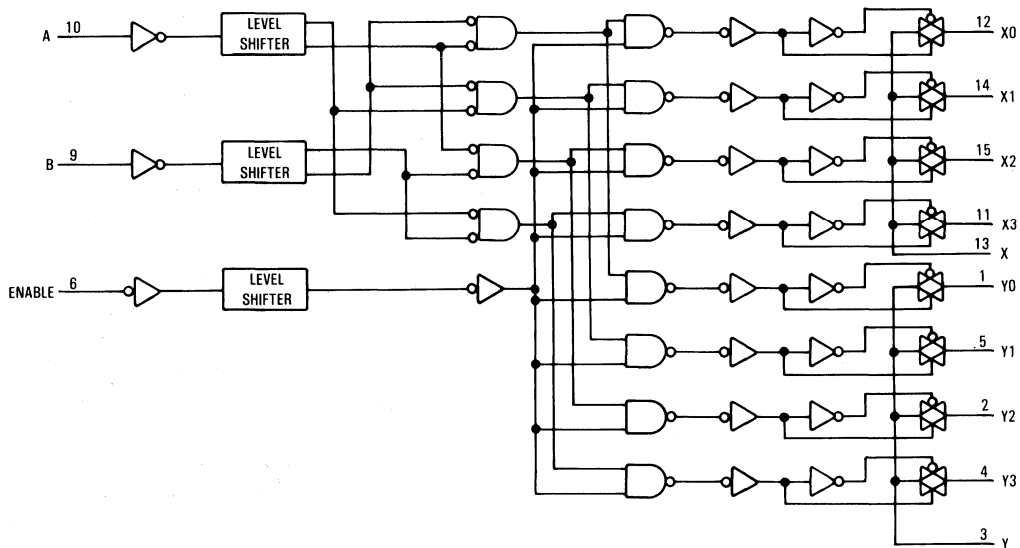
b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

FUNCTION DIAGRAM, HC4051



FUNCTION DIAGRAM, HC4052

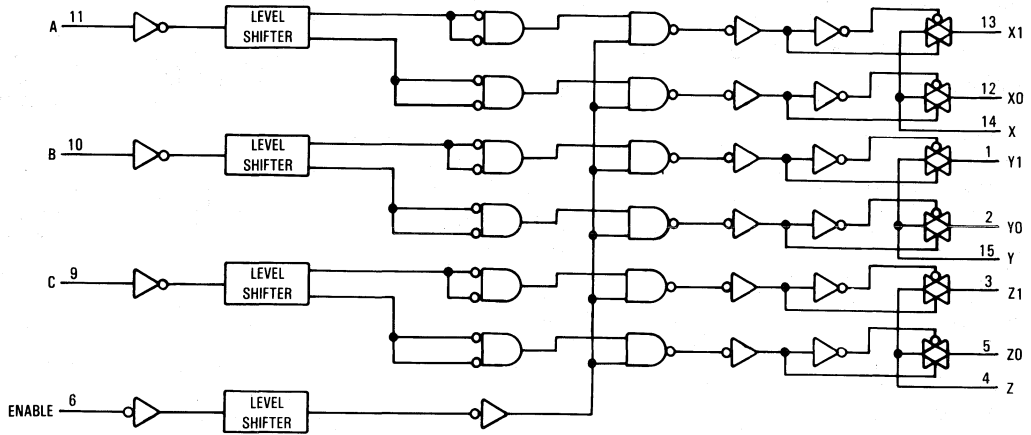


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FUNCTION DIAGRAM, HC4053



# 14-Stage Binary Ripple Counter with Oscillator

## High-Performance Silicon-Gate CMOS

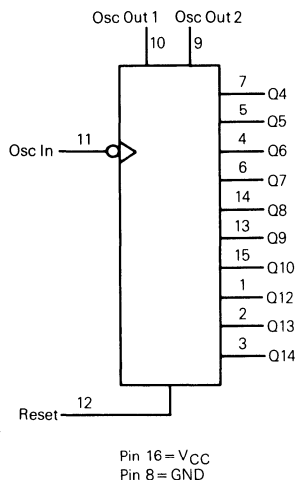
The MC54/74HC4060 is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master-slave flip-flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip-flop feeds the next, and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of Osc In. The state of the counter advances on the negative-going edge of Osc In. The active-high Reset is asynchronous and disables the oscillator to allow very low power consumption during standby operation.

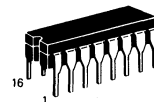
State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may need to be gated with Osc Out 2 of the HC4060.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 390 FETs or 97.5 Equivalent Gates

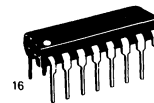
**LOGIC DIAGRAM**



### MC54/74HC4060



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**

#### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT

Q12	1	16	V <sub>CC</sub>
Q13	2	15	Q10
Q14	3	14	Q8
Q6	4	13	Q9
Q5	5	12	Reset
Q7	6	11	Osc In
Q4	7	10	Osc Out 1
GND	8	9	Osc Out 2

#### FUNCTION TABLE

Osc In	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

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# MC54/74HC4060

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260	°C
		300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 †Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
 Ceramic DIP: -10 mW/°C from 100° to 125°C  
 For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.5**	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

\*\*The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 11 with an external clock source.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage (Q4-Q10, Q12-Q14)	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage (Q4-Q10, Q12-Q14)	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
V <sub>OL</sub>	Maximum Low-Level Output Voltage (Q4-Q10, Q12-Q14)	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	V
			6.0	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	

NOTE: Information on typical parametric values can be found in Chapter 4.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) (Continued)

Symbol	Parameter	Test Conditions	VCC V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
VOH	Minimum High-Level Output Voltage (Osc Out 1, Osc Out 2)	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
VOL	Maximum Low-Level Output Voltage (Osc Out 1, Osc Out 2)	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	5.0	4.0	3.4	MHz
		4.5	25	20	17	
		6.0	29	24	20	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Osc In to Q4* (Figures 1 and 4)	2.0	530	665	795	ns
		4.5	106	133	159	
		6.0	91	114	135	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Osc In to Q14* (Figures 1 and 4)	2.0	1600	2000	2400	ns
		4.5	320	400	480	
		6.0	272	344	408	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0	240	300	360	ns
		4.5	48	60	72	
		6.0	41	51	61	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, QN to QN + 1 (Figures 3 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

**NOTES:**

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

\*For T<sub>A</sub> = 25°C and C<sub>L</sub> = 50 pF, typical propagation delay from Osc In to other Q outputs may be calculated with the following equations:

V<sub>CC</sub> = 2.0 V: t<sub>p</sub> = [205 + 107.5(N - 1)] ns

V<sub>CC</sub> = 4.5 V: t<sub>p</sub> = [41 + 21.5(N - 1)] ns

V<sub>CC</sub> = 6.0 V: t<sub>p</sub> = [35 + 18.3(N - 1)] ns

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		35	

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## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Osc In* (Figure 2)	2.0 4.5 6.0	100 25 17	125 25 21	150 30 26	ns
$t_w$	Minimum Pulse Width, Osc In (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4.

\*Osc In driven with external clock.

## PIN DESCRIPTIONS

### INPUTS

**OSC IN (PIN 11)** — Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

**RESET (PIN 12)** — Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

### OUTPUTS

**Q4-Q10, Q12-Q14 (PINS 7, 5, 4, 6, 14, 13, 15, 1, 2, 3)** — Active-high outputs. Each QN output divides the oscillator

frequency by  $2^N$ . The user should note that Q1, Q2, Q3, and Q11 are not available as outputs.

**OSC OUT 1, OSC OUT 2 (PINS 10, 9)** — Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator. (See Figures 4 and 5). When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 must be left open circuited. With the crystal oscillator configuration in Figure 6, Osc Out 2 must be left open circuited.

## SWITCHING WAVEFORMS

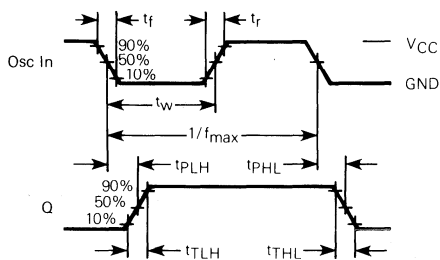


Figure 1.

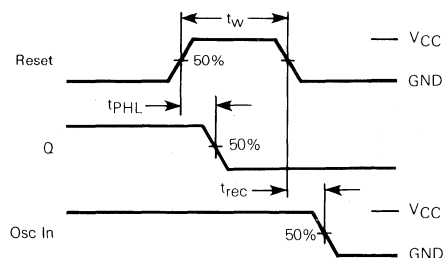


Figure 2.

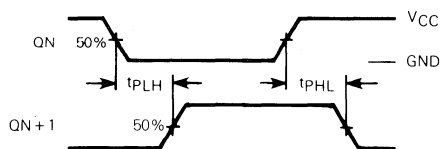
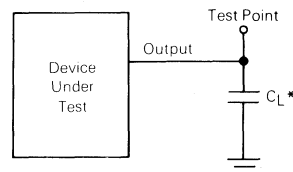


Figure 3.



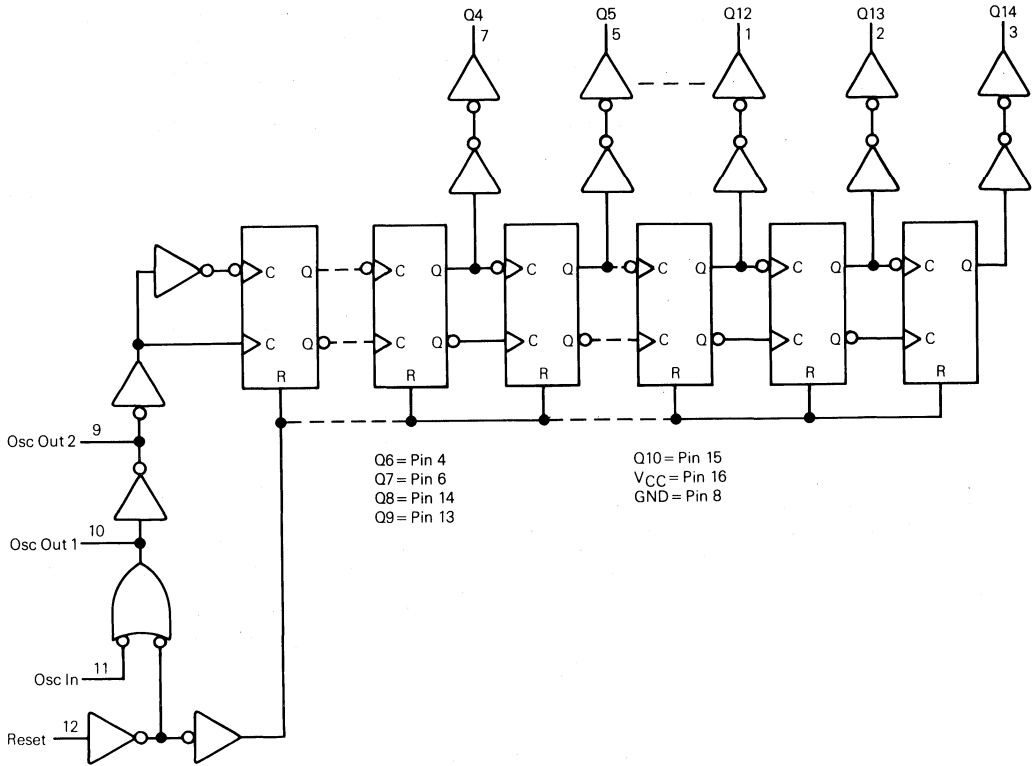
\* Includes all probe and jig capacitance.

Figure 4. Test Circuit

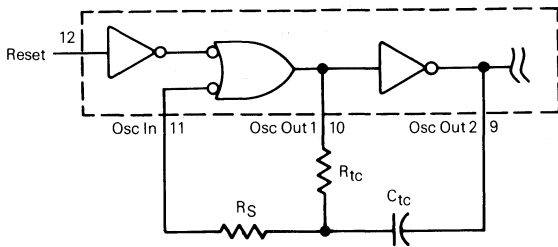
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# MC54/74HC4060

## EXPANDED LOGIC DIAGRAM



5



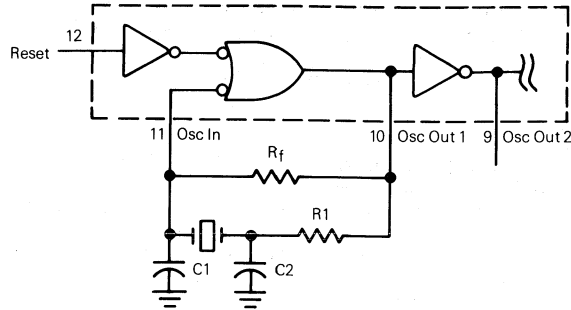
For  $2.0 \text{ V} \leq V_{CC} \leq 6.0 \text{ V}$   
 $10 R_{tc} > R_S > 2 R_{tc}$   
 $400 \text{ Hz} \leq f \leq 400 \text{ kHz}$ :

$$f \approx \frac{1}{3 R_{tc} C_{tc}} \quad (\text{if in Hz, } R_{tc} \text{ in ohms, } C_{tc} \text{ in farads})$$

The formula may vary for other frequencies.

Figure 5. Oscillator Circuit Using RC Configuration

# MC54/74HC4060



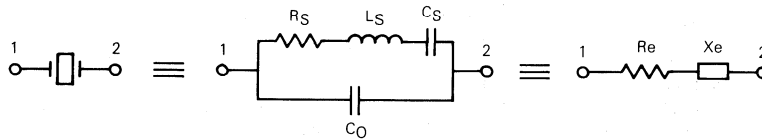
**Figure 6. Pierce Crystal Oscillator Circuit**

**Table 1. Crystal Oscillator Amplifier Specifications**

$T_A = 25^\circ\text{C}$  (Input = Pin 11, Output = Pin 10)

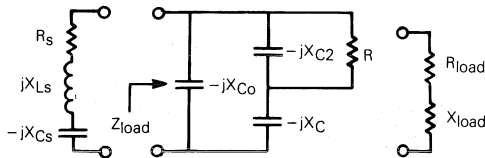
Type	Positive Reactance (Pierce)
Input Resistance, $R_{in}$	60 $\text{M}\Omega$ minimum
Output Impedance, $Z_{out}$ (4.5 V supply)	200 $\Omega$ (see text)
Input Capacitance, $C_{in}$	5 pF typical
Output Capacitance, $C_{out}$	7 pF typical
Series Capacitance, $C_a$	5 pF typical
Open loop voltage gain with output at full swing, $\alpha$	3 Vdc supply
	4 Vdc supply
	5 Vdc supply
	6 Vdc supply
	5.0 expected minimum
	4.0 expected minimum
	3.3 expected minimum
	3.1 expected minimum

## PIERCE CRYSTAL OSCILLATOR DESIGN



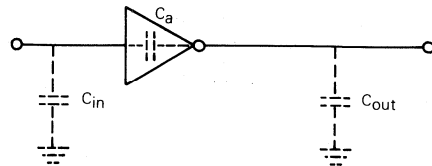
Values are supplied by crystal manufacturer (parallel resonant crystal).

**Figure 7. Equivalent Crystal Networks**



NOTE:  $C = C_1 + C_{in}$  and  $R = R_1 + R_{out}$ .  $C_o$  is considered as part of the load.  $C_a$  and  $R_f$  typically have minimal effect below 2 MHz.

**Figure 8. Series Equivalent Crystal Load**



Values are listed in Table 1.

**Figure 9. Parasitic Capacitances of the Amplifier**

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## DESIGN PROCEDURES

The following procedure applies for oscillators operating below 2 MHz where Z is a resistor R1. Above 2 MHz, additional impedance elements should be considered:  $C_{Out}$  and  $C_a$  of the amp, feedback resistor  $R_f$ , and amplifier phase shift error from  $180^\circ$ .

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{C_0}(R_s + jX_{L_s} - jX_{C_s})}{-jX_{C_0} + R_s + jX_{L_s} - jX_{C_s}} = R_e + jX_e$$

Reactance  $jX_e$  should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum  $R_s$  for the crystal should be used in the equation.

Step 2: Determine  $\beta$ , the attenuation, of the feedback network. For a closed-loop gain of 2,  $A_v\beta = 2, \beta = 2/A_v$ , where  $A_v$  is the gain of the HC4060 amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: A manufacturer may specify an external load capacitance of 32 pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate  $R_{load}$ . For example, a manufacturer specifies a crystal Q of 100,000. In-circuit Q is arbitrarily set at 20% below crystal Q or 80,000. Then  $R_{load} = (2\pi f_0 L_s / Q) - R_s$  where  $L_s$  and  $R_s$  are crystal parameters.

Step 5: Simultaneously solve, using a computer,

$$\beta = \frac{X_C \cdot X_{C2}}{R \cdot R_e + X_{C2}(X_e - X_C)} \quad (\text{with feedback phase shift} = 180^\circ) \quad (1)$$

$$X_e = X_{C2} + X_C + \frac{R_e X_{C2}}{R} = X_{Cload} \quad (\text{where the loading capacitor is an external load, not including } C_0) \quad (2)$$

$$R_{load} = \frac{R X_{C_0} X_{C2} [(X_C + X_{C2})(X_C + X_{C_0}) - X_C(X_C + X_{C_0} + X_{C2})]}{X_{C2}^2 (X_C + X_{C_0})^2 + R^2 (X_C + X_{C_0} + X_{C2})^2} \quad (3)$$

Here  $R = R_{out} + R1$ .  $R_{out}$  is amp output resistance, R1 is Z. The C corresponding to  $X_C$  is given by  $C = C1 + C_{in}$ .

Alternately, pick a value for R1 (i.e. let  $R1 = R_s$ ). Solve Equations 1 and 2 for C1 and C2. Use Equation 3 and the fact that  $Q = 2\pi f_0 L_s / (R_s + R_{load})$  to find in-circuit Q. If Q is not satisfactory pick another value for R1 and repeat the procedure.

### CHOOSING R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

### SELECTING $R_f$

The feedback resistor,  $R_f$ , typically ranges up to 20 M $\Omega$ .  $R_f$  determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone.  $R_f$  must be large enough so as to not affect the phase of the feedback network in an appreciable manner.

### ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

### ALSO RECOMMENDED FOR READING:

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

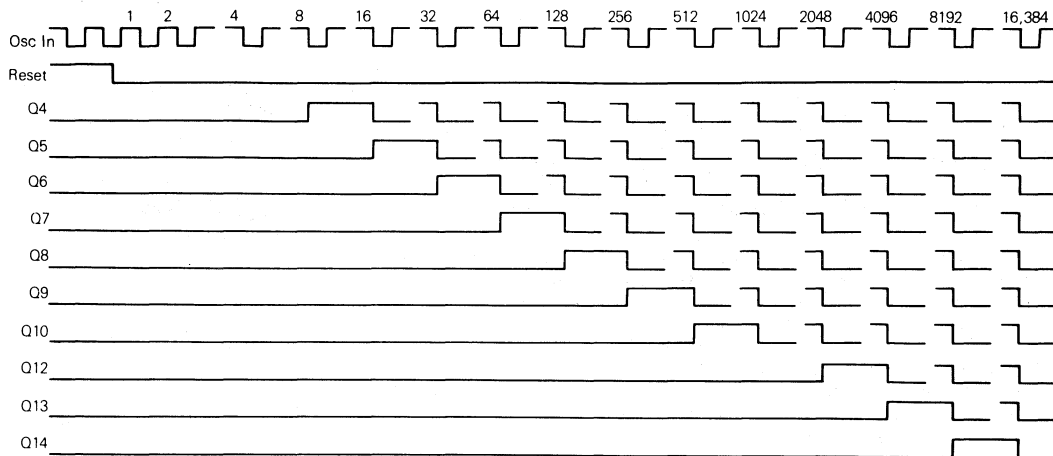
D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.



# MC54/74HC4060

## TIMING DIAGRAM



## Quad Analog Switch/ Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

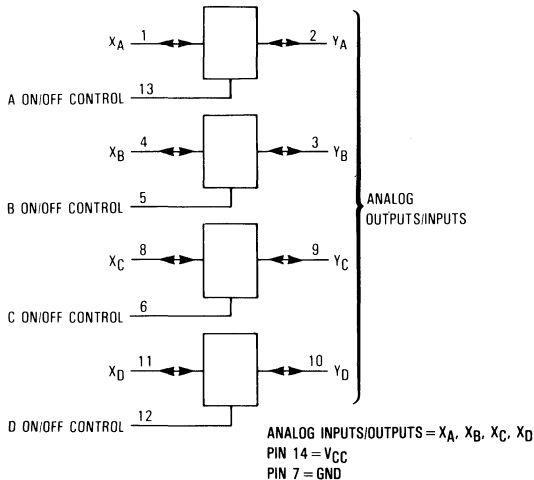
The MC54/74HC4066 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from  $V_{CC}$  to GND).

The HC4066 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances ( $R_{ON}$ ) are much more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

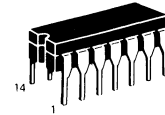
This device is identical in both function and pinout to the HC4016. The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Analog Input Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066 or HC4016
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates

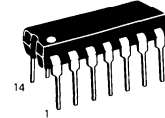
LOGIC DIAGRAM



### MC54/74HC4066



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



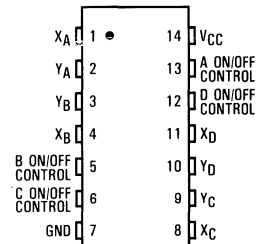
D SUFFIX  
 SOIC  
 CASE 751A-02

#### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



#### FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

# MC54/74HC4066

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND)	-0.5 to +14.0	V
V <sub>IS</sub>	Analog Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>in</sub>	Digital Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V
V <sub>IS</sub>	Analog Input Voltage (Referenced to GND)	GND	V <sub>CC</sub>	V
V <sub>in</sub>	Digital Input Voltage (Referenced to GND)	GND	V <sub>CC</sub>	V
V <sub>IO</sub> *	Static or Dynamic Voltage Across Switch	—	1.2	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)			ns
	V <sub>CC</sub> = 2.0 V	0	1000	
	V <sub>CC</sub> = 4.5 V	0	500	
	V <sub>CC</sub> = 9.0 V	0	400	
	V <sub>CC</sub> = 12.0 V	0	250	

\*For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Voltage ON/OFF Control Inputs	R <sub>on</sub> = Per Spec	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			9.0	6.3	6.3	6.3	
			12.0	8.4	8.4	8.4	
V <sub>IL</sub>	Maximum Low-Level Voltage ON/OFF Control Inputs	R <sub>on</sub> = Per Spec	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			9.0	1.8	1.8	1.8	
			12.0	2.4	2.4	2.4	
I <sub>in</sub>	Maximum Input Leakage Current, ON/OFF Control Inputs	V <sub>in</sub> = V <sub>CC</sub> or GND	12.0	± 0.1	± 1.0	± 1.0	µA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND V <sub>IO</sub> = 0 V	6.0	2	20	40	µA
			12.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.

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## DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
R <sub>on</sub>	Maximum "ON" Resistance	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to GND I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0†	—	—	—	Ω
			4.5	170	215	255	
			9.0	85	106	130	
			12.0	85	106	130	
		V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Endpoints) I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0	—	—	—	
			4.5	85	106	130	
			9.0	63	78	95	
			12.0	63	78	95	
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - GND) I <sub>S</sub> ≤ 2.0 mA	2.0	—	—	—	Ω
			4.5	30	35	40	
			9.0	20	25	30	
			12.0	20	25	30	
I <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> V <sub>IO</sub> = V <sub>CC</sub> or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I <sub>on</sub>	Maximum On-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V<sub>CC</sub> - V<sub>EE</sub>) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 4.

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, ON/OFF Control Inputs: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit	
			25°C to -55°C	≤85°C	≤125°C		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0	50	65	75	ns	
		4.5	10	13	15		
		9.0	10	13	15		
		12.0	10	13	15		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	150	190	225	ns	
		4.5	30	38	45		
		9.0	30	30	30		
		12.0	30	30	30		
t <sub>pZL</sub> , t <sub>pZH</sub>	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	125	160	185	ns	
		4.5	25	32	37		
		9.0	25	32	37		
		12.0	25	32	37		
C	Maximum Capacitance	ON/OFF Control Input	—	10	10	10	pF
		Control Input = GND	—	—	—	—	
		Analog I/O Feedthrough	—	35	35	35	
			—	1.0	1.0	1.0	

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Switch) (Figure 13) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		15	

# MC54/74HC4066

## ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f <sub>in</sub> = 1 MHz Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>O</sub> S Increase f <sub>in</sub> Frequency Until dB Meter Reads -3 dB R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off-Channel Feedthrough Isolation (Figure 6)	f <sub>in</sub> = Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>I</sub> S f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	-50 -50 -50 -40 -40 -40	dB
—	Feedthrough Noise, Control to Switch (Figure 7)	V <sub>in</sub> ≤ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns) Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	60 130 200 30 65 100	mVpp
—	Crosstalk Between Any Two Switches (Figure 12)	f <sub>in</sub> = Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>I</sub> S f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	-70 -70 -70 -80 -80 -80	dB
THD	Total Harmonic Distortion (Figure 14)	f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF THD = THD <sub>Measured</sub> - THD <sub>Source</sub> V <sub>I</sub> S = 4.0 Vpp sine wave V <sub>I</sub> S = 8.0 Vpp sine wave V <sub>I</sub> S = 11.0 Vpp sine wave	4.5 9.0 12.0	0.10 0.06 0.04	%

\*Guaranteed limits not tested. Determined by design and verified by qualification.

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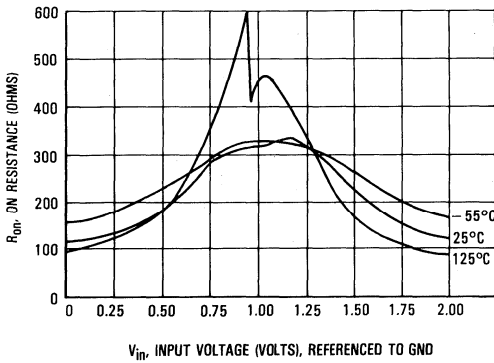


Figure 1a. Typical On Resistance,  $V_{CC} = 2.0$  V

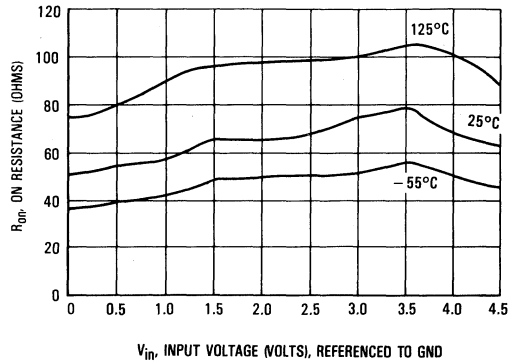


Figure 1b. Typical On Resistance,  $V_{CC} = 4.5$  V

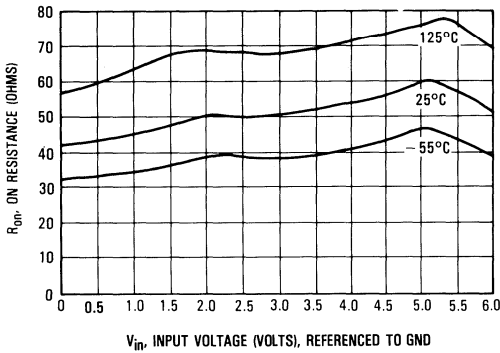


Figure 1c. Typical On Resistance,  $V_{CC} = 6.0$  V

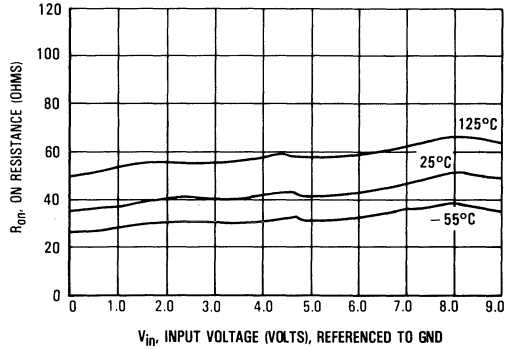


Figure 1d. Typical On Resistance,  $V_{CC} = 9.0$  V

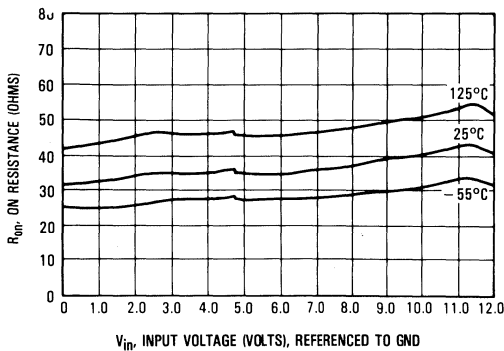


Figure 1e. Typical On Resistance,  $V_{CC} = 12.0$  V

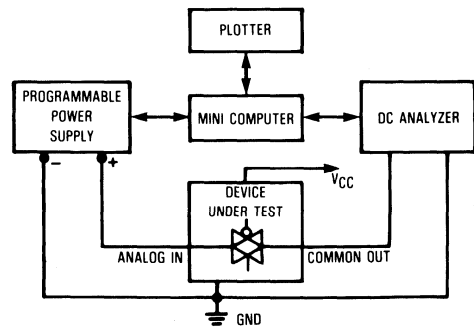


Figure 2. On Resistance Test Set-Up

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# MC54/74HC4066

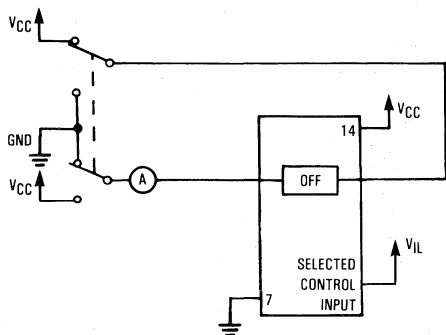


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

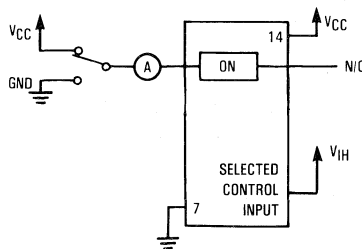
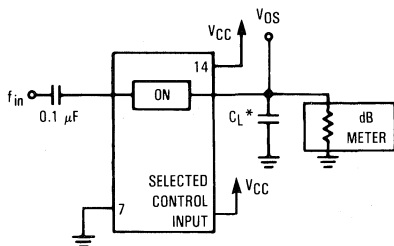
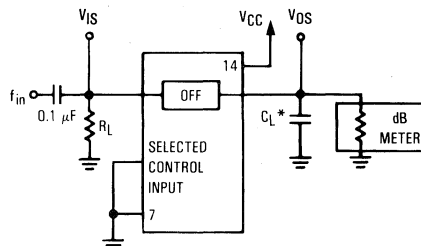


Figure 4. Maximum On Channel Leakage Current, Test Set-Up



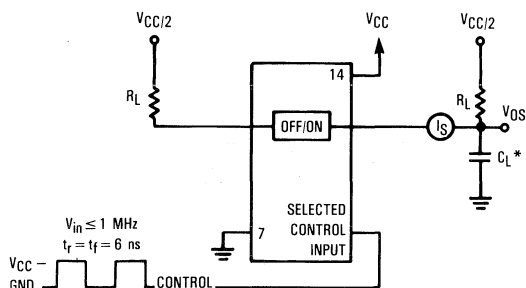
\*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth Test Set-Up



\*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

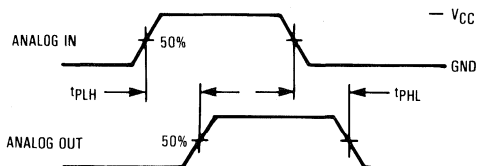
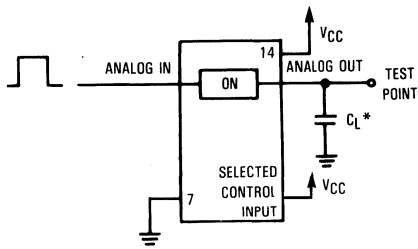


Figure 8. Propagation Delays, Analog In to Analog Out

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\*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

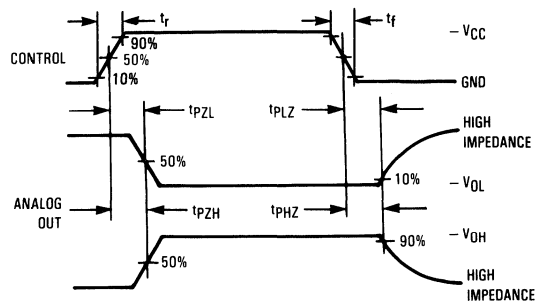
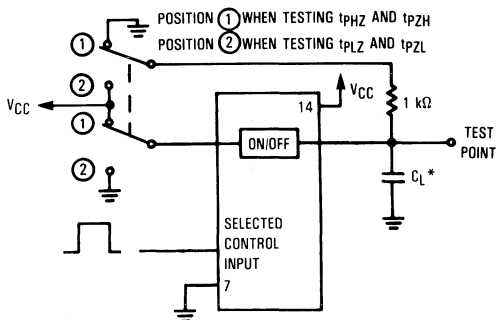
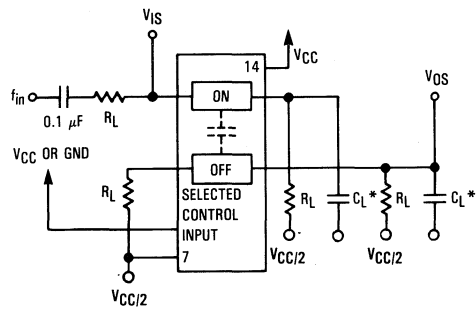


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



\*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



\*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

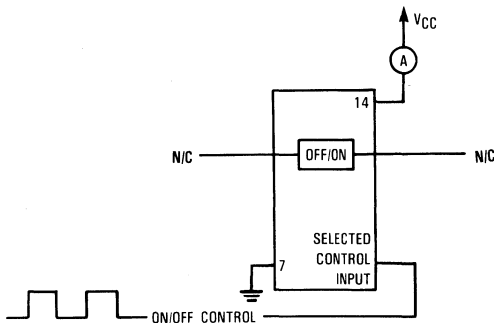
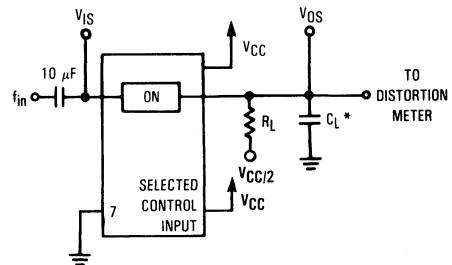


Figure 13. Power Dissipation Capacitance Test Set-Up



\*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up



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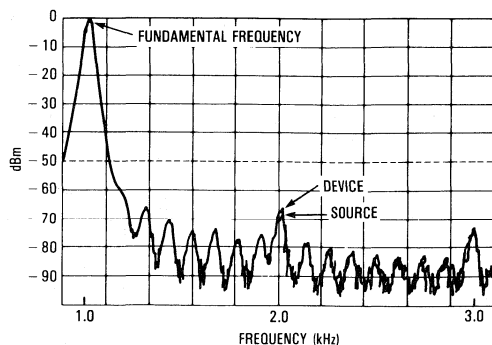


Figure 15. Plot, Harmonic Distortion

## APPLICATION INFORMATION

The ON/OFF Control pins should be at  $V_{CC}$  or GND logic levels,  $V_{CC}$  being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked-up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and GND. The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below GND. In the example below,

the difference between  $V_{CC}$  and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above  $V_{CC}$  and/or below GND are anticipated on the analog channels, external diodes ( $D_x$ ) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the  $D_x$  diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear out mechanism.

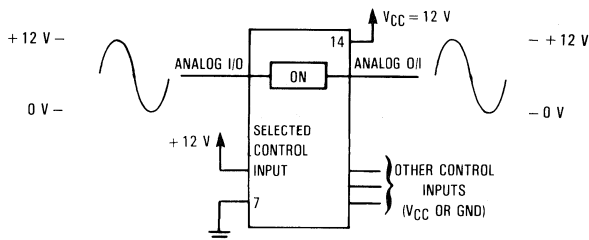


Figure 16. 12 V Application

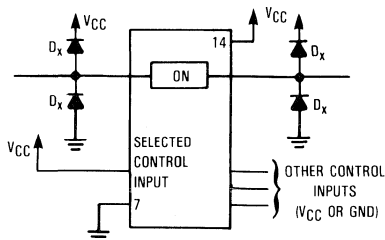


Figure 17. Transient Suppressor Application

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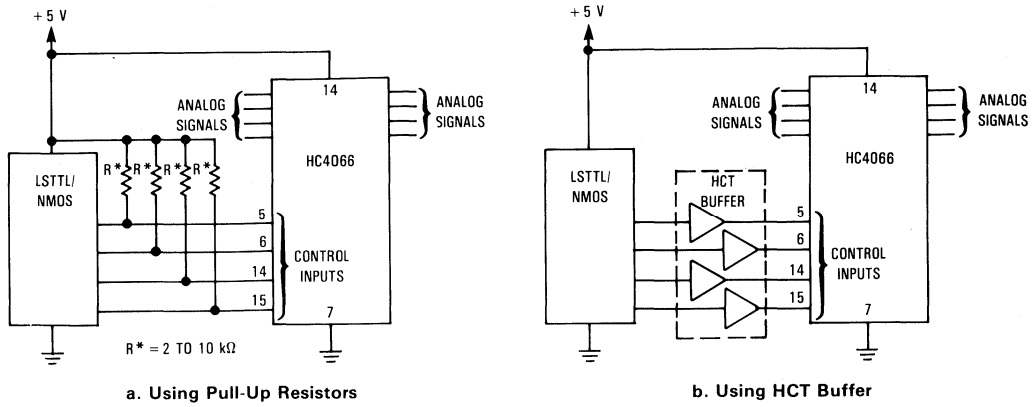


Figure 18. LSTTL/NMOS to HCMOS Interface

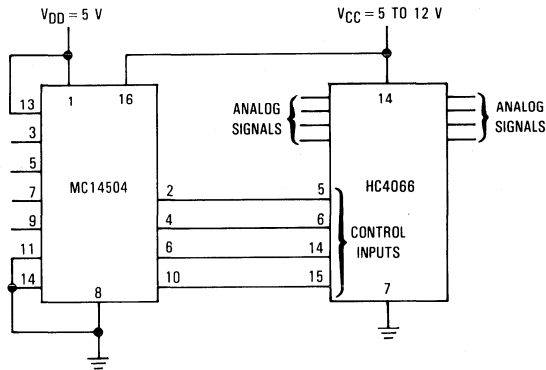


Figure 19. TTL/NMOS-to-CMOS Level Converter  
Analog Signal Peak-to-Peak Greater than 5 V  
(Also see HC4316)

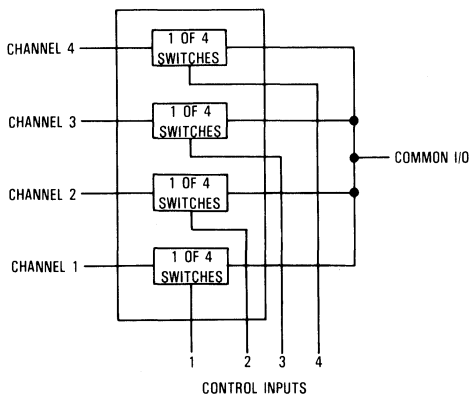


Figure 20. 4-Input Multiplexer

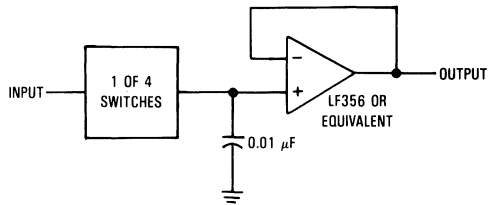


Figure 21. Sample/Hold Amplifier

5

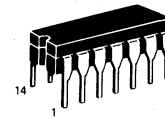
## Triple 3-Input OR Gate

### High-Performance Silicon-Gate CMOS

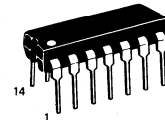
The MC54/74HC4075 is identical in pinout to the MC14075B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates

## MC54/74HC4075



**J SUFFIX**  
**CERAMIC**  
**CASE 632-08**



**N SUFFIX**  
**PLASTIC**  
**CASE 646-06**



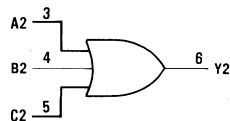
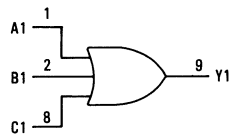
**D SUFFIX**  
**SOIC**  
**CASE 751A-02**

### ORDERING INFORMATION

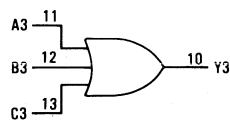
MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### LOGIC DIAGRAM

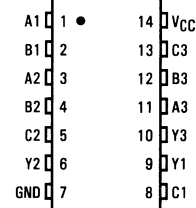


$$Y = A + B + C$$



PIN 14 =  $V_{CC}$   
 PIN 7 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs			Output
A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

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## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	2.0	±0.1	±1.0	±1.0	μA
			4.5				
			6.0				
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	2.0	2	20	40	μA
			4.5				
			6.0				

NOTE: Information on typical parametric values can be found in Chapter 4.

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## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

$C_{PD}$	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	
			26

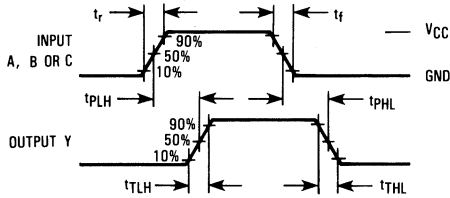
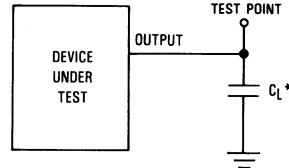


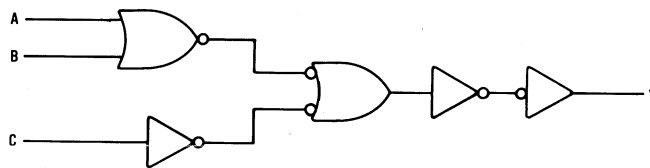
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### EXPANDED LOGIC DIAGRAM (1/4 of the Device)



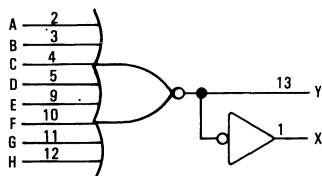
## 8-Input NOR/OR Gate

### High-Performance Silicon-Gate CMOS

The MC54/74HC4078 is similar to the CD4078B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 30 FETs or 7.5 Equivalent Gates

#### LOGIC DIAGRAM

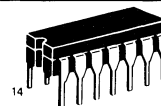


$$Y = \overline{A + B + C + D + E + F + G + H}$$

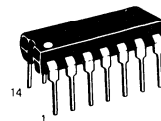
$$X = A + B + C + D + E + F + G + H$$

PIN 14 =  $V_{CC}$   
 PIN 7 = GND  
 PINS 6, 8 = NO CONNECTION

## MC54/74HC4078



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



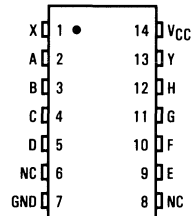
D SUFFIX  
 SOIC  
 CASE 751A-02

#### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

#### PIN ASSIGNMENT



NC = NO CONNECTION

#### FUNCTION TABLE

Inputs A through H	Outputs	
	Y	X
All inputs L	H	L
All other combinations	L	H

# MC54/74HC4078

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC4078

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 3)	2.0	130	165	195	ns
		4.5	26	33	39	
		6.0	22	28	33	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Any Input to Output X (Figures 2 and 3)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1, 2, and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		29	

## SWITCHING WAVEFORMS

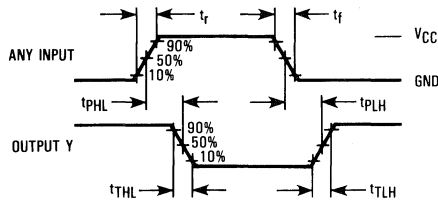


Figure 1

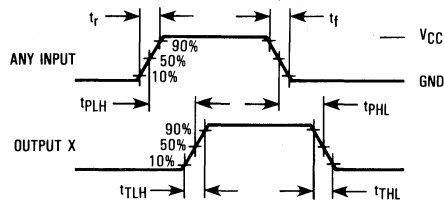
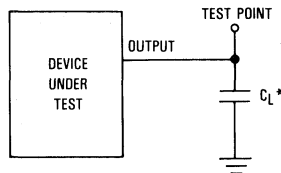


Figure 2



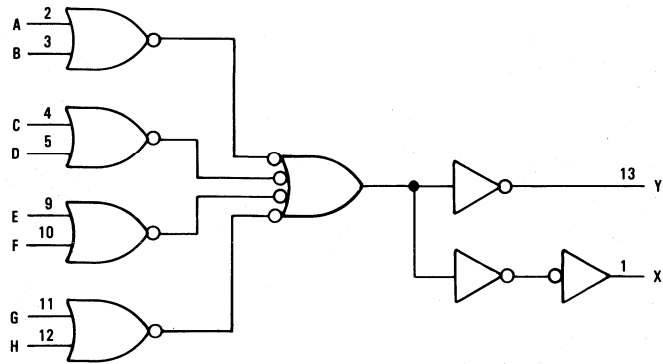
\*Includes all probe and jig capacitance.

Figure 3. Test Circuit



# MC54/74HC4078

## EXPANDED LOGIC DIAGRAM



# Quad Analog Switch/ Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies

## High-Performance Silicon-Gate CMOS

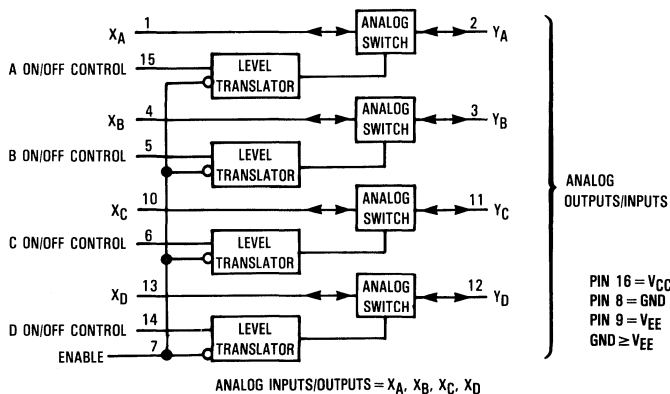
The MC54/74HC4316 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full analog power-supply range (from  $V_{CC}$  to  $V_{EE}$ ).

The HC4316 is similar in function to the metal-gate CMOS MC14016 and MC14066, and to the High-Speed CMOS HC4016 and HC4066. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances ( $R_{ON}$ ) are much more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches. Logic-level translators are provided so that the On/Off Control and Enable logic-level voltages need only be  $V_{CC}$  and GND, while the switch is passing signals ranging between  $V_{CC}$  and  $V_{EE}$ . When the Enable pin (active-low) is high, all four analog switches are turned off.

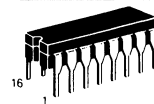
- Logic-Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range ( $V_{CC} - V_{EE}$ ) = 2.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 Volts, Independent of  $V_{EE}$
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates

5

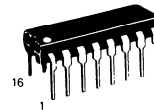
**LOGIC DIAGRAM**



## MC54/74HC4316



J SUFFIX  
 CERAMIC  
 CASE 620-09



N SUFFIX  
 PLASTIC  
 CASE 648-08



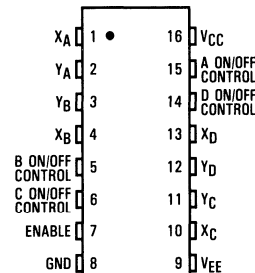
D SUFFIX  
 SOIC  
 CASE 751B-04

### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		State of Analog Switch
Enable	On/Off Control	
L	H	On
L	L	Off
H	X	Off

X = don't care

# MC54/74HC4316

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Ref. to GND) (Ref. to V <sub>EE</sub> )	-0.5 to +7.0 -0.5 to +14.0	V
V <sub>EE</sub>	Negative DC Supply Voltage (Ref. to GND)	-7.0 to +0.5	V
V <sub>IS</sub>	Analog Input Voltage	V <sub>EE</sub> - 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>in</sub>	Digital Input Voltage (Ref. to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
I	DC Current Into or Out of Any Pin	±25	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	Positive DC Supply Voltage (Ref. to GND)	2.0	6.0	V	
V <sub>EE</sub>	Negative DC Supply Voltage (Ref. to GND)	-6.0	GND	V	
V <sub>IS</sub>	Analog Input Voltage	V <sub>EE</sub>	V <sub>CC</sub>	V	
V <sub>in</sub>	Digital Input Voltage (Ref. to GND)	GND	V <sub>CC</sub>	V	
V <sub>IO</sub> *	Static or Dynamic Voltage Across Switch	-	1.2	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Control or Enable Inputs) (Figure 10)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

\*For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V<sub>EE</sub> = GND Except Where Noted

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit	
				25°C to -55°C	≤85°C	≤125°C		
V <sub>IH</sub>	Minimum High-Level Voltage, Control or Enable Inputs	R <sub>on</sub> = Per Spec	2.0	1.5	1.5	1.5	V	
			4.5	3.15	3.15	3.15		
			6.0	4.2	4.2	4.2		
V <sub>IL</sub>	Maximum Low-Level Voltage, Control or Enable Inputs	R <sub>on</sub> = Per Spec	2.0	0.3	0.3	0.3	V	
			4.5	0.9	0.9	0.9		
			6.0	1.2	1.2	1.2		
I <sub>in</sub>	Maximum Input Leakage Current, Control or Enable Inputs	V <sub>in</sub> = V <sub>CC</sub> or GND V <sub>EE</sub> = -6.0 V	6.0	±0.1	±1.0	±1.0	μA	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND V <sub>IO</sub> = 0 V	V <sub>EE</sub> = GND	6.0	2	20	40	μA
			V <sub>EE</sub> = -6.0	6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.

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# MC54/74HC4316

## DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to V<sub>EE</sub>)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	V <sub>EE</sub> V	Guaranteed Limit			Unit
					25°C to -55°C	≤85°C	≤125°C	
R <sub>on</sub>	Maximum "ON" Resistance	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to V <sub>EE</sub> I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0*	0.0	—	—	—	Ω
			4.5	0.0	320	400	480	
			4.5	-4.5	170	215	255	
			6.0	-6.0	170	215	255	
		V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or V <sub>EE</sub> (Endpoints) I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0	0.0	—	—	—	
			4.5	0.0	180	225	270	
			4.5	-4.5	135	170	205	
			6.0	-6.0	135	170	205	
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - V <sub>EE</sub> ) I <sub>S</sub> ≤ 2.0 mA	2.0	0.0	—	—	—	Ω
			4.5	0.0	30	35	40	
			4.5	-4.5	20	25	30	
			6.0	-6.0	20	25	30	
			6.0	-6.0	20	25	30	
I <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> V <sub>IO</sub> = V <sub>CC</sub> or V <sub>EE</sub> Switch Off (Figure 3)	6.0	-6.0	0.1	0.5	1.0	μA
I <sub>on</sub>	Maximum On-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Figure 4)	6.0	-6.0	0.1	0.5	1.0	μA

\*At supply voltage (V<sub>CC</sub> - V<sub>EE</sub>) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 4.

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Control or Enable: t<sub>r</sub> = t<sub>f</sub> = 6 ns, V<sub>EE</sub> = GND)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit	
			25°C to -55°C	≤85°C	≤125°C		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0	60	75	90	ns	
		4.5	12	15	18		
		6.0	10	13	15		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0	250	315	375	ns	
		4.5	50	63	75		
		6.0	43	54	64		
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0	265	335	400	ns	
		4.5	53	66	80		
		6.0	45	56	68		
C	Maximum Capacitance	ON/OFF Control and Enable Inputs Control Input = GND Analog I/O Feedthrough	—	10	10	10	pF
			—	35	35	35	
			—	1.0	1.0	1.0	

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Switch) (Figure 13) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		15	

# MC54/74HC4316

## ADDITIONAL APPLICATION CHARACTERISTICS (GND=0 V)

Symbol	Parameter	Test Conditions	VCC V	VEE V	Limit* 25°C	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	$f_{in} = 1$ MHz Sine Wave Adjust $f_{in}$ Voltage to Obtain 0 dBm at $V_{OS}$ Increase $f_{in}$ Frequency Until dB Meter Reads -3 dB $R_L = 50 \Omega$ , $C_L = 10$ pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	150 160 160	MHz
-	Off-Channel Feedthrough Isolation (Figure 6)	$f_{in} =$ Sine Wave Adjust $f_{in}$ Voltage to Obtain 0 dBm at $V_{IS}$ $f_{in} = 10$ kHz, $R_L = 600 \Omega$ , $C_L = 50$ pF $f_{in} = 1.0$ MHz, $R_L = 50 \Omega$ , $C_L = 10$ pF	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	-50 -50 -50 -40 -40 -40	dB
-	Feedthrough Noise, Control to Switch (Figure 7)	$V_{in} \leq 1$ MHz Square Wave ( $t_r = t_f = 6$ ns) Adjust $R_L$ at Setup so that $I_S = 0$ A $R_L = 600 \Omega$ , $C_L = 50$ pF $R_L = 10$ k $\Omega$ , $C_L = 10$ pF	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	60 130 200 30 65 100	mVpp
-	Crosstalk Between Any Two Switches (Figure 12)	$f_{in} =$ Sine Wave Adjust $f_{in}$ Voltage to Obtain 0 dBm at $V_{IS}$ $f_{in} = 10$ kHz, $R_L = 600 \Omega$ , $C_L = 50$ pF $f_{in} = 1.0$ MHz, $R_L = 50 \Omega$ , $C_L = 10$ pF	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	-70 -70 -70 -80 -80 -80	dB
THD	Total Harmonic Distortion (Figure 14)	$f_{in} = 1$ kHz, $R_L = 10$ k $\Omega$ , $C_L = 50$ pF $THD = THD_{Measured} - THD_{Source}$ $V_{IS} = 4.0$ Vpp sine wave $V_{IS} = 8.0$ Vpp sine wave $V_{IS} = 11.0$ Vpp sine wave	2.25 4.50 6.00	-2.25 -4.50 -6.00	0.10 0.06 0.04	%

\*Limits not tested. Determined by design and verified by qualification.

# MC54/74HC4316

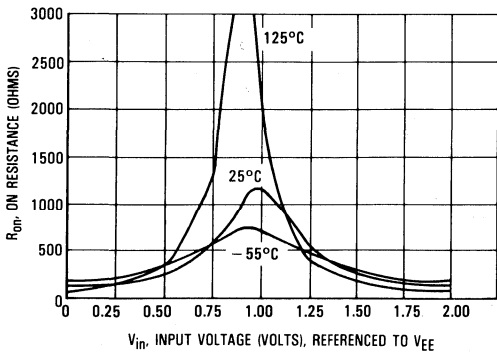


Figure 1a. Typical On Resistance,  $V_{CC} - V_{EE} = 2.0$  V

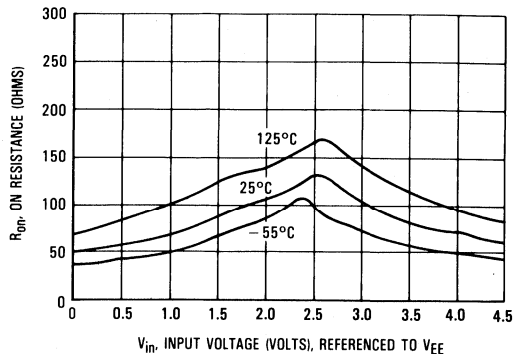


Figure 1b. Typical On Resistance,  $V_{CC} - V_{EE} = 4.5$  V

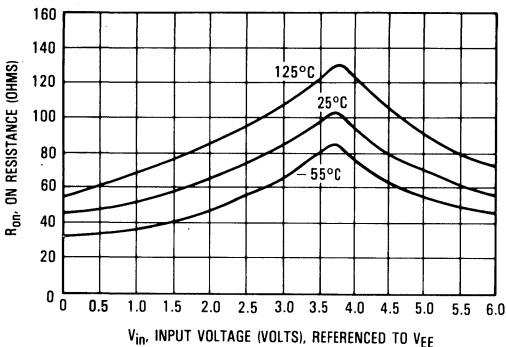


Figure 1c. Typical On Resistance,  $V_{CC} - V_{EE} = 6.0$  V

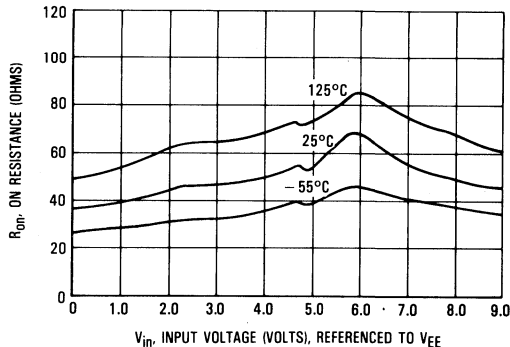


Figure 1d. Typical On Resistance,  $V_{CC} - V_{EE} = 9.0$  V

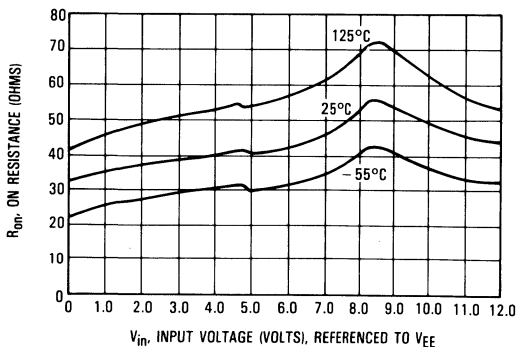


Figure 1e. Typical On Resistance,  $V_{CC} - V_{EE} = 12.0$  V

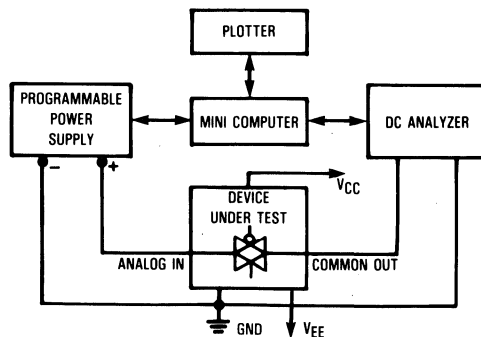


Figure 2. On Resistance Test Set-Up

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# MC54/74HC4316

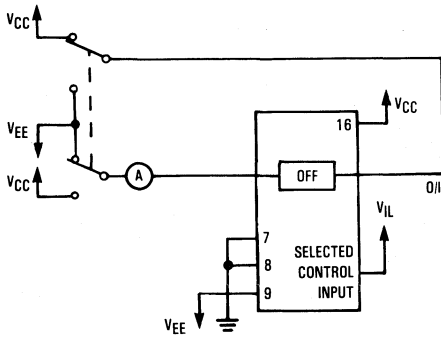


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

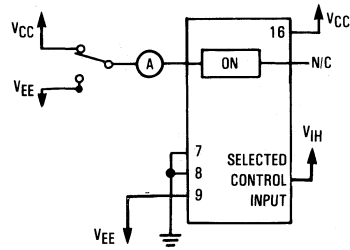
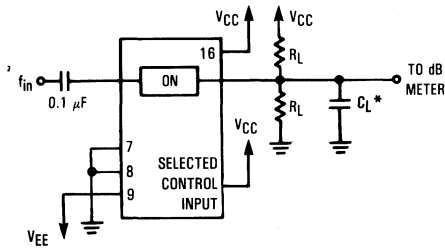
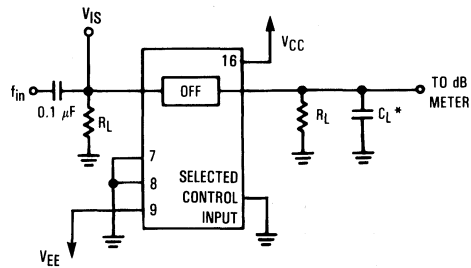


Figure 4. Maximum On Channel Leakage Current, Test Set-Up



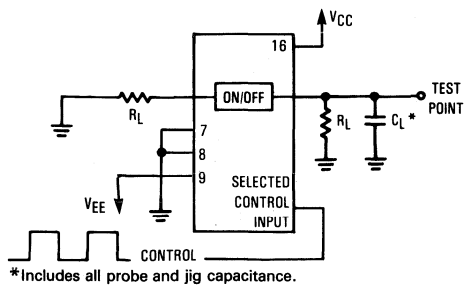
\*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth Test Set-Up



\*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up



\*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, Control to Analog Out, Test Set-Up

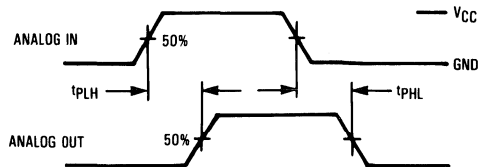
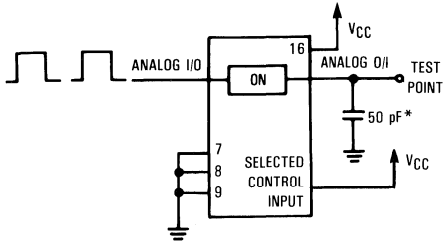


Figure 8. Propagation Delays, Analog in to Analog Out

# MC54/74HC4316



\*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

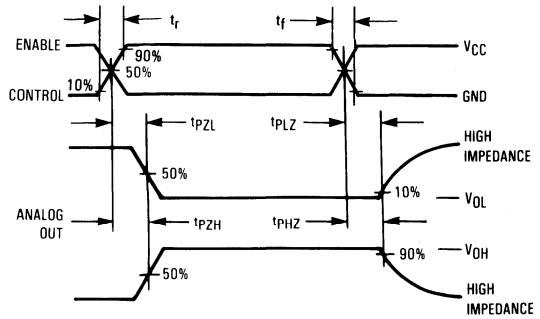
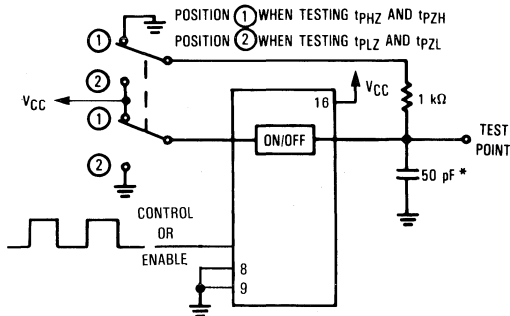
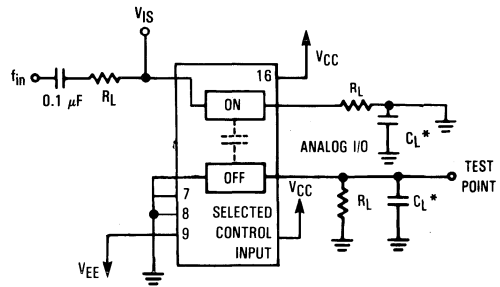


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



\*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



\*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up (Adjacent Channels Used)

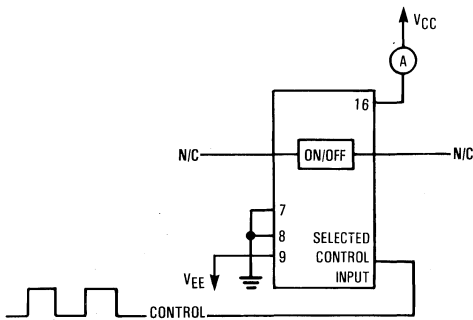
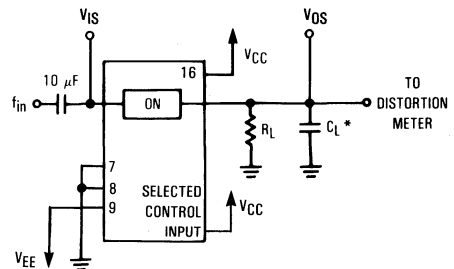


Figure 13. Power Dissipation Capacitance Test Set-Up



\*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up



# MC54/74HC4316

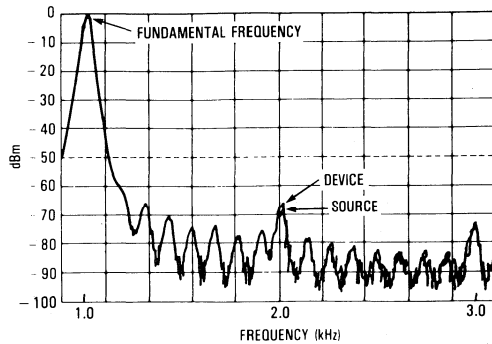


Figure 15. Plot, Harmonic Distortion

## APPLICATION INFORMATION

The Enable and Control pins should be at  $V_{CC}$  or GND logic levels,  $V_{CC}$  being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or  $V_{EE}$  through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and  $V_{EE}$ . The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below  $V_{EE}$ . In the example below,

the difference between  $V_{CC}$  and  $V_{EE}$  is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above  $V_{CC}$  and/or below  $V_{EE}$  are anticipated on the analog channels, external diodes ( $D_x$ ) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the  $D_x$  diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn-on devices ideally suited for precise dc protection with no inherent wear out mechanism.

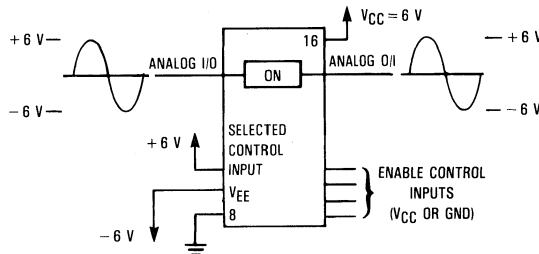


Figure 16

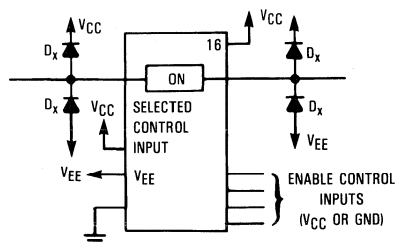


Figure 17. Transient Suppressor Application

# MC54/74HC4316

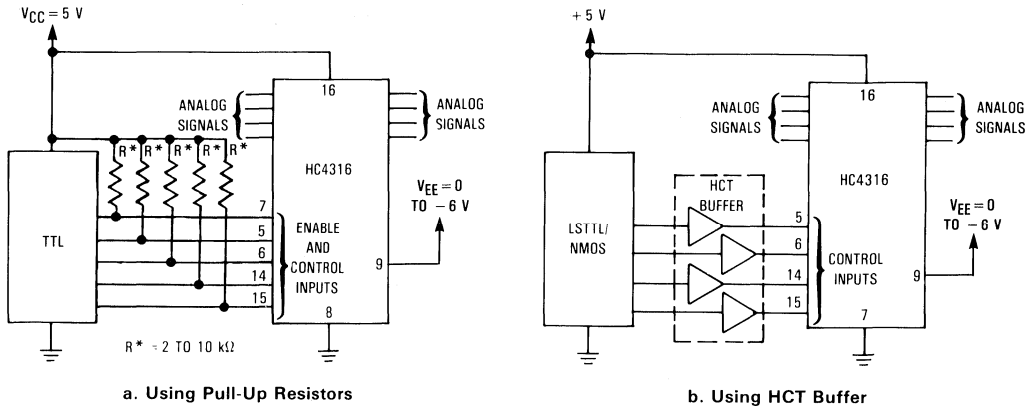


Figure 18. LSTTL/NMOS to HCMOS Interface

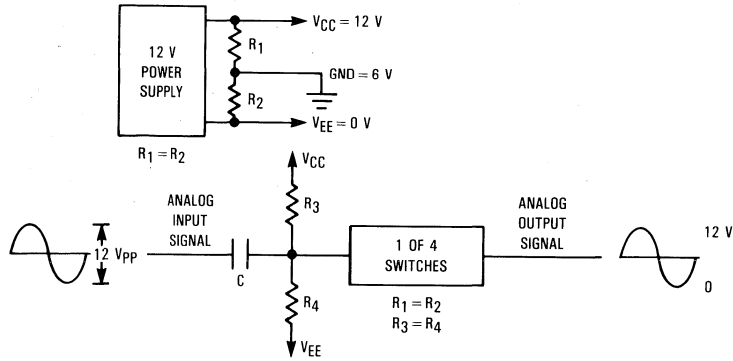


Figure 19. Switching a 0-to-12 V Signal Using a Single Power Supply ( $GND \neq 0V$ )

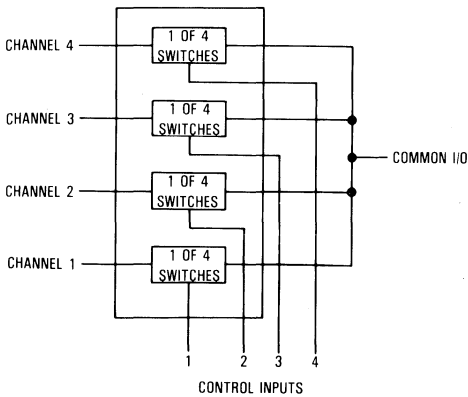


Figure 20. 4-Input Multiplexer

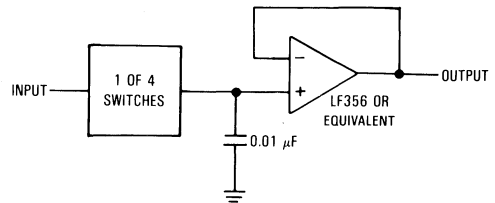


Figure 21. Sample/Hold Amplifier

5

# Analog Multiplexers/ Demultiplexers with Address Latch

## High-Performance Silicon-Gate CMOS

The MC54/74HC4351, and MC54/74HC4353 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from  $V_{CC}$  to  $V_{EE}$ ).

The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. The data at the Channel-Select inputs may be latched by using the active-low Latch Enable pin. When Latch Enable is high, the latch is transparent. When either Enable 1 (active low) or Enable 2 (active high) is inactive, all analog switches are turned off.

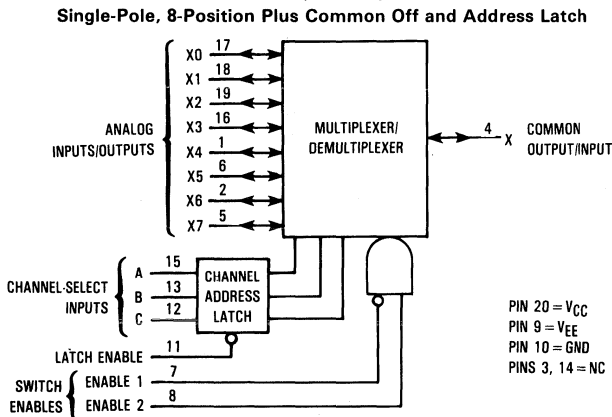
The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance ( $R_{ON}$ ) is more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

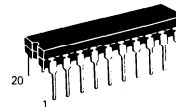
For multiplexers/demultiplexers without latches, see the HC4051, HC4052, and HC4053.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ( $V_{CC} - V_{EE}$ ) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal-Gate Types
- Low Noise
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: HC4351 — 222 FETs or 55.5 Equivalent Gates  
 HC4353 — 186 FETs or 46.5 Equivalent Gates

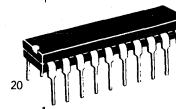
### LOGIC DIAGRAM MC54/74HC4351



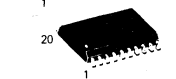
## MC54/74HC4351 MC54/74HC4353



J SUFFIX  
 CERAMIC  
 CASE 732-03



N SUFFIX  
 PLASTIC  
 CASE 738-03



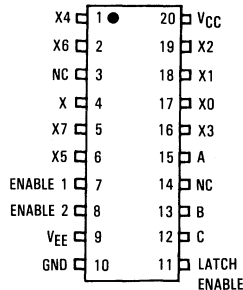
DW SUFFIX  
 SOIC  
 CASE 751D-03

### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

$T_A$  =  $-55^\circ$  to  $125^\circ\text{C}$  for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT MC54/74HC4351



### FUNCTION TABLE MC54/74HC4351

Control Inputs			ON Channel (LE = H)*		
Enable	Select				
1	2	C	B	A	
L	H	L	L	L	X0
L	H	L	L	H	X1
L	H	L	H	L	X2
L	H	L	H	H	X3
L	H	H	L	L	X4
L	H	H	L	H	X5
L	H	H	H	L	X6
L	H	H	H	H	X7
H	X	X	X	X	None
X	X	X	X	X	None

X = don't care

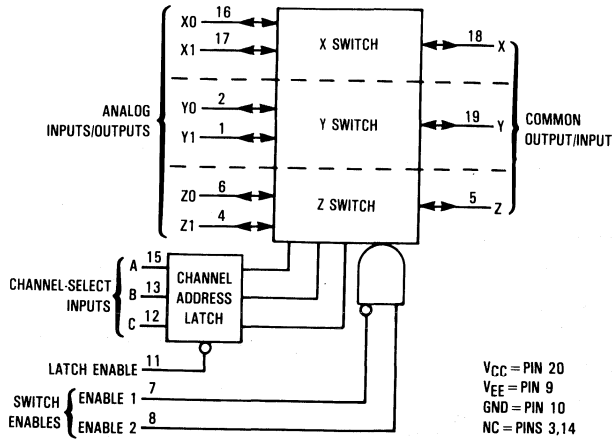
\*When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

# MC54/74HC4351 • MC54/74HC4353

## MC54/74HC4353

Triple Single-Pole, Double-Position Plus Common Off and Address Latch

### BLOCK DIAGRAM

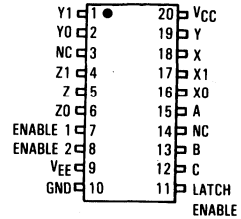


V<sub>CC</sub> = PIN 20  
V<sub>EE</sub> = PIN 9  
GND = PIN 10  
NC = PINS 3,14

#### NOTE:

This device allows independent control of each switch. Channel-Select Input A controls the X Switch, Input B controls the Y Switch, and Input C controls the Z Switch.

### PIN ASSIGNMENT



NC = NO CONNECTION

### FUNCTION TABLE

Control Inputs		Select			ON Channel (LE = H)*		
Enable		1	2	C	B	A	
L	H	L	L	L	Z0	Y0	X0
L	H	L	L	H	Z0	Y0	X1
L	H	L	H	L	Z0	Y1	X0
L	H	L	H	H	Z0	Y1	X1
L	H	H	L	L	Z1	Y0	X0
L	H	H	L	H	Z1	Y0	X1
L	H	H	H	L	Z1	Y1	X0
L	H	H	H	H	Z1	Y1	X1
H	X	X	X	X			None
X	L	X	X	X			None

X = Don't Care

\*When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

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## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Ref. to GND) (Ref. to V <sub>EE</sub> )	-0.5 to +7.0 -0.5 to 14.0	V
V <sub>EE</sub>	Negative DC Supply Voltage (Ref. to GND)	-7.0 to +0.5	V
V <sub>IS</sub>	Analog Input Voltage	V <sub>EE</sub> - 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>in</sub>	Digital Input Voltage (Ref. to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
I	DC Current Into or Out of Any Pin	±25	mA
P <sub>D</sub>	Power Dissipation in Still Air Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the ranges indicated in the Recommended Operating Conditions.

Unused digital input pins must be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused Analog I/O pins may be left open or terminated. See Applications Information.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	Positive DC Supply Voltage (Ref. to GND) (Ref. to V <sub>EE</sub> )	2.0 2.0	6.0 12.0	V	
V <sub>EE</sub>	Negative DC Supply Voltage (Ref. to GND)	-6.0	GND	V	
V <sub>IS</sub>	Analog Input Voltage	V <sub>EE</sub>	V <sub>CC</sub>	V	
V <sub>in</sub>	Digital Input Voltage (Ref. to GND)	GND	V <sub>CC</sub>	V	
V <sub>IO</sub> *	Static or Dynamic Voltage Across Switch	-	1.2	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time, Channel Select or Enable Inputs (Figure 9a)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

\*For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V<sub>EE</sub> = GND, Except Where Noted

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R <sub>on</sub> = Per Spec	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	R <sub>on</sub> = Per Spec	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
I <sub>in</sub>	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V <sub>in</sub> = V <sub>CC</sub> or GND, V <sub>EE</sub> = -6.0 V	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	Channel Select = V <sub>CC</sub> or GND Enables = V <sub>CC</sub> or GND V <sub>IS</sub> = V <sub>CC</sub> or GND V <sub>IO</sub> = 0 V  V <sub>EE</sub> = GND V <sub>EE</sub> = -6.0	6.0	2	20	40	μA
			6.0	8	80	160	
			6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.

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# MC54/74HC4351 • MC54/74HC4353

## DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	V <sub>EE</sub> V	Guaranteed Limit			Unit	
					25°C to -55°C	≤ 85°C	≤ 125°C		
R <sub>on</sub>	Maximum "ON" Resistance	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to V <sub>EE</sub> I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	4.5	0.0	190	240	280	Ω	
			4.5	-4.5	120	150	170		
			6.0	-6.0	100	125	140		
		V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or V <sub>EE</sub> (Endpoints) I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	4.5	0.0	150	190	230		
			4.5	-4.5	100	125	140		
			6.0	-6.0	80	100	115		
ΔR <sub>on</sub>	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - V <sub>EE</sub> ) I <sub>S</sub> ≤ 2.0 mA	4.5	0.0	30	35	40	Ω	
			4.5	-4.5	12	15	18		
			6.0	-6.0	10	12	14		
I <sub>off</sub>	Maximum Off-Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IO</sub> = V <sub>CC</sub> - V <sub>EE</sub> Switch Off (Figure 3)	6.0	-6.0	0.1	0.5	1.0	μA	
			Maximum Off-Channel Leakage Current, Common Channel		V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IO</sub> = V <sub>CC</sub> - V <sub>EE</sub> Switch Off (Figure 4)				
	HC4351	6.0	-6.0	0.2	2.0	4.0			
	HC4352	6.0	-6.0	0.1	1.0	2.0			
	HC4353	6.0	-6.0	0.1	1.0	2.0			
I <sub>on</sub>	Maximum On-Channel Leakage Current, Channel to Channel	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> Switch to Switch = V <sub>CC</sub> - V <sub>EE</sub> (Figure 5)	6.0	-6.0	0.2	2.0	4.0	μA	
			HC4351	6.0	-6.0	0.1	1.0		2.0
			HC4352	6.0	-6.0	0.1	1.0		2.0
			HC4353	6.0	-6.0	0.1	1.0		2.0

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit	
			25°C to -55°C	≤ 85°C	≤ 125°C		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Channel-Select to Analog Output (Figure 9)	2.0	370	465	550	ns	
		4.5	74	93	110		
		6.0	63	79	94		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0	60	75	90	ns	
		4.5	12	15	18		
		6.0	10	13	15		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Analog Output (Figure 12)	2.0	325	410	485	ns	
		4.5	65	82	97		
		6.0	55	70	82		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)	2.0	290	365	435	ns	
		4.5	58	73	87		
		6.0	49	62	74		
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)	2.0	345	435	515	ns	
		4.5	69	87	103		
		6.0	59	74	87		
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF	
C <sub>I/O</sub>	Maximum Capacitance Analog I/O Common O/I: HC4351 HC4352 HC4353 Feedthrough	Enable 1 = V <sub>IH</sub> , Enable 2 = V <sub>IL</sub>	—	35	35	35	pF
			—	130	130	130	
			—	80	80	80	
			—	50	50	50	
			—	1.0	1.0	1.0	

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) (Figure 14) Used to determine the no-load dynamic power consumption: P <sub>D</sub> = C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f + I <sub>CC</sub> V <sub>CC</sub> For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF
		45 (HC4351)	80 (HC4352)	45 (HC4353)	

# MC54/74HC4351•MC54/74HC4353

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Channel-Select to Latch Enable (Figure 12)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Channel Select (Figure 12)	2.0	0	0	0	ns
		4.5	0	0	0	
		6.0	0	0	0	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable (Figure 12)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times, Channel-Select, Latch Enable, and Enables 1 and 2	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

## ADDITIONAL APPLICATION CHARACTERISTICS (GND=0.0 V)

Symbol	Parameter	Test Condition	V <sub>CC</sub> V	V <sub>EE</sub> V	Limit*			Unit
					25°C 54/74HC			
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6)	f <sub>in</sub> = 1 MHz Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub> Increase f <sub>in</sub> Frequency Until dB Meter Reads -3 dB R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	2.25	-2.25	80	95	120	MHz
			4.50	-4.50	80	95	120	
			6.00	-6.00	80	95	120	
-	Off-Channel Feedthrough Isolation (Figure 7)	f <sub>in</sub> ≡ Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF  f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	2.25	-2.25	-50			dB
			4.50	-4.50	-50			
			6.00	-6.00	-50			
-	Feedthrough Noise, Channel Select Input to Common O/I (Figure 8)	V <sub>in</sub> ≡ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns) Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A Enable = GND  R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF  R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF	2.25	-2.25	25			mVpp
			4.50	-4.50	105			
			6.00	-6.00	135			
-	Crosstalk Between Any Two Switches (Figure 13) (Test does not apply to HC4351)	f <sub>in</sub> ≡ Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF  f <sub>in</sub> = 1 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	2.25	-2.25	-50			dB
			4.50	-4.50	-50			
			6.00	-6.00	-50			
THD	Total Harmonic Distortion (Figure 15)	f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF THD = THD <sub>Measured</sub> - THD <sub>Source</sub> V <sub>IS</sub> = 4.0 V <sub>pp</sub> sine wave V <sub>IS</sub> = 8.0 V <sub>pp</sub> sine wave V <sub>IS</sub> = 11.0 V <sub>pp</sub> sine wave	2.25	-2.25	0.10			%
			4.50	-4.50	0.08			
			6.00	-6.00	0.05			

\*Limits not tested. Determined by design and verified by qualification.

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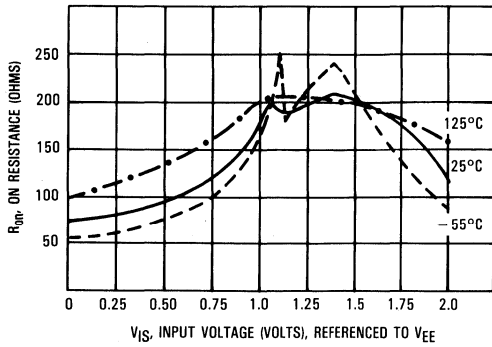


Figure 1a. Typical On Resistance,  $V_{CC} - V_{EE} = 2.0 \text{ V}$

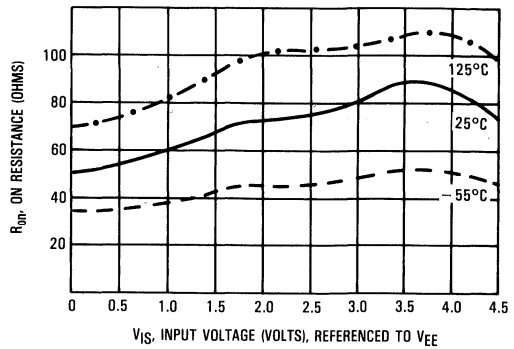


Figure 1b. Typical On Resistance,  $V_{CC} - V_{EE} = 4.5 \text{ V}$

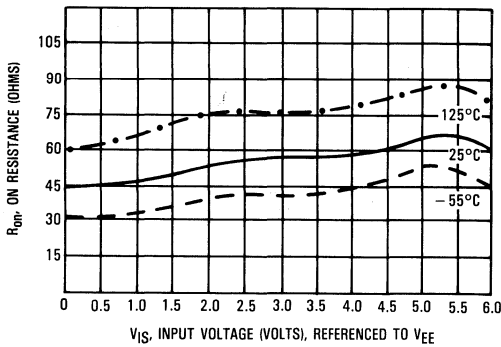


Figure 1c. Typical On Resistance,  $V_{CC} - V_{EE} = 6.0 \text{ V}$

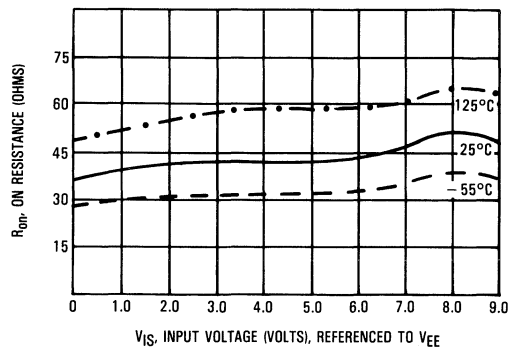


Figure 1d. Typical On Resistance,  $V_{CC} - V_{EE} = 9.0 \text{ V}$

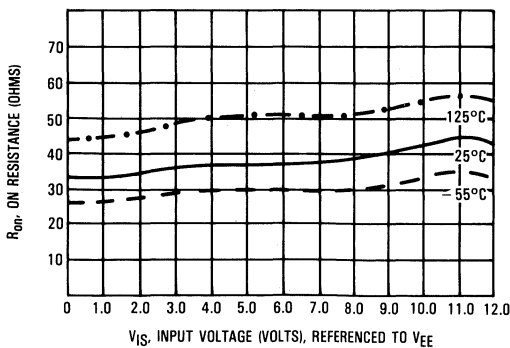


Figure 1e. Typical On Resistance,  $V_{CC} - V_{EE} = 12.0 \text{ V}$

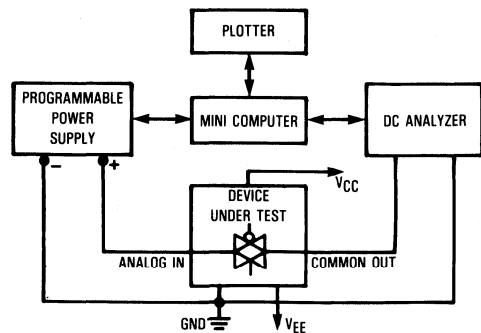


Figure 2. On Resistance Test Set-Up

5



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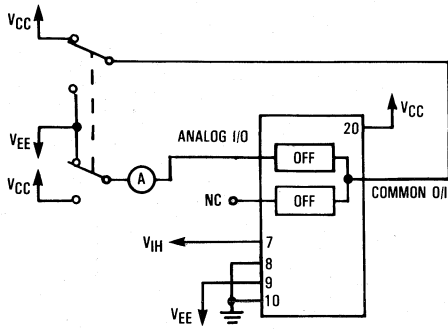


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

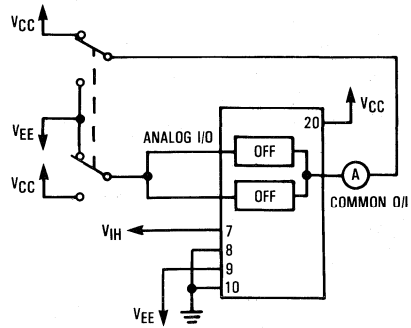


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

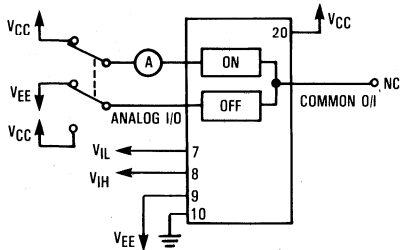
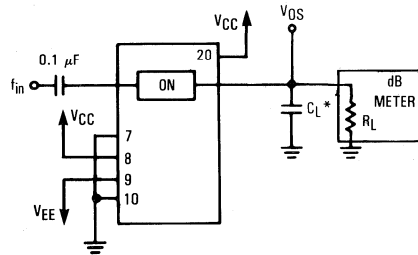
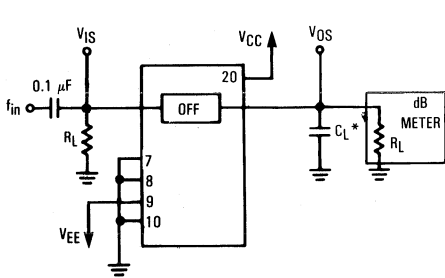


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



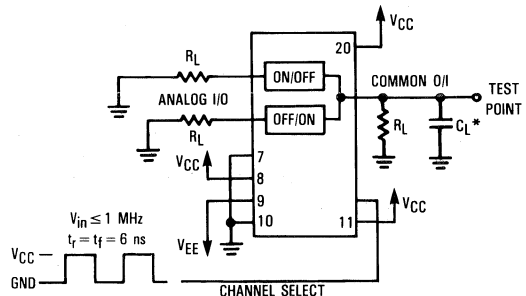
\* Includes all probe and jig capacitance.

Figure 6. Maximum On-Channel Bandwidth Test Set-Up



\* Includes all probe and jig capacitance.

Figure 7. Off-Channel Feedthrough Isolation, Test Set-Up



\* Includes all probe and jig capacitance.

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

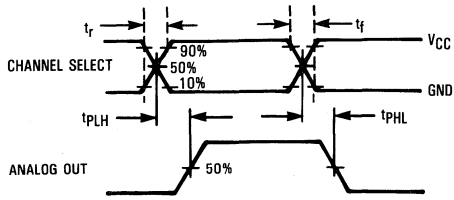
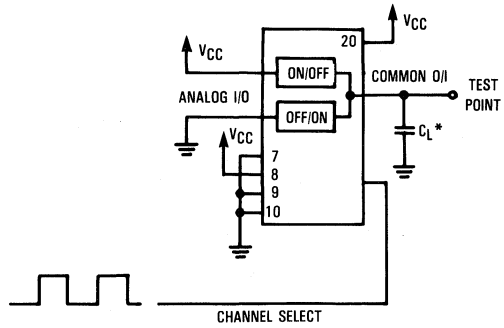


Figure 9a. Propagation Delays, Channel Select to Analog Out



\*Includes all probe and jig capacitance.

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

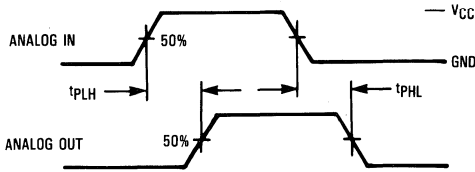
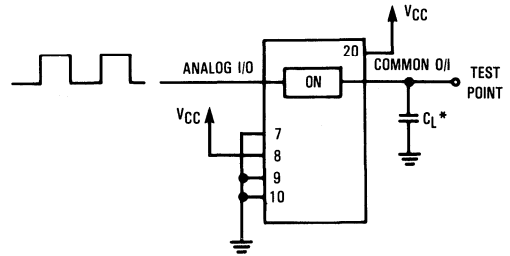


Figure 10a. Propagation Delays, Analog In to Analog Out



\*Includes all probe and jig capacitance.

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

5

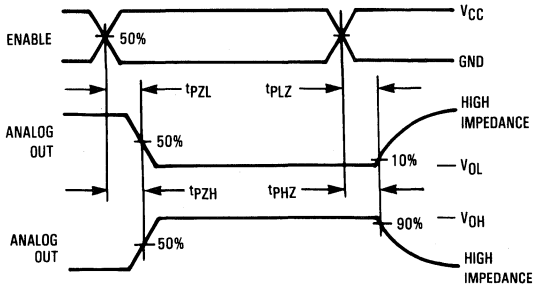
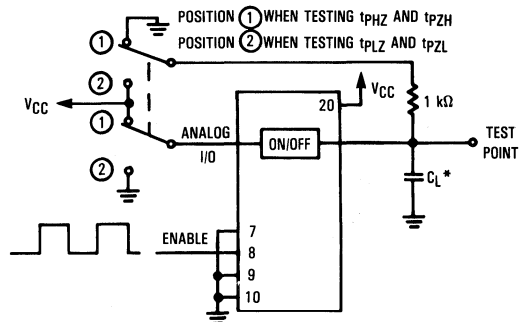


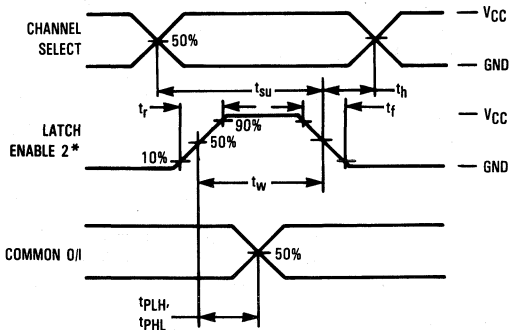
Figure 11a. Propagation Delay, Enable 1 or 2 to Analog Out



\*Includes all probe and jig capacitance.

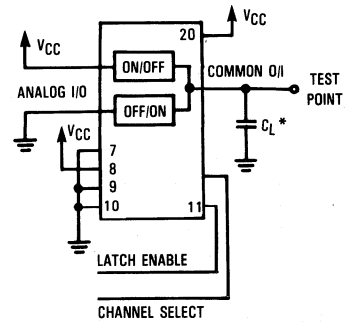
Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out

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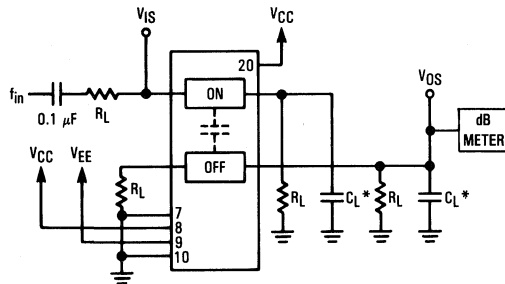
\*Latch Enable 1 is a similar waveform except the Latch Enable waveform is inverted.

**Figure 12a. Propagation Delay, Latch Enable to Analog Out**



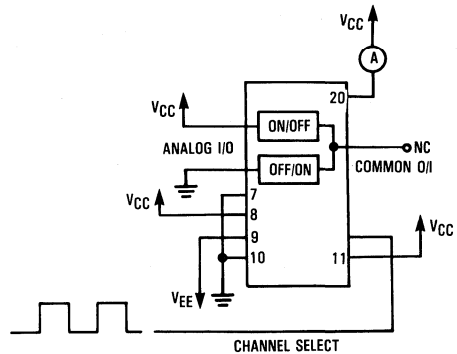
\*Includes all probe and jig capacitance.

**Figure 12b. Propagation Delay, Test Set-Up Latch Enable to Analog Out**

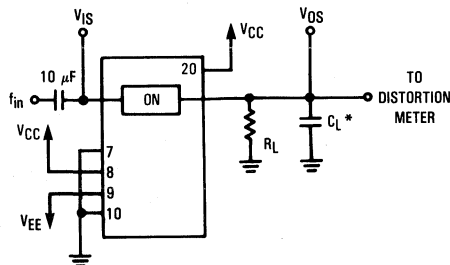


\*Includes all probe and jig capacitance.

**Figure 13. Crosstalk Between Any Two Switches, Test Set-Up**

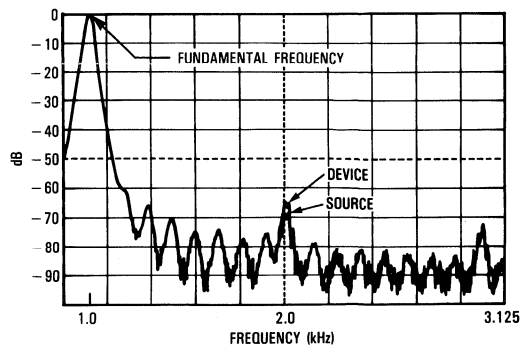


**Figure 14. Power Dissipation Capacitance, Test Set-Up**



\*Includes all probe and jig capacitance.

**Figure 15a. Total Harmonic Distortion, Test Set-Up**



**Figure 15b. Plot, Harmonic Distortion**

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at  $V_{CC}$  or GND logic levels.  $V_{CC}$  being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5\text{ V} = \text{logic high}$$

$$GND = 0\text{ V} = \text{logic low}$$

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and  $V_{EE}$ . The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below  $V_{EE}$ . In this example, the difference between  $V_{CC}$  and  $V_{EE}$  is ten volts. Therefore, using the configuration in Figure 16, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog in-

puts/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{CC} - GND = 2\text{ to }6\text{ volts}$$

$$V_{EE} - GND = 0\text{ to }-6\text{ volts}$$

$$V_{CC} - V_{EE} = 2\text{ to }12\text{ volts}$$

$$\text{and } V_{EE} \leq GND$$

When voltage transients above  $V_{CC}$  and/or below  $V_{EE}$  are anticipated on the analog channels, external Germanium or Schottky diodes ( $D_x$ ) are recommended as shown in Figure 17. These diodes should be able to absorb the maximum anticipated current surges during clipping.

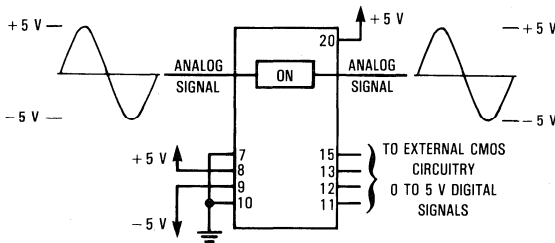


Figure 16. Application Example

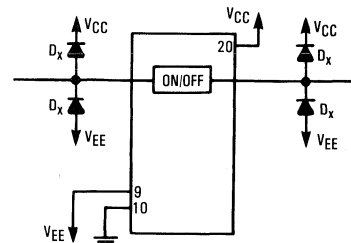
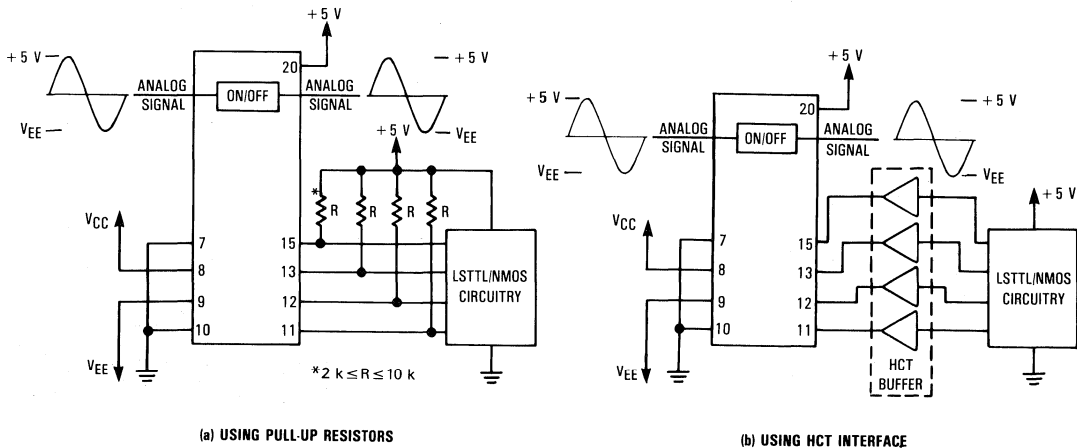


Figure 17. External Germanium or Schottky Clipping Diodes

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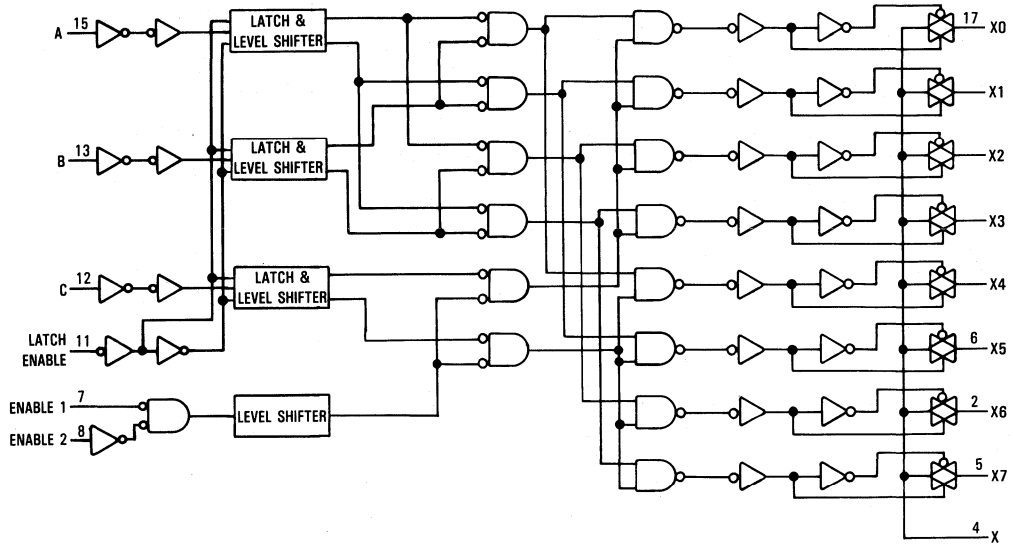
(a) USING PULL-UP RESISTORS

(b) USING HCT INTERFACE

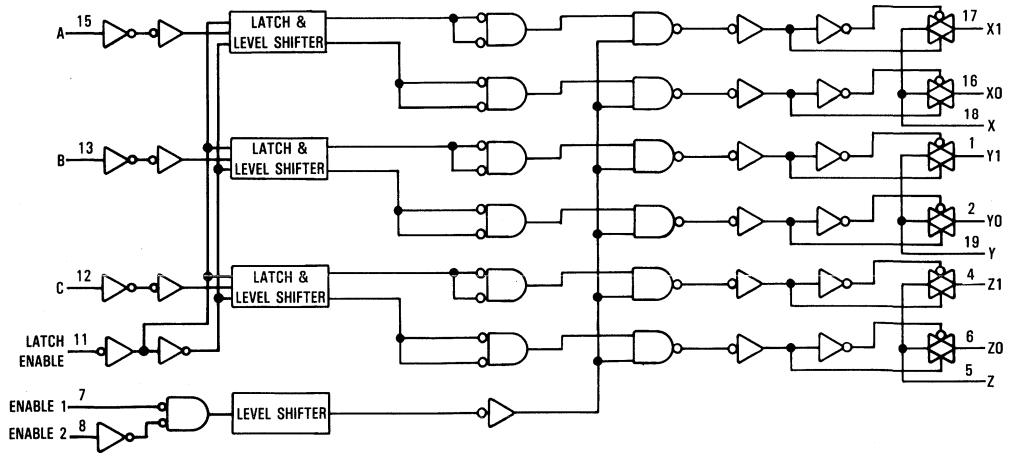
Figure 18. Interfacing LSTTL/NMOS to CMOS Inputs

# MC54/74HC4351•MC54/74HC4353

## FUNCTION DIAGRAM HC4351



## FUNCTION DIAGRAM HC4353



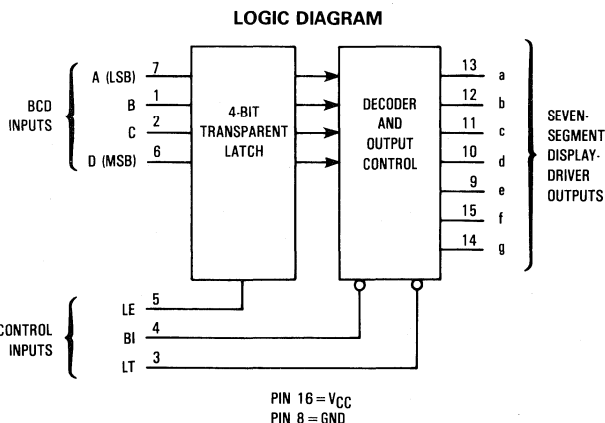
# BCD-to-Seven-Segment Latch/ Decoder/Display Driver

## High-Performance Silicon-Gate CMOS

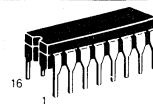
The MC54/74HC4511 is identical in pinout to the MC14511 metal-gate CMOS decoder/driver. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4511 provides the functions of a 4-bit storage latch, a BCD-to-seven-segment decoder, and a display driver. It can be used either directly or indirectly with seven-segment light-emitting diode (LED), incandescent, fluorescent, gas discharge, or liquid-crystal readouts. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn off or pulse modulate the brightness of the display, and to store a BCD code, respectively.

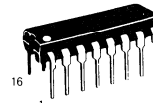
- Latch Storage of BCD Inputs
- Blanking Input
- Lamp Test Input
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates



## MC54/74HC4511



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



**N SUFFIX  
 PLASTIC  
 CASE 648-08**



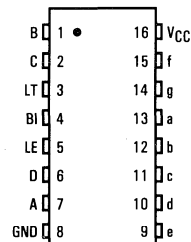
**D SUFFIX  
 SOIC  
 CASE 751B-04**

### ORDERING INFORMATION

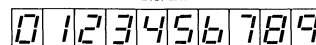
MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



DISPLAY



# MC54/74HC4511

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±70	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 3)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	6.0	5.9	5.9	5.9	
			4.5	3.98	3.84	3.70	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC4511

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 6)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	129	153	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Output (Figures 2 and 6)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	129	153	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Blanking Input to Output (Figures 3 and 6)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	129	153	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Lamp Test to Output (Figures 4 and 6)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	129	153	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 3 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		70	

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Input A, B, C, or D to Latch Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input A, B, C, or D (Figure 5)	2.0	0	0	0	ns
		4.5	0	0	0	
		6.0	0	0	0	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 3)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.



# MC54/74HC4511

## SWITCHING WAVEFORMS

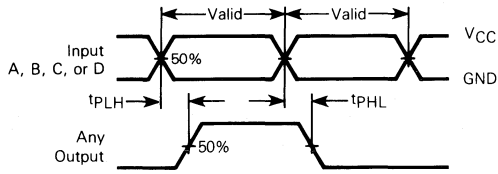


Figure 1.

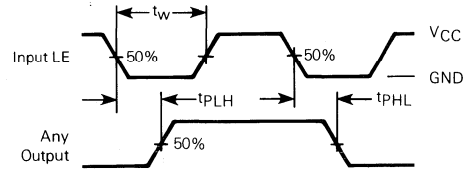


Figure 2.

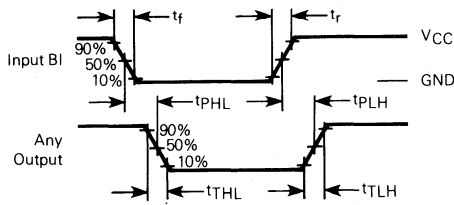


Figure 3.

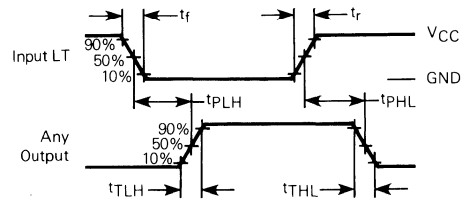


Figure 4.

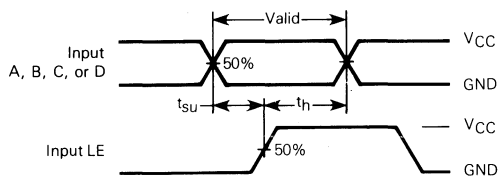
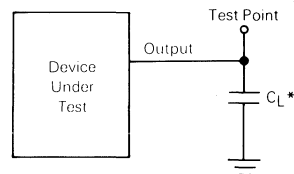


Figure 5.



\* Includes all probe and jig capacitance.

Figure 6. Test Circuit

# MC54/74HC4511

## FUNCTION TABLE

Inputs				Outputs							
LE	BI	LT	D C B A	a	b	c	d	e	f	g	Display
X	X	L	X X X X	H	H	H	H	H	H	H	8
X	L	H	X X X X	L	L	L	L	L	L	L	Blank
L	H	H	L L L L	H	H	H	H	H	H	L	0
L	H	H	L L L H	L	H	H	L	L	L	L	1
L	H	H	L L H L	H	H	L	H	H	L	H	2
L	H	H	L L H H	H	H	H	L	L	L	H	3
L	H	H	L H L L	L	H	H	L	L	H	H	4
L	H	H	L H L H	H	L	H	H	L	H	H	5
L	H	H	L H H L	L	L	H	H	H	H	H	6
L	H	H	L H H H	H	H	H	L	L	L	L	7
L	H	H	H L L L	H	H	H	H	H	H	H	8
L	H	H	H L L H	H	H	H	L	L	H	H	9
L	H	H	H L H L	L	L	L	L	L	L	L	Blank
L	H	H	H L H H	L	L	L	L	L	L	L	Blank
L	H	H	H H L L	L	L	L	L	L	L	L	Blank
L	H	H	H H L H	L	L	L	L	L	L	L	Blank
L	H	H	H H H L	L	L	L	L	L	L	L	Blank
L	H	H	H H H H	L	L	L	L	L	L	L	Blank
H	H	H	X X X X	*	*	*	*	*	*	*	*

\* = Depends upon the BCD code previously applied while LE was at a low level.

## PIN DESCRIPTIONS

### INPUTS

**A, B, C, D (PINS 7, 1, 2, 6)** — BCD inputs. A (pin 7) is the least significant bit and D (pin 6) is the most significant bit. Hexadecimal code A-F at these inputs causes the outputs to assume a low level, offering an alternate method of blanking the display.

### OUTPUTS

**a, b, c, d, e, f, g (PINS 13, 12, 11, 10, 9, 15, 14)** — Decoded, buffered seven-segment display-driver outputs. These outputs, unlike the MC14511, have CMOS drivers, which produce typical CMOS output voltage levels. These outputs are connected to various displays as shown in Figure 7.

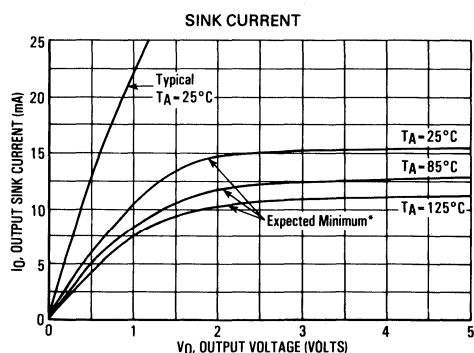
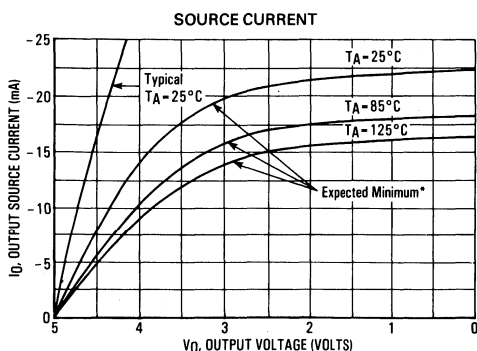
### CONTROL INPUTS

**BI (PIN 4)** — Active-low display blanking input. A low level on this input will cause all outputs to be held low, thereby blanking the display. LT is the only input that overrides the BI input.

**LT (PIN 3)** — Active-low lamp test. A low level on this input causes all outputs to assume a high level. This input allows the user to test all segments of a display with a single control input. This input is independent of all other inputs.

**LE (PIN 5)** — Latch enable input. This input controls the 4-bit transparent latch. A high level on this input latches the code present at the A, B, C and D inputs; a low level allows the code to be transmitted through the latch to the decoder.

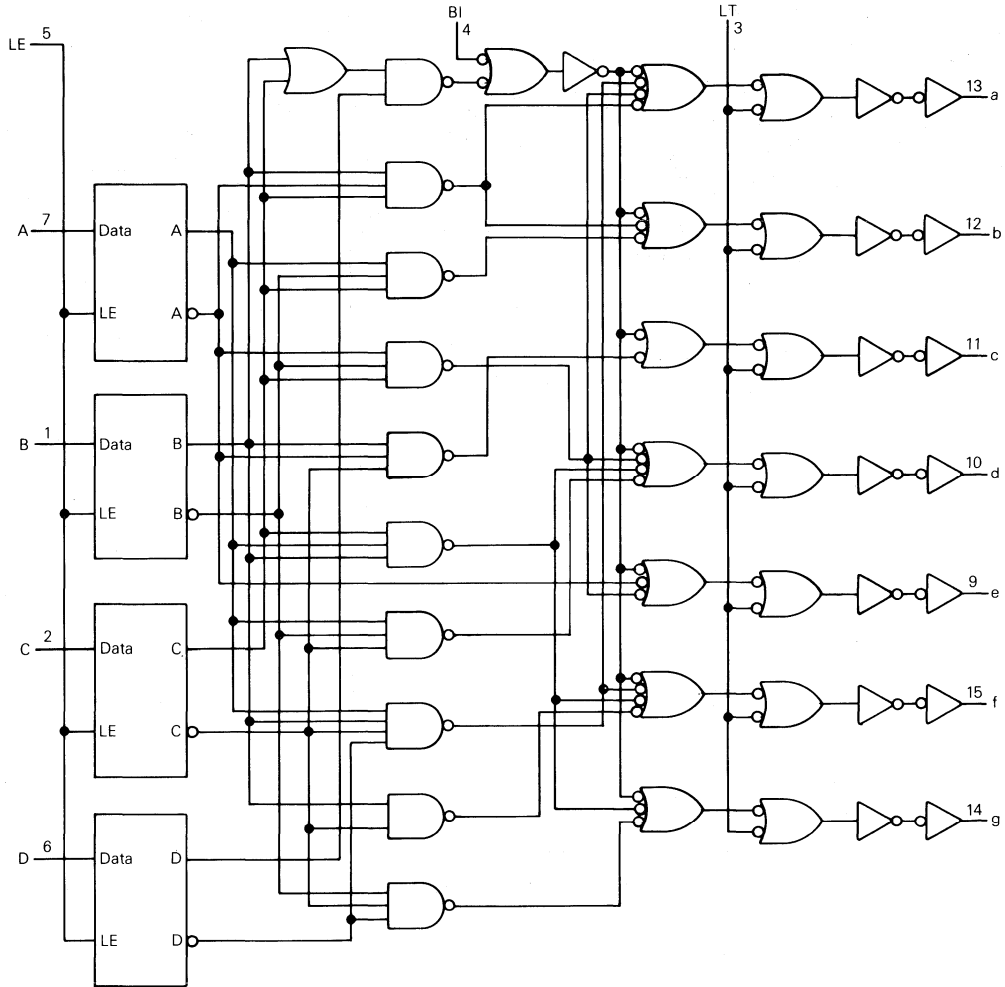
## OUTPUT CHARACTERISTIC CURVES ( $V_{CC} = 5\text{ V}$ )



\* The expected minimum curves are not guarantees, but are design aids.

# MC54/74HC4511

## EXPANDED LOGIC DIAGRAM



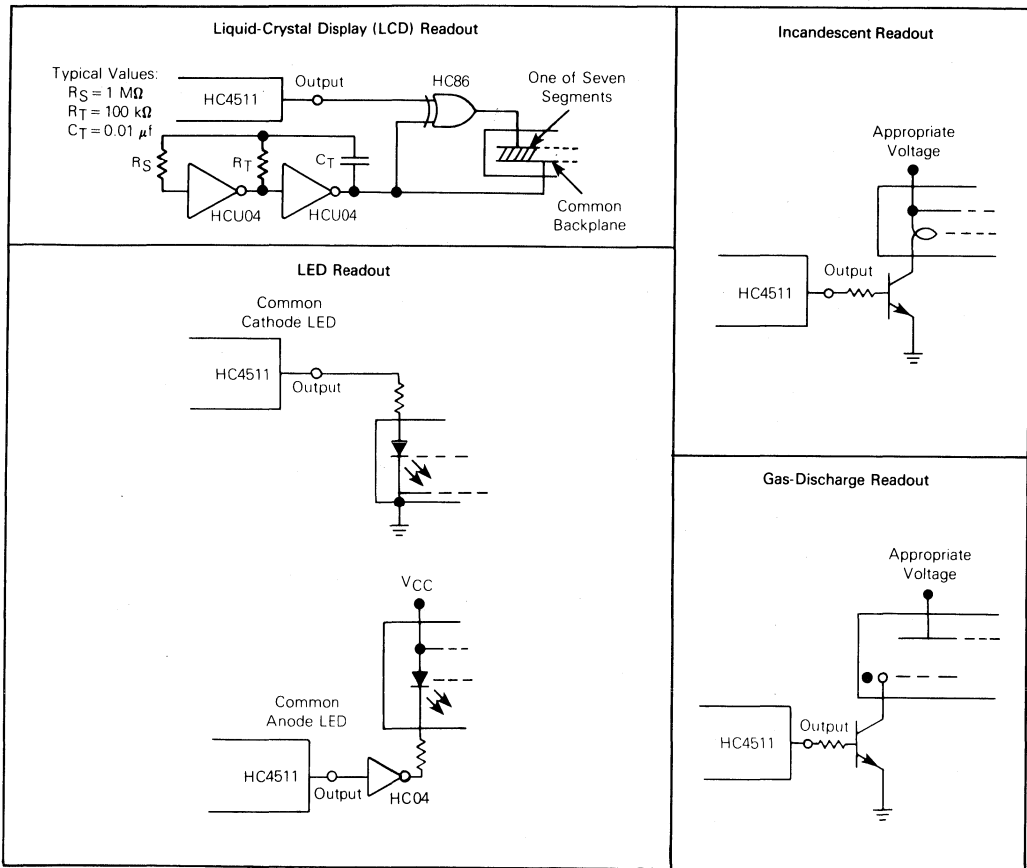


Figure 7. Connections to Various Display Readouts

# 1-of-16 Decoder/Demultiplexer with Address Latch

## High-Performance Silicon-Gate CMOS

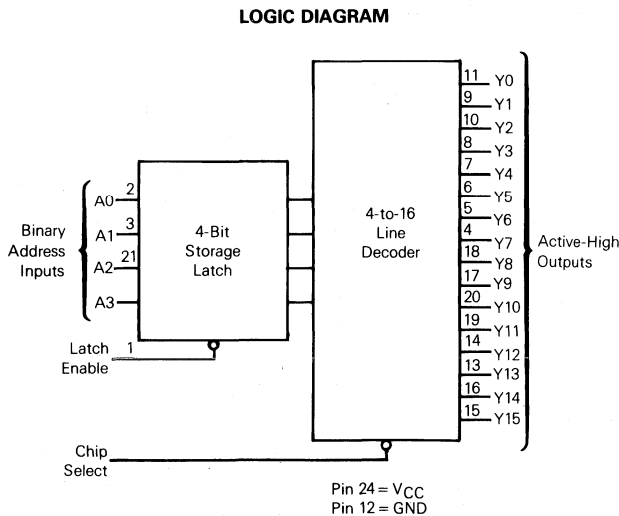
The MC54/74HC4514 is identical in pinout to the MC14514B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of a 4-bit storage latch with a Latch Enable and Chip Select input. When a low signal is applied to the Latch Enable input, the Address is stored, and decoded. When the Chip Select input is high, all sixteen outputs are forced to a low level.

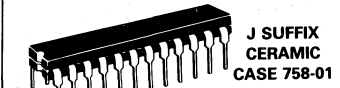
The Chip Select input is provided to facilitate the chip-select, demultiplexing, and cascading functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using the Chip Select as a data input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 268 FETs or 67 Equivalent Gates



## MC54/74HC4514

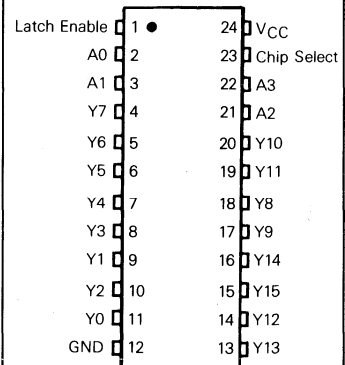


### ORDERING INFORMATION

MC74HCXXXDW	SOIC
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



# MC54/74HC4514

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

# MC54/74HC4514

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Chip Select to Output Y (Figures 1 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 5)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t <sub>PHL</sub>		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PLH</sub>	Maximum Propagation Delay, Latch Enable to Output Y (Figures 3 and 5)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t <sub>PHL</sub>		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		70	

## TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Input A to Latch Enable (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input A (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC4514

## SWITCHING WAVEFORMS

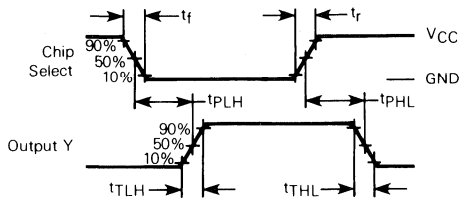


Figure 1.

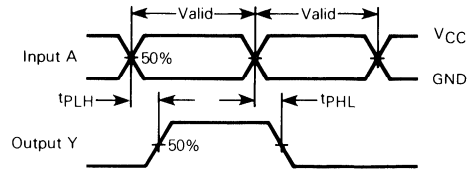


Figure 2.

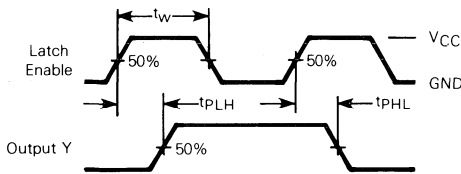


Figure 3.

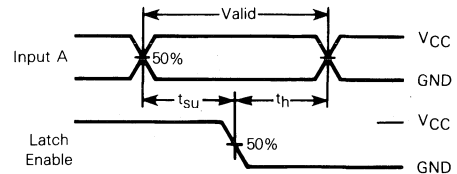
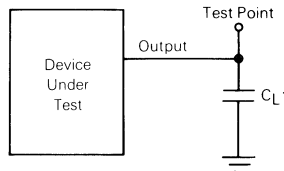


Figure 4.



\*Includes all probe and jig capacitance.

Figure 5. Test Circuit

5



# MC54/74HC4514

## FUNCTION TABLE

Latch Enable	Chip Select	Address Inputs				Selected Output (High)
		A3	A2	A1	A0	
H	L	L	L	L	L	Y0
H	L	L	L	L	H	Y1
H	L	L	L	H	L	Y2
H	L	L	L	H	H	Y3
H	L	L	H	L	L	Y4
H	L	L	H	L	H	Y5
H	L	L	H	H	L	Y6
H	L	L	H	H	H	Y7
H	L	H	L	L	L	Y8
H	L	H	L	L	H	Y9
H	L	H	L	H	L	Y10
H	L	H	L	H	H	Y11
H	L	H	H	L	L	Y12
H	L	H	H	L	H	Y13
H	L	H	H	H	L	Y14
H	L	H	H	H	H	Y15
X	H	X	X	X	X	All Outputs = L
L	L	X	X	X	X	Latched Data

## PIN DESCRIPTIONS

### ADDRESS INPUTS

**A0, A1, A2, A3 (PINS 2, 3, 21, 22)** — Address Inputs. These inputs are decoded to produce a high level on one of 16 outputs. The inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. The decimal equivalent of the binary input address indicates which of the 16 data outputs, Y0-Y15, is selected.

### OUTPUTS

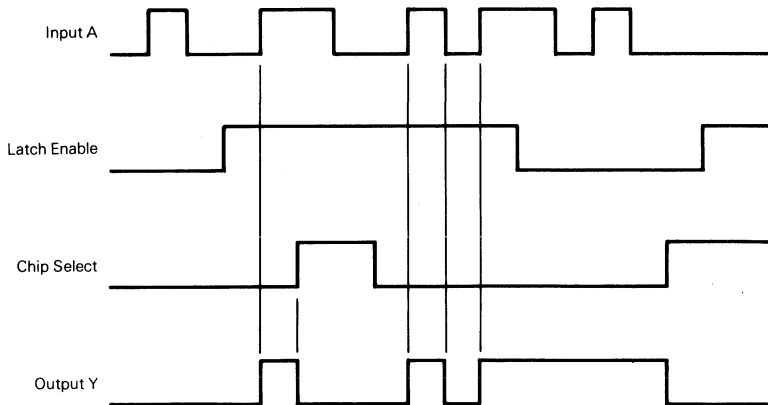
**Y0-Y15 (PINS 11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15)** — Active-High Outputs. These outputs produce a high level when selected (Latch Enable = H, Chip Select = L) and are at a low level when not selected.

### CONTROL INPUTS

**LATCH ENABLE (PIN 1)** — Latch Enable Input. A low level on this input stores the data on the Address data inputs in the 4-bit latch. A high level on the Latch Enable input makes the latch transparent and allows the outputs to follow the inputs. Note that the data is latched only while the Latch Enable input is at a low level.

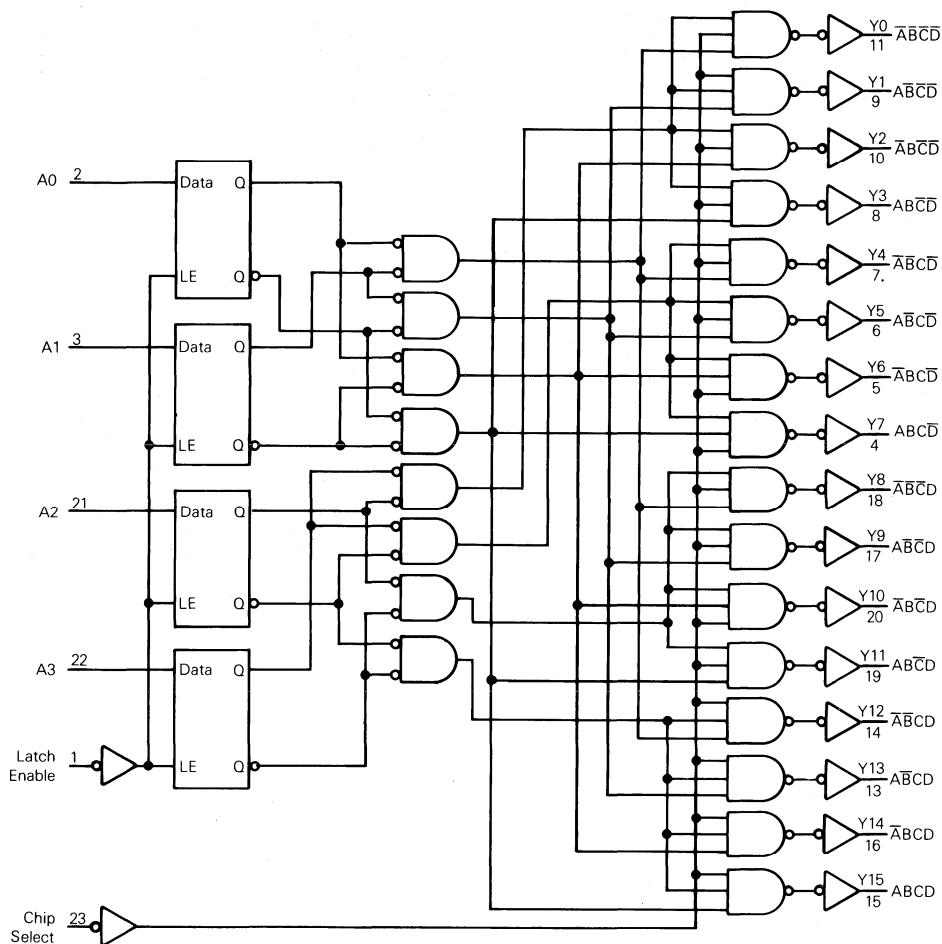
**CHIP SELECT (PIN 23)** — Chip Select Input. A high on this input produces a low level on all outputs, regardless of what appears at the address or Latch Enable inputs. A low level on the Chip Select input allows the selected output to produce a high level.

## TIMING DIAGRAM



# MC54/74HC4514

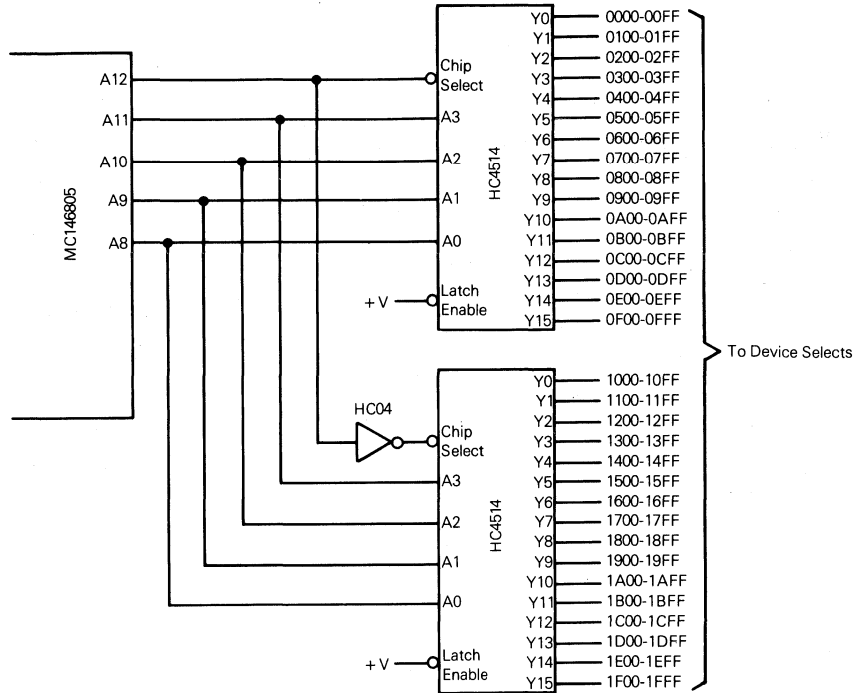
## EXPANDED LOGIC DIAGRAM



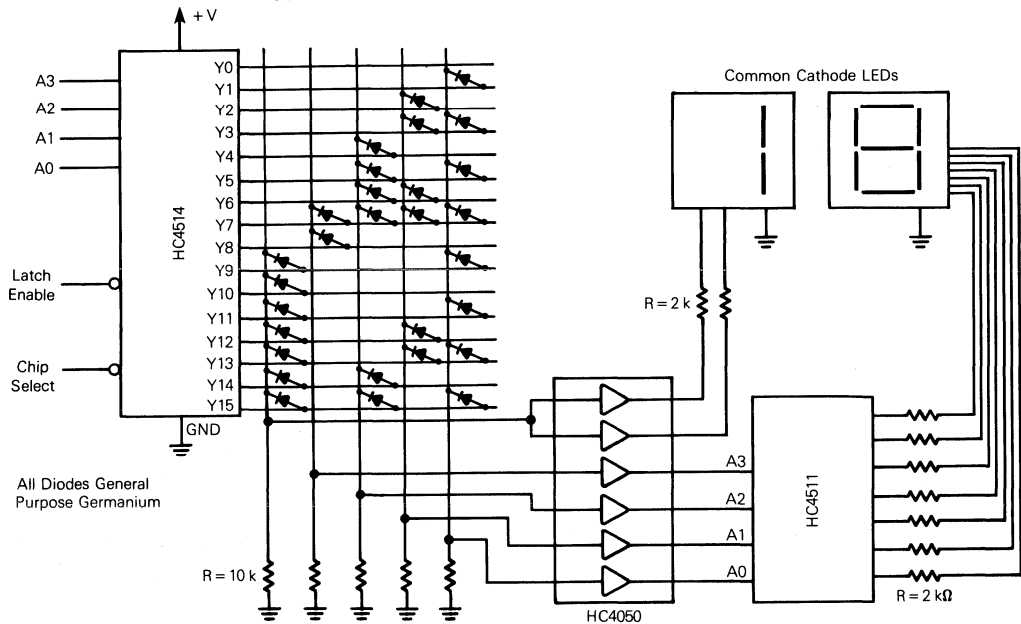
5

# MC54/74HC4514

## MICROPROCESSOR MEMORY DECODING



## CODE TO CODE CONVERSION — HEXADECIMAL TO BCD

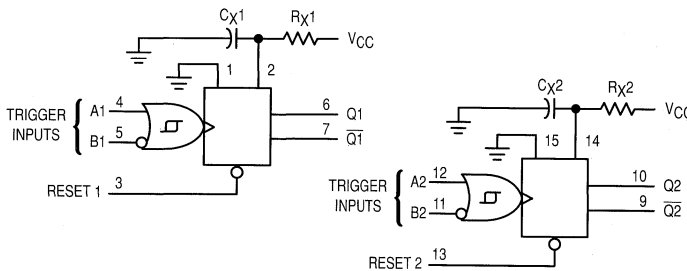


## Dual Precision Monostable Multivibrator (Retriggerable, Resettable)

The MC54/74HC4538A is identical in pinout to the MC14538B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

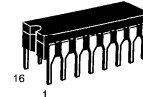
This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and produces a precision output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger-input rise and fall time restrictions. The output pulse width is determined by the external timing components,  $R_X$  and  $C_X$ . The device has a reset function which forces the Q output low and the  $\bar{Q}$  output high, regardless of the state of the output pulse circuitry.

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse is Independent of the Trigger Pulse Width
- $\pm 10\%$  Guaranteed Pulse Width Variation from Part to Part (Using the Same Test Jig)
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range 3.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 145 FETs or 36 Equivalent Gates

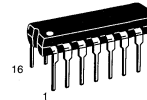


PIN 16 =  $V_{CC}$   
 PIN 8 = GND  
 $R_X$  AND  $C_X$  ARE EXTERNAL COMPONENTS  
 PIN 1 AND PIN 15 MUST BE HARD WIRED TO GND

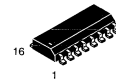
### MC54/74HC4538A



**J SUFFIX**  
**CERAMIC**  
**CASE 620-09**



**N SUFFIX**  
**PLASTIC**  
**CASE 648-08**



**D SUFFIX**  
**SOIC**  
**CASE 751B-04**

#### ORDERING INFORMATION

MC74HCXXXXAN Plastic  
 MC54HCXXXXAJ Ceramic  
 MC74HCXXXXAD SOIC

#### PIN ASSIGNMENT

GND	1	16	$V_{CC}$
$C_X1/R_X1$	2	15	GND
RESET 1	3	14	$C_X2/R_X2$
A1	4	13	RESET 2
B1	5	12	A2
Q1	6	11	B2
$\bar{Q}1$	7	10	Q2
GND	8	9	$\bar{Q}2$

#### FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\bar{Q}$
H	H	H		
H	L	L		
H	X	L	Not Triggered	Not Triggered
H	H	X	Not Triggered	Not Triggered
H	L,H	H	Not Triggered	Not Triggered
H	L	L,H	Not Triggered	Not Triggered
L	X	X	L	H
	X	X	Not Triggered	Not Triggered

# MC54/74HC4538A

MAXIMUM RATINGS*			
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	
I <sub>in</sub>	DC Input Current, per Pin A, B, Reset C <sub>x</sub> , R <sub>x</sub>	±20 ±30	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high-impedance circuits. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0**	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time — Reset (Figure 7)	V <sub>CC</sub> = 2.0 V	0	1000	ns
		V <sub>CC</sub> = 4.5 V	0	500	
	A or B (Figure 5)	—	No Limit		
R <sub>x</sub>	External Timing Resistor	V <sub>CC</sub> < 4.5 V	10	*	kΩ
		V <sub>CC</sub> ≥ 4.5 V	2.0	*	
C <sub>x</sub>	External Timing Capacitor	0	*	μF	

\* The maximum allowable values of R<sub>x</sub> and C<sub>x</sub> are a function of the leakage of capacitor C<sub>x</sub>, the leakage of the HC4538A, and leakage due to board layout and surface resistance. For most applications, C<sub>x</sub>/R<sub>x</sub> should be limited to a maximum value of 10 μF/1.0 MΩ. Values of C<sub>x</sub> > 1.0 μF may cause a problem during power down (see Power-Down Considerations). Susceptibility to externally induced noise signals may occur for R<sub>x</sub> > 1.0 MΩ.

\*\* The HC4538A will function at 2.0 V but for optimum pulse width stability, V<sub>CC</sub> should be above 3.0 V.

NOTE: Information on typical parametric values can be found in Chapter 4.

# MC54/74HC4538A

DC CHARACTERISTICS FOR THE MC54/74HC4538A										
Symbol	Parameter	Test Conditions	VCC Volts	Guaranteed Limits						Unit
				25°C to -55°C		≤85°C		≤125°C		
				Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5		1.5		1.5		V
			4.5	3.15		3.15		3.15		
			6.0	4.2		4.2		4.2		
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0		0.5		0.5		0.5	V
			4.5		1.35		1.35		1.35	
			6.0		1.8		1.8		1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9		1.9		1.9		V
			4.5	4.4		4.4		4.4		
		6.0	5.9		5.9		5.9			
		4.5	3.98		3.84		3.7			
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0		0.1		0.1		0.1	V
			4.5		0.1		0.1		0.1	
		6.0		0.1		0.1		0.1		
		4.5		0.26		0.33		0.4		
I <sub>in</sub>	Maximum Input Leakage Current (A, B, Reset)	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0		±0.1		±1.0		±1.0	μA
I <sub>in</sub>	Maximum Input Leakage Current (R <sub>x</sub> , C <sub>x</sub> )	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0		±50		±500		±500	nA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package) Standby State	V <sub>in</sub> = V <sub>CC</sub> or GND Q1 and Q2 = Low I <sub>out</sub> = 0 μA	6.0		130		220		350	μA

I <sub>CC</sub>	Maximum Supply Current (per package) Active State	V <sub>in</sub> = V <sub>CC</sub> or GND Q1 and Q2 = High I <sub>out</sub> = 0 μA Pins 2 and 14 = 0.5 V <sub>CC</sub>	6.0	25°C		-45°C to 85°C		-55°C to 125°C		μA
					400		600		800	

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# MC54/74HC4538A

AC CHARACTERISTICS FOR THE MC54/74HC4538A ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)									
Symbol	Parameter	VCC Volts	Guaranteed Limits						Unit
			25°C to -55°C		≤85°C		≤125°C		
			Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Maximum Propagation Delay Input A or B to Q (Figures 6 and 8)	2.0		175		220		265	ns
		4.5		35		44		53	
		6.0		30		37		45	
t <sub>PHL</sub>	Maximum Propagation Delay Input A or B to NQ (Figures 6 and 8)	2.0		195		245		295	ns
		4.5		39		49		59	
		6.0		33		42		50	
t <sub>PHL</sub>	Maximum Propagation Delay Reset to Q (Figures 7 and 8)	2.0		175		220		265	ns
		4.5		35		44		53	
		6.0		30		37		45	
t <sub>PLH</sub>	Maximum Propagation Delay Reset to NQ (Figures 7 and 8)	2.0		175		220		265	ns
		4.5		35		44		53	
		6.0		30		37		45	
t <sub>T LH</sub> , t <sub>T HL</sub>	Maximum Output Transition Time, Any Output (Figures 7 and 8)	2.0		75		95		110	ns
		4.5		15		19		22	
		6.0		13		16		19	
C <sub>in</sub>	Maximum Input Capacitance (A, B, Reset) (C <sub>x</sub> , R <sub>x</sub> )	—		10		10		10	pF
				25		25		25	

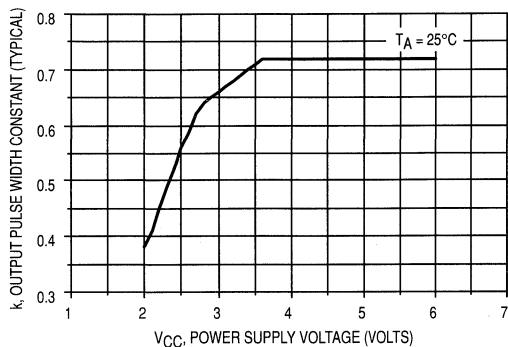
C <sub>pd</sub>	Power Dissipation Capacitance (per Multivibrator) Used to determine no-load dynamic power consumption: $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V						pF
		150						

TIMING CHARACTERISTICS FOR THE MC54/74HC4538A (Input $t_r = t_f = 6.0$ ns)									
Symbol	Parameter	VCC Volts	Guaranteed Limits						Unit
			25°C to -55°C		≤85°C		≤125°C		
			Min	Max	Min	Max	Min	Max	
t <sub>rec</sub>	Minimum Recovery Time, Inactive to A or B (Figure 7)	2.0	0		0		0		ns
		4.5	0		0		0		
		6.0	0		0		0		
t <sub>w</sub>	Minimum Pulse Width, Input A or B (Figure 6)	2.0	60		75		90		ns
		4.5	12		15		18		
		6.0	10		13		15		
t <sub>w</sub>	Minimum Pulse Width, Reset (Figure 7)	2.0	60		75		90		ns
		4.5	12		15		18		
		6.0	10		13		15		
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times, Reset (Figure 7)	2.0		1000		1000		1000	ns
		4.5		500		500		500	
		6.0		400		400		400	
	A or B (Figure 7)	2.0	No Limit						
		4.5							
		6.0							

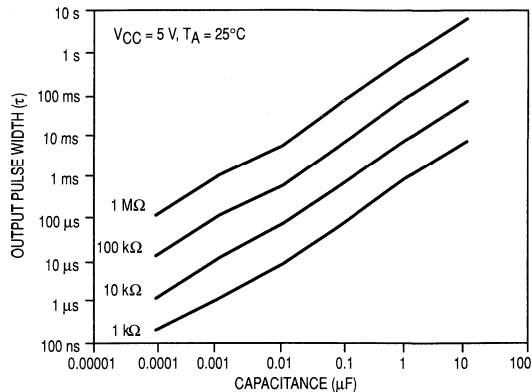
# MC54/74HC4538A

OUTPUT PULSE WIDTH CHARACTERISTICS ( $C_L = 50$ pF)											
Symbol	Parameter	Conditions			Guaranteed Limits						Unit
		Timing Components	$V_{CC}$ Volts	25°C to -55°C		≤85°C		≤125°C			
				Min	Max	Min	Max	Min	Max		
$\tau$	Output Pulse Width* (Figures 6 and 8)	$R_X = 10$ k $\Omega$ , $C_X = 0.1$ $\mu$ F	5.0	0.63	0.77	0.6	0.8	0.59	0.81	ms	
—	Pulse Width Match Between Circuits in the same Package	—	—	±5.0						%	
—	Pulse Width Match Variation (Part to Part)	—	—	±10						%	

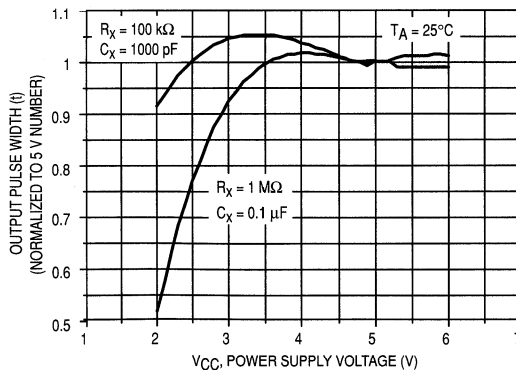
\*For output pulse widths greater than 100  $\mu$ s, typically  $\tau = kR_X C_X$ , where the value of k may be found in Figure 1.



**Figure 1. Typical Output Pulse Width Constant, k, versus Supply Voltage**  
(For output pulse widths >100  $\mu$ s:  $\tau = kR_X C_X$ )



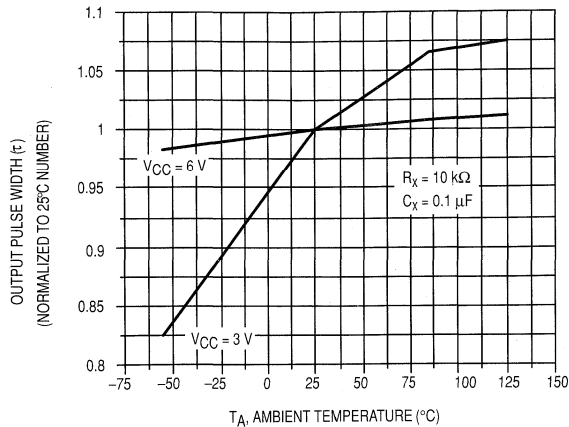
**Figure 2. Output Pulse Width versus Timing Capacitance**



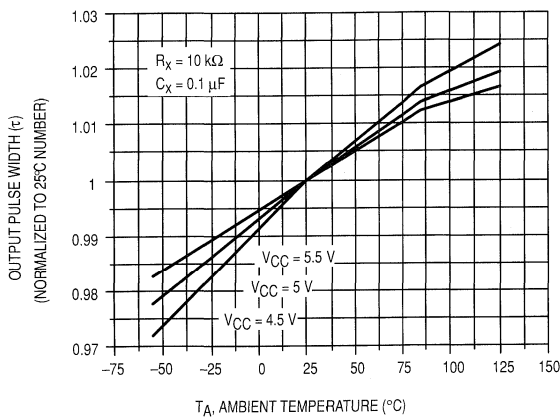
**Figure 3. Normalized Output Pulse Width versus Power Supply Voltage**



# MC54/74HC4538A



**Figure 4. Normalized Output Pulse Width versus Power Supply Voltage**



**Figure 5. Normalized Output Pulse Width versus Power Supply Voltage**

# MC54/74HC4538A

## SWITCHING WAVEFORMS

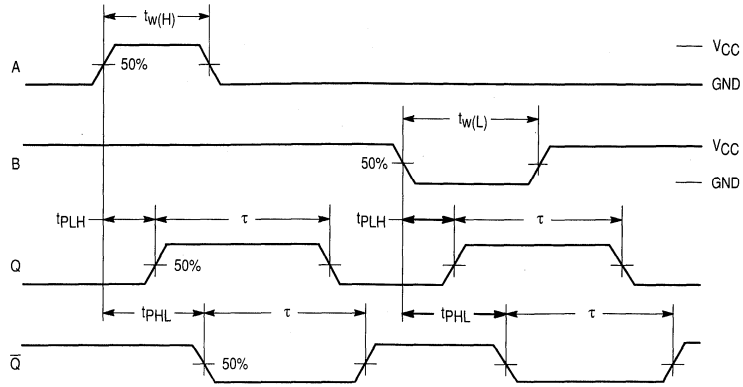


Figure 6.

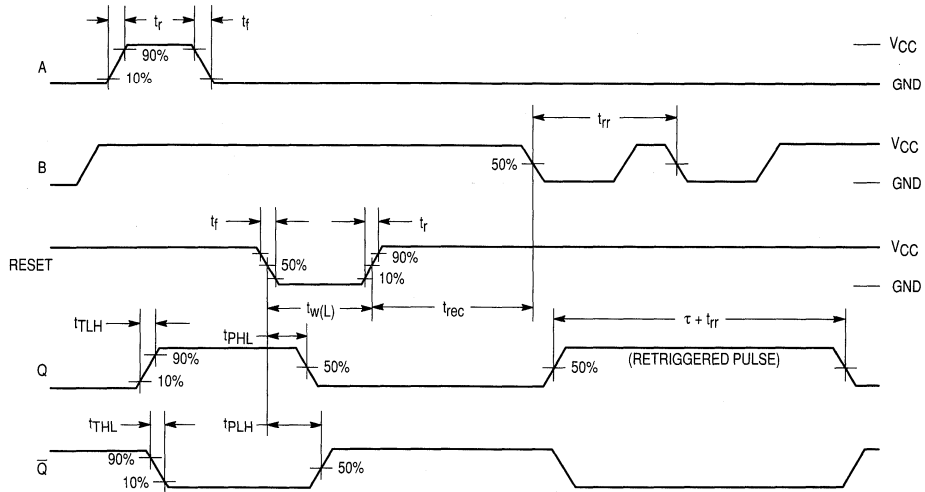
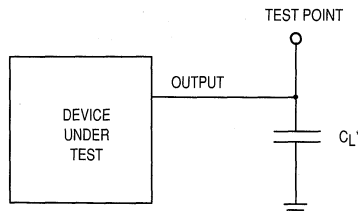


Figure 7.



\*Includes all probe and jig capacitance

Figure 8. Test Circuit

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# MC54/74HC4538A

## PIN DESCRIPTIONS

### INPUTS

**A1, A2 (PINS 4, 12)** — Positive-edge trigger inputs. A rising-edge signal on either of these pins triggers the corresponding multivibrator when there is a high level on the B1 or B2 input.

**B1, B2 (PINS 5, 11)** — Negative-edge trigger inputs. A falling-edge signal on either of these pins triggers the corresponding multivibrator when there is a low level on the A1 or A2 input.

**RESET 1, RESET 2 (PINS 3, 13)** — Reset inputs (active low). When a low level is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low level and the  $\bar{Q}$  output is set to a high level.

**C<sub>X</sub>1/R<sub>X</sub>1 and C<sub>X</sub>2/R<sub>X</sub>2 (PINS 2 and 14)** — External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram). Polystyrene capacitors are recommended for optimum

pulse width control. Electrolytic capacitors are not recommended due to high leakages associated with these type capacitors.

**GND (PINS 1 and 15)** — External ground. The external timing capacitors discharge to ground through these pins.

### OUTPUTS

**Q1, Q2 (PINS 6, 10)** — Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R<sub>X</sub> and C<sub>X</sub>.

**$\bar{Q}1, \bar{Q}2$  (PINS 7, 9)** — Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

### LOGIC DETAIL (1/2 THE DEVICE)

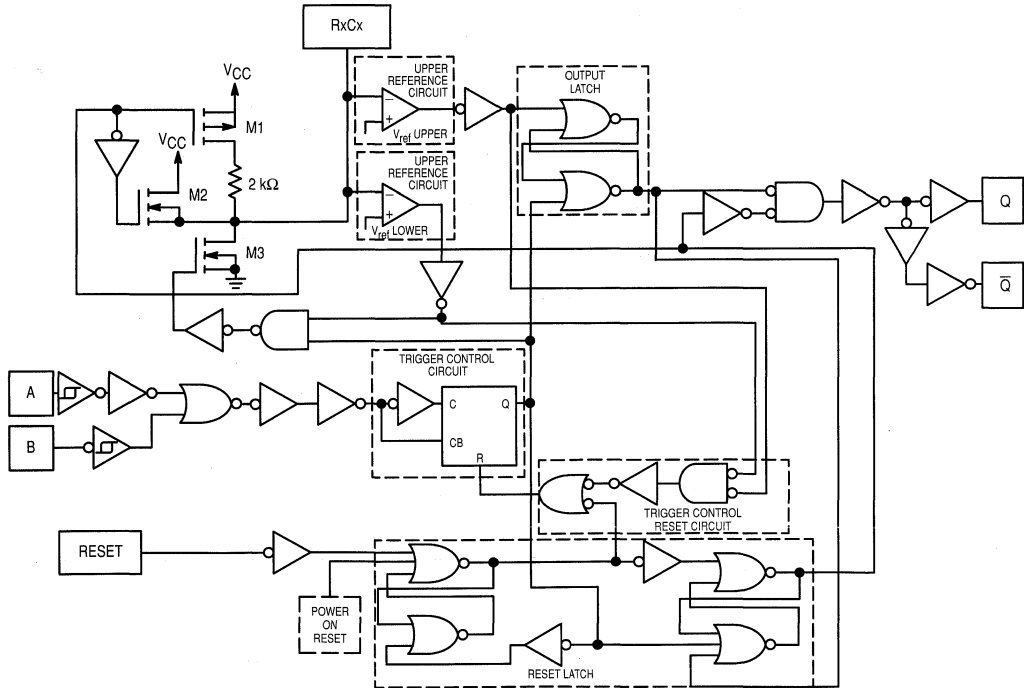


Figure 9.

# MC54/74HC4538A

## CIRCUIT OPERATION

Figure 12 shows the HC4538A configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 10): In the quiescent state, the external timing capacitor,  $C_X$ , is charged to  $V_{CC}$ . When a trigger occurs, the Q output goes high and  $C_X$  discharges quickly to the lower reference voltage ( $V_{ref\ Lower} \approx 1/3 V_{CC}$ ).  $C_X$  then charges, through  $R_X$ , back up to the upper reference voltage ( $V_{ref\ Upper} \approx 2/3 V_{CC}$ ), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic detail (Figure 9) and the timing diagram (Figure 10).

### QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 10). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 10).

The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor,  $C_X$ , is charged to  $V_{CC}$  (#4), and both the upper and lower reference circuit has a low output (#5).

In addition, the output of the trigger-control reset circuit is low.

### TRIGGER OPERATION

The HC4538A is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously initiates two events. First, the output latch goes low, thus taking the Q output of the HC4538A to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor,  $C_X$ , to rapidly discharge toward ground (#11). (Note that the voltage across  $C_X$  appears at the input of both the upper and lower reference circuit comparator).

When  $C_X$  discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing  $C_X$  to begin to charge back up toward  $V_{CC}$ , with a time constant  $t = R_X C_X$  (#15). Once the voltage across  $C_X$  charges to above the lower reference voltage, the lower reference circuit will go low allowing the monostable multivibrator to be retriggered.

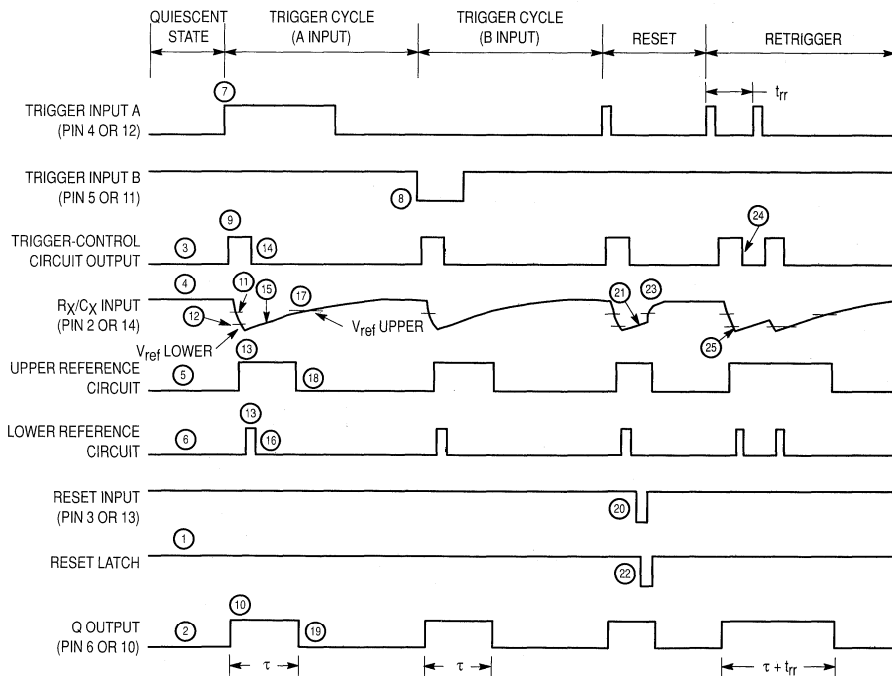


Figure 10. Timing Diagram

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# MC54/74HC4538A

When  $C_X$  charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the HC4538A to a low state (#19), and completing the time-out cycle.

## POWER-DOWN CONSIDERATIONS

Large values of  $C_X$  may cause problems when powering down the HC4538A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from  $V_{CC}$  through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the  $V_{CC}$  power supply must not be faster than  $t = V_{CC} \cdot C_X / (30 \text{ mA})$ . For example, if  $V_{CC} = 5.0 \text{ V}$  and  $C_X = 15 \mu\text{F}$ , the  $V_{CC}$  supply must turn off no faster than  $t = (5.0 \text{ V}) \cdot (15 \mu\text{F}) / 30 \text{ mA} = 2.5 \text{ ms}$ . This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of  $V_{CC}$  to zero volts occurs, the HC4538A may sustain damage. To avoid this possibility, use an external damping diode,  $D_X$ , connected as shown in Figure 11. Best results can be achieved if diode  $D_X$  is chosen to be a germanium or Schottky type diode able to withstand large current surges.

## RESET AND POWER ON RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the HC4538A to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while  $C_X$  is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus  $C_X$  is allowed to quickly charge up to  $V_{CC}$  (#23) to await the next trigger signal.

On power up of the HC4538A the power-on reset circuit will be high causing a reset condition. This will prevent the trigger-control circuit from accepting a trigger input during this state. The HC4538A's Q outputs are low and the  $\bar{Q}$  not outputs are high.

## RETRIGGER OPERATION

When used in the retriggerable mode (Figure 12), the HC4538A may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24), and the voltage across  $C_X$  is above the lower reference voltage. As long as the  $C_X$  voltage is below the lower reference voltage, the reset of the flip-flop is high, disabling any trigger pulse. This prevents M3 from turning on during this period resulting in an output pulse width that is predictable.

The amount of undershoot voltage on  $R_X C_X$  during the trigger mode is a function of loop delay, M3 conductivity, and  $V_{DD}$ . Minimum retrigger time,  $t_{rr}$  (Figure 7), is a function of 1) time to discharge  $R_X C_X$  from  $V_{DD}$  to lower reference voltage ( $T_{\text{discharge}}$ ); 2) loop delay ( $T_{\text{delay}}$ ); 3) time to charge  $R_X C_X$  from the undershoot voltage back to the lower reference voltage ( $T_{\text{charge}}$ ).

Figure 13 shows the device configured in the nonretriggerable mode.

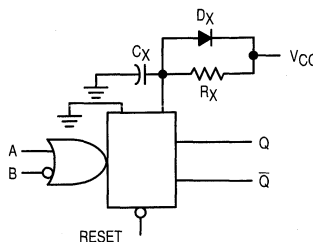


Figure 11. Discharge Protection During Power Down

# MC54/74HC4538A

## TYPICAL APPLICATIONS

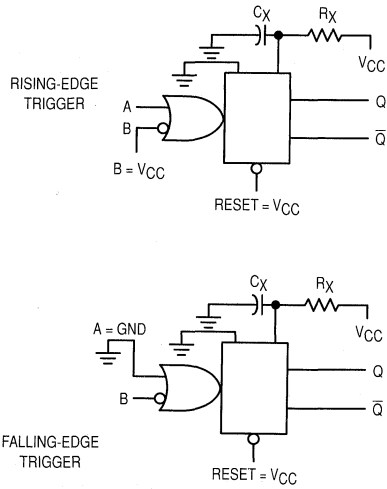


Figure 12. Retriggerable Monostable Circuitry

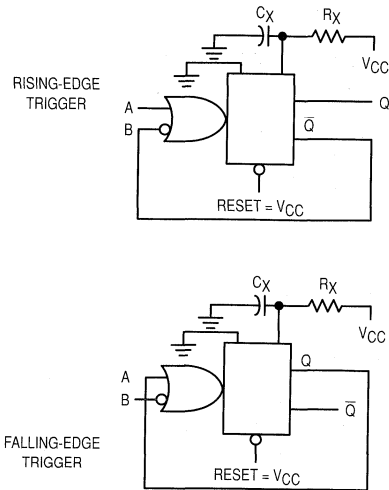
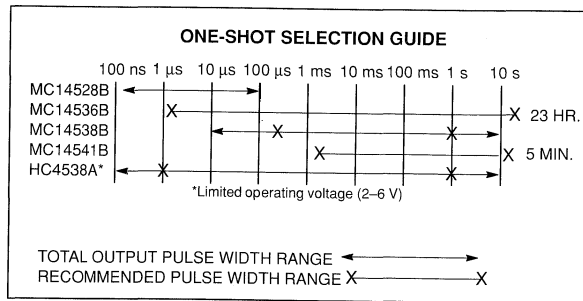


Figure 13. Non-retriggerable Monostable Circuitry



# Quad 2-Input Exclusive NOR Gate

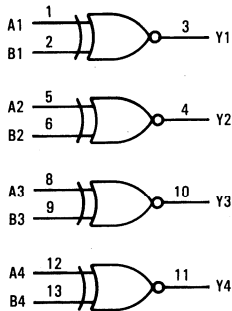
## High-Performance Silicon-Gate CMOS

The MC54/74HC7266 is identical in pinout to the LS266 and the HC266. The HC7266 has standard CMOS outputs instead of open-drain outputs.

The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates

### LOGIC DIAGRAM

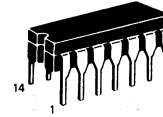


$$Y = \overline{A \oplus B}$$

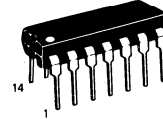
$$= AB + \overline{A} \overline{B}$$

PIN 14 = V<sub>CC</sub>  
 PIN 7 = GND

## MC54/74HC7266



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06



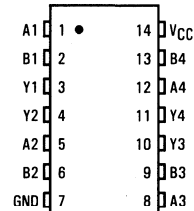
D SUFFIX  
 SOIC  
 CASE 751A-02

### ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

# MC54/74HC7266

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 4.

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# MC54/74HC7266

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

### NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		33	

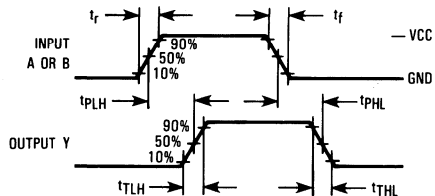
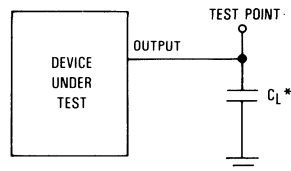


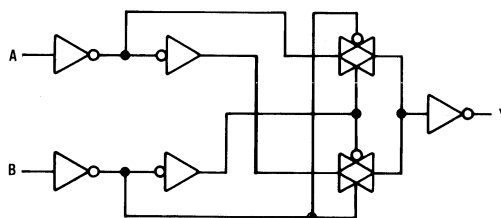
Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 2. Test Circuit

### LOGIC DETAIL (1/4 of Device)



APPLICATION INFORMATION

Bi  $\phi$ -L is defined as biphas-level code. Also known as Manchester Code, this technique utilizes binary phase shift keying (PSK). The Bi  $\phi$ -L output shown in Figure 3 carries both data and synchronization information; therefore, separate data and clock lines are not required to transfer information. A positive-going transition in the middle of the bit interval

indicates a logic zero; a negative-going transition indicates a logic one (see Figure 4).

NRZ-L shown in Figure 3 is non-return-to-zero level code. This is simply serial data out of a shift register, such as the HC597.

The Bi  $\phi$ -L signal must be phase coherent (i.e., no glitches). Therefore, NRZ-L and clock transitions must be coincident.

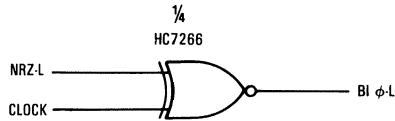


Figure 3. Biphase-Level Encoder (Manchester Encoder)

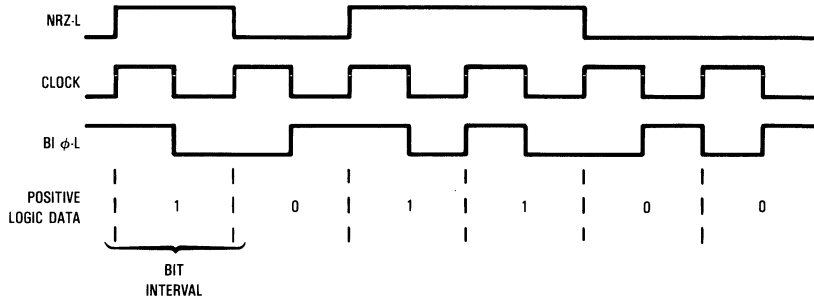


Figure 4. Timing Diagram

5

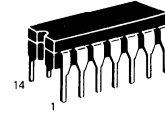
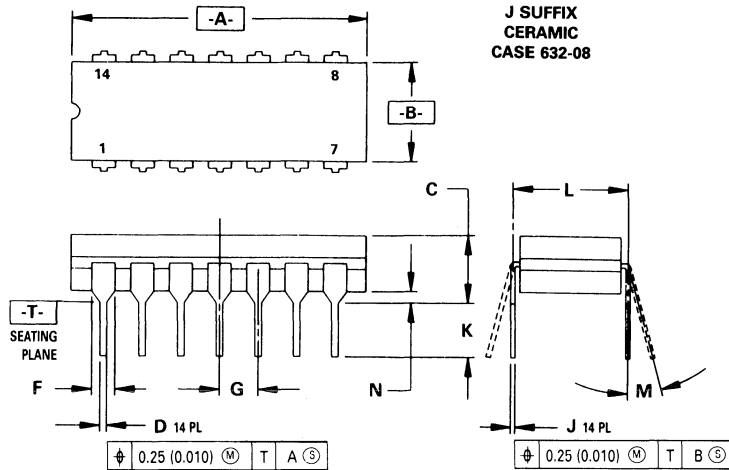
# Package Dimensions

6

# PACKAGE DIMENSIONS

The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

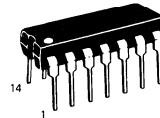
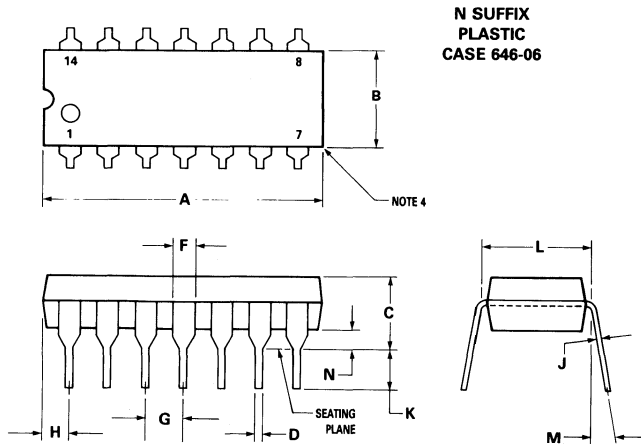
## 14-PIN PACKAGES



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

**NOTES:**

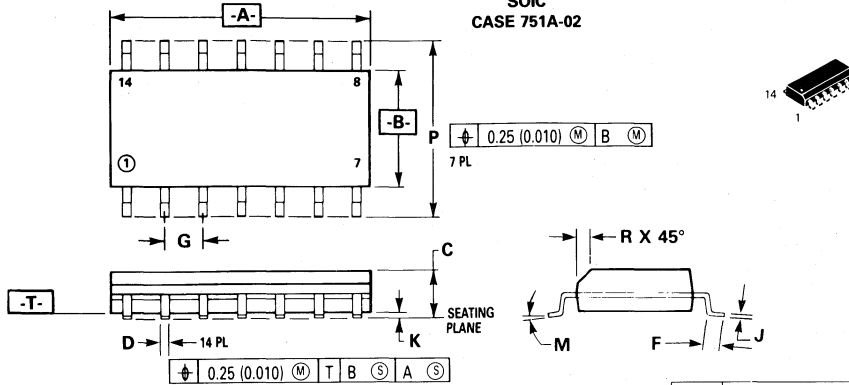
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.

6

# PACKAGE DIMENSIONS

## 14-PIN PACKAGES

D SUFFIX  
SOIC  
CASE 751A-02



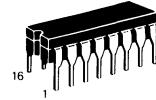
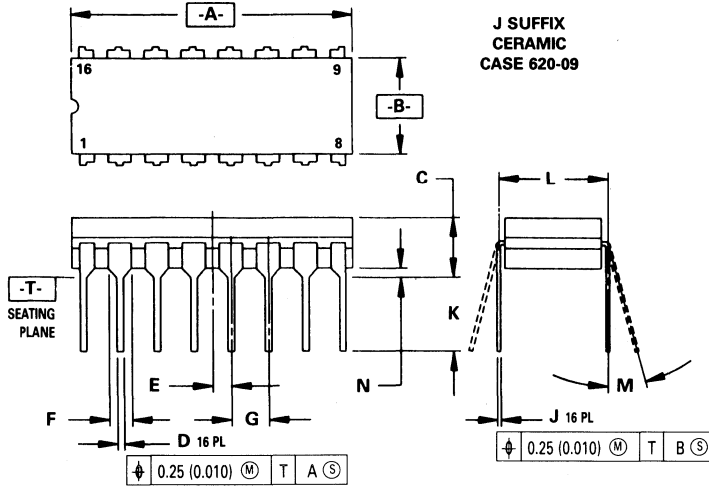
NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

# PACKAGE DIMENSIONS

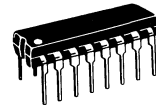
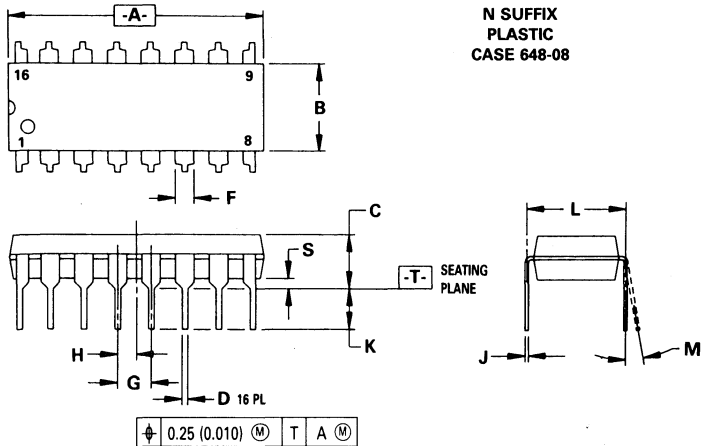
## 16-PIN PACKAGES



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

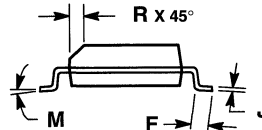
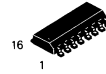
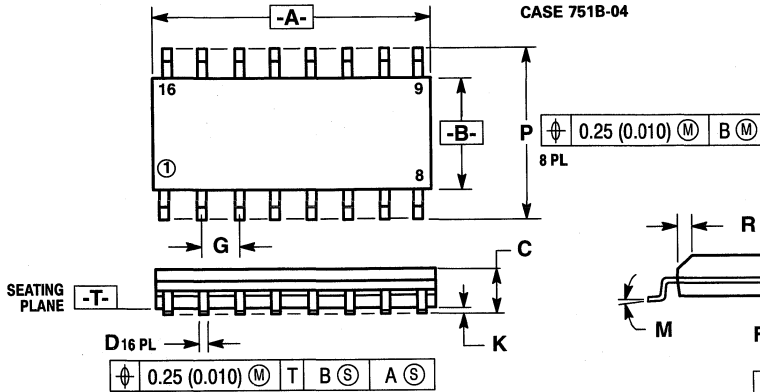
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

# PACKAGE DIMENSIONS

## 16-PIN PACKAGES

D SUFFIX  
SOIC  
CASE 751B-04

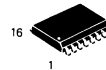
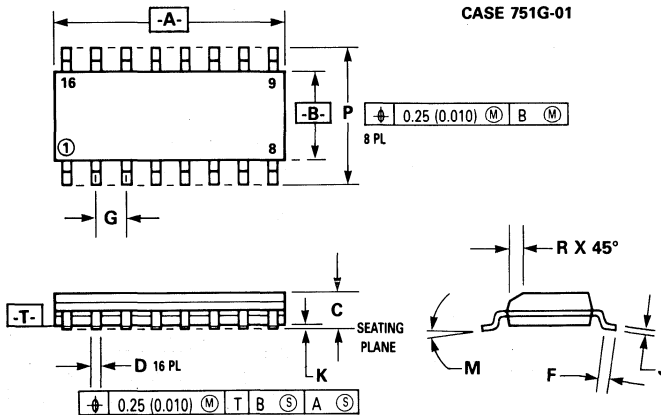


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751B-03 IS OBSOLETE, NEW STANDARD 751B-04.

DW SUFFIX  
SOIC  
CASE 751G-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029

NOTES:

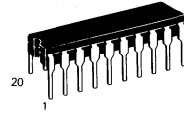
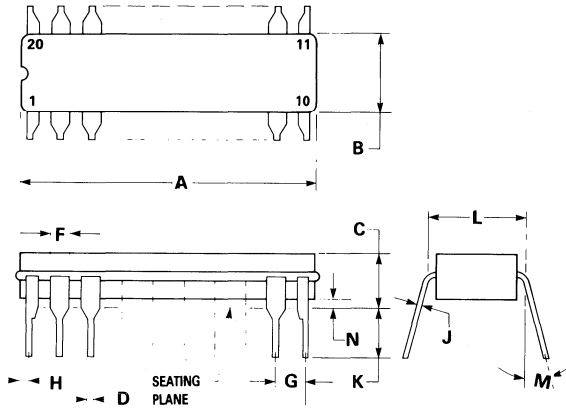
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

6

# PACKAGE DIMENSIONS

## 20-PIN PACKAGES

### J SUFFIX CERAMIC CASE 732-03

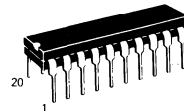
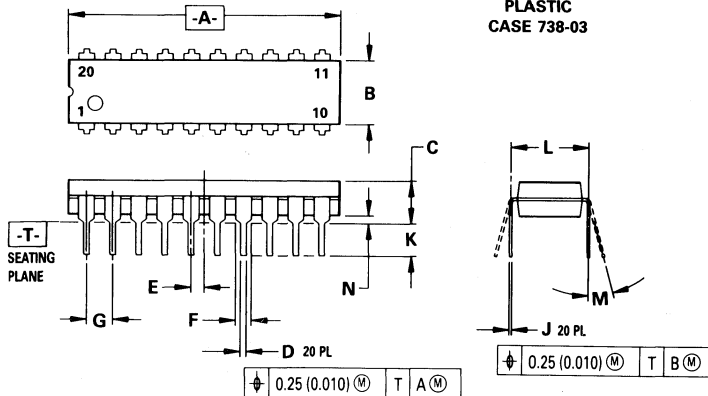


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

**NOTES:**

- LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
- DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIM A AND B INCLUDES MENISCUS.

### N SUFFIX PLASTIC CASE 738-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

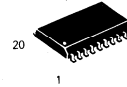
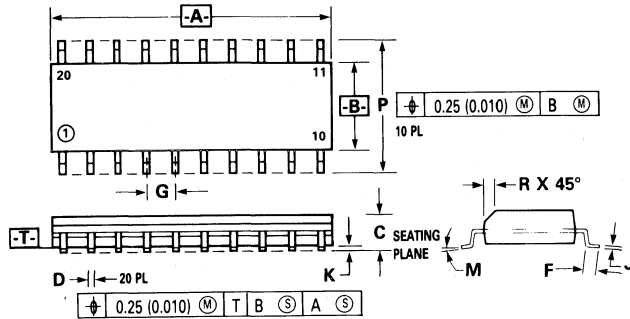
6



# PACKAGE DIMENSIONS

## 20-PIN PACKAGES

DW SUFFIX  
SOIC  
CASE 751D-03



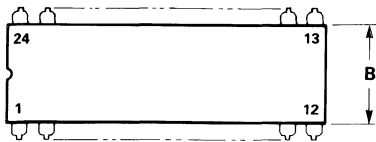
NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

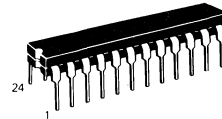
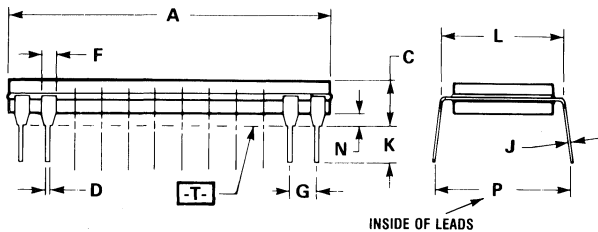
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
<b>A</b>	12.65	12.95	0.499	0.510
<b>B</b>	7.40	7.60	0.292	0.299
<b>C</b>	2.35	2.65	0.093	0.104
<b>D</b>	0.35	0.49	0.014	0.019
<b>F</b>	0.50	0.90	0.020	0.035
<b>G</b>	1.27 BSC		0.050 BSC	
<b>J</b>	0.25	0.32	0.010	0.012
<b>K</b>	0.10	0.25	0.004	0.009
<b>M</b>	0°	7°	0°	7°
<b>P</b>	10.05	10.55	0.395	0.415
<b>R</b>	0.25	0.75	0.010	0.029

# PACKAGE DIMENSIONS

## 24-PIN PACKAGES



**J SUFFIX  
CERAMIC  
CASE 758-01**

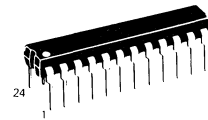
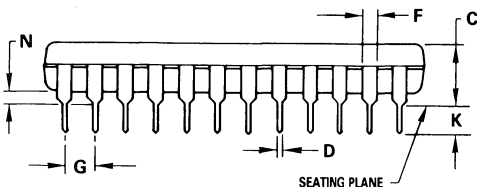
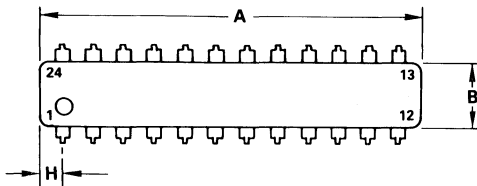


**NOTES:**

1. DIMENSION A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES  
 $\pm 0.25 (0.010) \text{ (M) T A (M)}$
3. **-T-** IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

**N SUFFIX  
PLASTIC  
CASE 724-03**



**NOTES:**

1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).
2. CHAMFERED CONTOUR OPTIONAL.

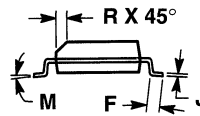
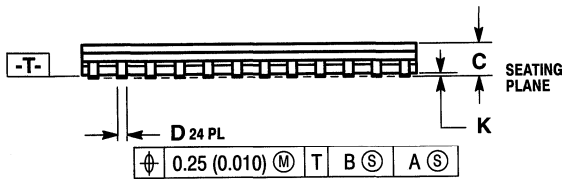
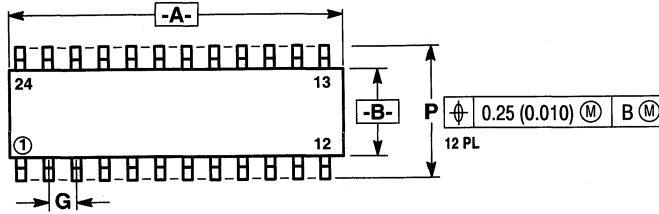
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.13	1.230	1.265
B	6.35	6.86	0.250	0.270
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040

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# PACKAGE DIMENSIONS

## 24-PIN PACKAGES

DW SUFFIX  
PLASTIC  
CASE 751E-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751E-01 AND -02 OBSOLETE, NEW STANDARD 751E-03.















**1** **Alphanumeric  
Index**

**2** **Function  
Selector Guide**

**3** **Definitions and  
Glossary of Terms**

**4** **Design  
Considerations**

**5** **Data Sheets**

**6** **Package  
Dimensions**





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